Instruction set Architecture

Limitations of 8085 ISA :

Less number of registers: 8085 has very few number of registers which require more number of memory accesses and hence it is slow.

More number of cycles: To complete one instruction upto 3 cycles are required to complete it and hence takes more time. For example : LDA 2048H requires 3 cycles.

Heavy dependency on accumulator: All the arithmatic operations are performed via accumulator register hence it becomes difficult to keep track of data.

Register Size: Register size is small and hence two registers are required to store one address instead of just 1 register.

Complex Instructions missing: Instructions like Multiplication, Division, Loops are absent.

Proposed ISA

Address Bus	:	16 bits (hence 64K total memory)
Data Bus	:	32 bits
Register Size	:	32 bits
Word Size	:	32 bits
Number of Registers	:	32
Memory Model	:	Aligned memory model

Since accessing memory is relatively slow, hence many registers are required so that once a word is fetched it can be kept in register until it is no longer needed. Hence we have 32 registers.

Types of addressing mode supported:
Direct Addressing Mode
Indirect Addressing Mode
Immediate Addressing Mode
Register Addressing Mode

Registers :
General purpose : 27
Special Registers : 5

5 bits are required to represent 32 registers.

00000	A
00001	B
00010	C
....	
...	
...	
...	
11010	ZA
11011	ME(16 bit register which store the address and whenever called will fetch the data from that memory location which stored in M(Indirect))
11100	Instruction Register
11101	Program Counter
11110	Stack Pointer
11111	Flag Register

Flag Register:
000**Z** 000**C** 000**P** 000**A** 000**S** 0000 0000 0000
Zero Flag, Carry Flag, Parity Flag, Auxillary Carry, Sign Flag

EXPANDING OPCODES

Mnemonic	Opcode length	Opcode	Register bits (Number of registers)	Memory bits	Type of mode
LDR	11	000.....000	5(1)	16(1)	DIRECT
STR	11	000....001	5(1)	16(1)	DIRECT
MAI	11	000...010	5(1)	16(1)	IMMEDIATE
JZR(Jump if register value zero)	11	000...011	5(1)	16(1)	REGISTER
JUM	16	000..100 00000	X	16(1)	IMMEDIATE
JMC	16	000..100 00001	X	16(1)	IMMEDIATE
JMZ	16	000..100 00010	X	16(1)	IMMEDIATE
JMP	16	000..100 00011	X	16(1)	IMMEDIATE
MVR (especial case with ME register)	22	00..101 00..000	5(2)	X	REGISTER
ADD	22	00..101 00..001	5(2)	X	REGISTER
SUB	22	00..101 00..010	5(2)	X	REGISTER
MUL	22	00..101 00..011	5(2)	X	REGISTER
DIV	22	00..101 00..100	5(2)	X	REGISTER
MOD	22	00..101 00..101	5(2)	X	REGISTER
OR2	22	00..101 00..110	5(2)	X	REGISTER
AND	22	00..101 00..111	5(2)	X	REGISTER
XOR	22	00..101 00.....1000	5(2)	X	REGISTER
COM (Only flags will be changed)	22	00..101 00....1001	5(2)	X	REGISTER
STI(Store Indirect) Copy content of register 1 to address pointed by register 2	22	00..101 00....1010	5(2)	X	REGISTER
NOT	27	00..101 0..10000 00000	5(1)	X	REGISTER
MOI	27	00..101 0..10000 00001	5(1)	X	IMMEDIATE
ADI	27	00..101 0..10000 00010	5(1)	X	IMMEDIATE
SUI	27	00..101 0..10000 00011	5(1)	X	IMMEDIATE
MUI	27	00..101 0..10000 00100	5(1)	X	IMMEDIATE
DVI	27	00..101 0..10000 00101	5(1)	X	IMMEDIATE

MDI	27	00..101 0..10000 00110	5(1)	X	IMMEDIATE
ANI	27	00..101 0..10000 00111	5(1)	X	IMMEDIATE
ORI	27	00..101 0..10000 01000	5(1)	X	IMMEDIATE
INC	27	00..101 0..10000 01001	5(1)	X	REGISTER
DEC	27	00..101 0..10000 01010	5(1)	X	REGISTER
LHS	27	00..101 0..10000 01011	5(1)	X	REGISTER
RHS	27	00..101 0..10000 01100	5(1)	X	REGISTER
PSH	27	00..101 0..10000 01101	5(1)	X	REGISTER
POP	27	00..101 0..10000 01110	5(1)	X	REGISTER
OUT	27	00..101 0..10000 01111	5(1)	X	IMMEDIATE
INP	27	00..101 0..10000 10000	5(1)	X	IMMEDIATE
LOP	27	00..101 0..10000 10001	5(1)	X	REGISTER
ELP	32	00..101 0..10000 10100 00000	X	X	NONE
HLT	32	00..101 0..10000 10100 00001	X	X	NONE
NOP	32	00..101 0..10000 10100 00010	X	X	NONE