Week 1: Practice Problems

1. Which statement is false concerning Moore's Law?

    a. The term was named for Gordon Moore.
    b. Gordon Moore was one of the founders of IBM.
    c. In the 1960s the storage density of integrated circuits on a silicon chip doubled about every year.
    d. Today, when we speak of Moore's Law we refer to the doubling of computer power every 18 months.

2. Which of the following statements are true during the read operation?

    a. Issue the control signal READ.
    b. The data to be read from memory is stored into MAR.
    c. The data to be read from memory is stored into IR.
    d. The data to be read from memory is stored into MDR.

3. The Instruction Register (IR).

    a. Holds the memory address of the next instruction.
    b. Holds the memory address of the current instruction.
    c. Holds the encoded instruction that is currently being executed or decoded.
    d. Holds the executed or decodedinstruction.

4. The register R_1 = 12, and R_2= 13. The instruction ADD R_1, R_2 is in memory location 2000H. After the execution of the instruction the value of PC, MAR, IR and R1 are.

    a. PC= 2004H; MAR = 2004H; IR= ADD R1, R2; R1= 25.
    b. PC= 2000H;MAR = 2000H; IR= ADD R1, R2; R1= 12.
    c. PC= 2004H; MAR = 2004H; IR= ADD R1, R2; R1= 12.
    d. PC= 2004H;MAR = 2000H; IR= ADD R1, R2; R1= 25.

5. A computer has 1 MB of memory. Each word in this computer is 32 bytes. How many bits are needed to address any single word in memory?

    a. 20 bits to address each word.
    b. 32 bits to address each word.
    c. 12 bits to address each word.
    d. 15 bits to address each word.

6. Which of the following statements are true for a bus architecture?

    a. Only one data transfer allowed in one clock cycle for single bus architecture.
    b. Parallelism in data transfer is allowed in multi bus architecture only.
    c. The multi-bus architecture is supposedly faster than the single-bus architecture.
    d. Both the bus architecture have the same connection complexity.

7. The data 451Ah is to be represented in a byte addressable memory system starting from location 2000h using little endian format. The memory locations 2000h, 2001h will contain the data

    a. 45h, and 1Ah respectively.
    b. 1Ah, and 45h respectively.
    c. A1h, and 54h respectively.
    d. 54h, and A1h respectively.

8. Which of the following statements are true.

    a. In von-Neumann architecture, the instructions and data are stored in the same memory module.
    b. In Harvard architecture, the instructions and data are stored in separate memory module.
    c. Harvard architecture is more flexible compare to von-Neumann architecture.
    d. In Harvard architecture instructions and data accesses can be done in parallel.

9. The minimum number of instructions required to execute the statement A= B+C using stack-based architecture is _____.

10. Which statements are true for general purpose registers (GPRs) are.

    a. Faster than the memory.
    b. Slower than the memory.
    c. Non-volatile in nature.
    d. Newer architecture have a large number of GPRs.

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