PROJECT ON

VLSI

SELF PROJECT

AMIT PADEY

Design –

* Responsible for design of 5-bit shift - register for serial data input and assigning gain values to Amplifiers when 5- bit data is received.
* Responsible for designing block diagram of Backend Module.
* Tested Verilog code for different input conditions.
* Written and edited Verilog code for the Backend Module.
* Attempted Bonus question and responsible for designing counters for counting clock pulse of main clock and oscillator clock for estimating frequency of oscillator. Unable to store estimated frequency of oscillator in a register inside backend.
* Responsible for designing delay (count) to set Amplifiers and oscillator.
* Responsible for designing delay (count) to set ready when serial data is received.
* Responsible for designing code to reset whole chip when resetbAll is 0

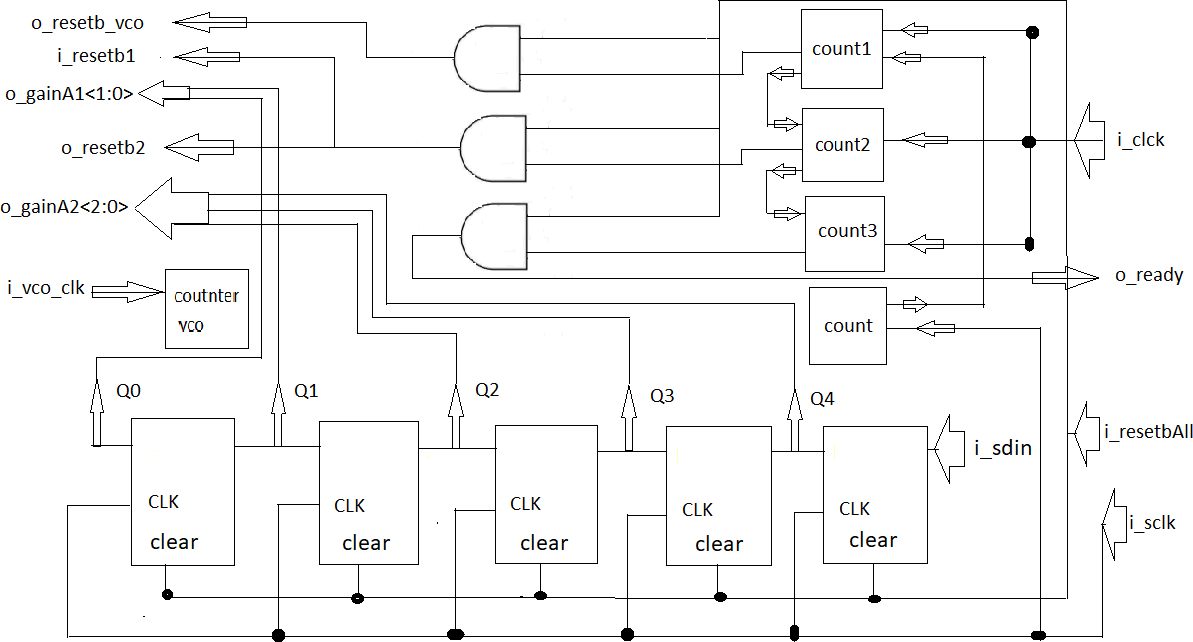


Fig: Block Diagram of Backend Module