PROJECT ON VLSI

SELF PROJECT

Design, layout of logic gates using electric tool and LT-Spice

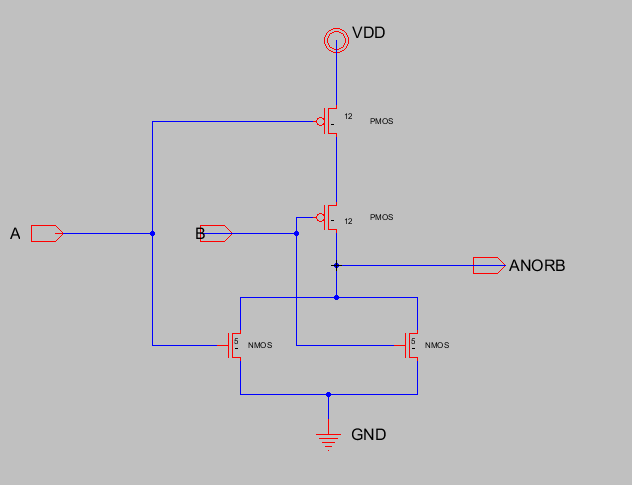
AMIT PADEY

M.TECH Y22

PHOTONIC SCIENCES AND ENGINEERING (PSE)

INDIAN INSTITUTE OF TECHNOLOGY, KANPUR

**First standard cell : 2-input NOR gate Schematic-**



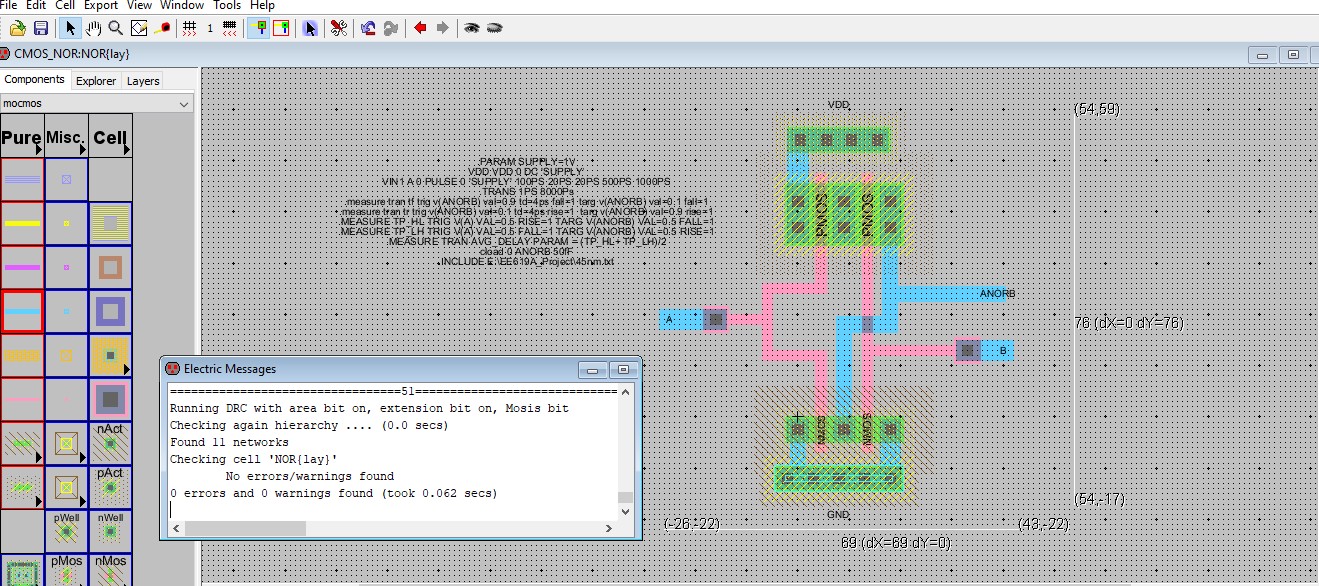
# Fig 1: NOR Schematic

**NOR gate sizing-** For choosing the sizes, I have applied following signal and measured its rise and fall time.

VIN1 A 0 PULSE 0 'SUPPLY' 100PS 20PS 20PS 500PS 1000PS VIN2 B 0 PULSE 0 'SUPPLY' 200PS 20PS 20PS 500PS 1000PS

And changed the sizes of p-MOS and n-MOS such that its rise and fall time becomes equal. The sizes of the n-MOS and p-MOS, for which rise and fall time are equal, I have chosen that size.

n-MOS=5 p-MOS=12



# Fig2: NOR LAYOUT WITH DRC LOG

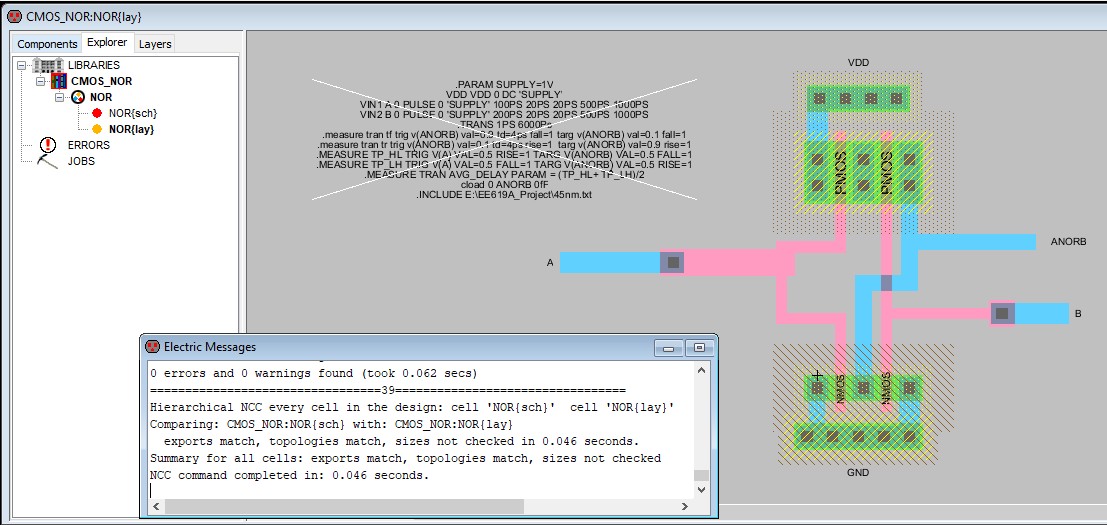


Fig3: NOR LAYOUT WITH LVS LOG

## Propagation delay-

Table – 1. Propagation delays from schematic

|  |  |  |  |
| --- | --- | --- | --- |
| Load (CL) | tphl | tplh | tp |
| 5 fF | 2.77 x 10-11 | 3.26 x 10-11 | 3.018 x 10-11 |
| 50 fF | 1.99 x 10-10 | 2.44 x 10-10 | 2.219 x 10-10 |

Table – 2. Propagation delays from layout

|  |  |  |  |
| --- | --- | --- | --- |
| Load (CL) | tphl | tplh | tp |
| 5 fF | 3.033 x 10-11 | 3.593 x 10-11 | 3.313 x 10-11 |
| 50 fF | 2.025 x 10-10 | 2.472 x 10-10 | 2.249 x 10-10 |

## Power consumption

Table – 3. Power Consumption

|  |  |  |
| --- | --- | --- |
|  | CL = 5 fF | CL = 50 fF |
| Schematic | -5.816uW | -41.72 uW |
| Layout | -6.5241 uW | -41.953 uW |

## Waveforms-

Input values used for generating waveforms-

VIN1 A 0 PULSE 0 'SUPPLY' 200PS 20PS 20PS 900PS 2000PS VIN2 B 0 PULSE 0 'SUPPLY' 2200PS 20PS 20PS 900PS 2000PS

.TRANS 1PS 8000Ps

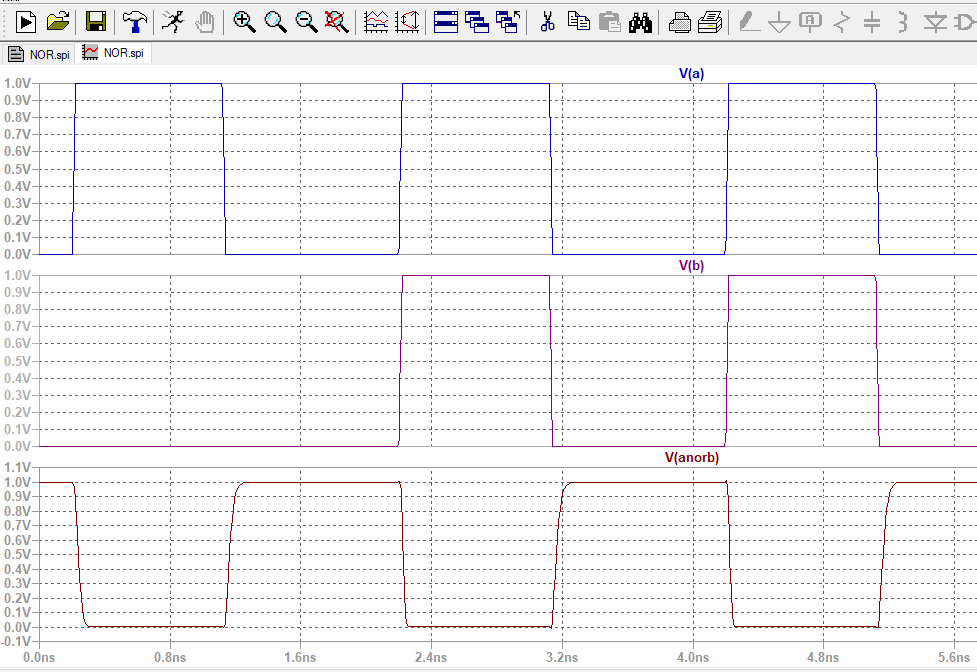


Fig 4: Waveform from schematic of input and output for 5fF

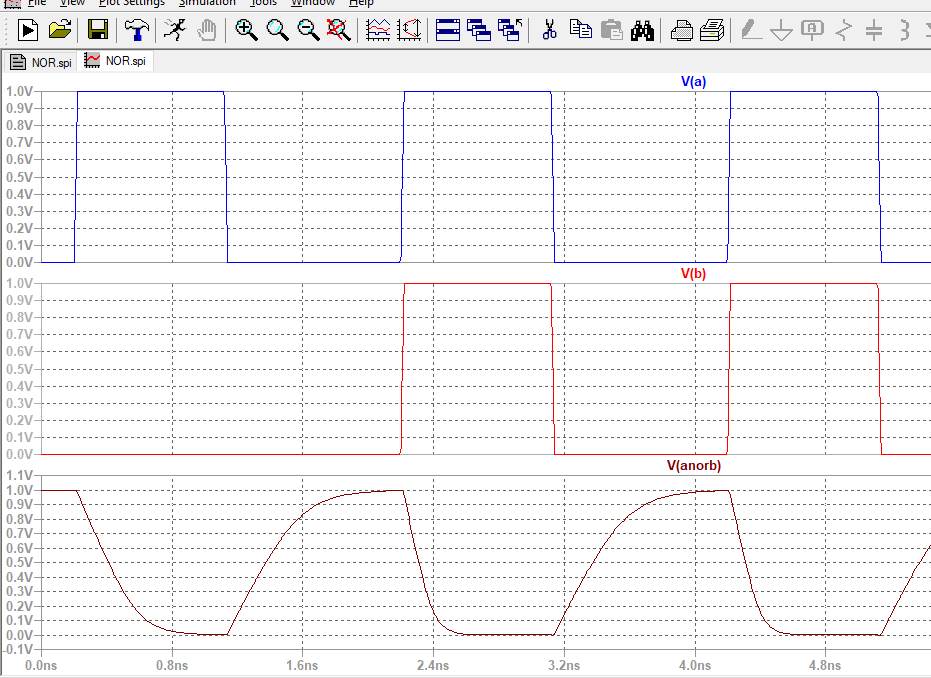


Fig 5: Waveform from schematic of input and output for 5fF

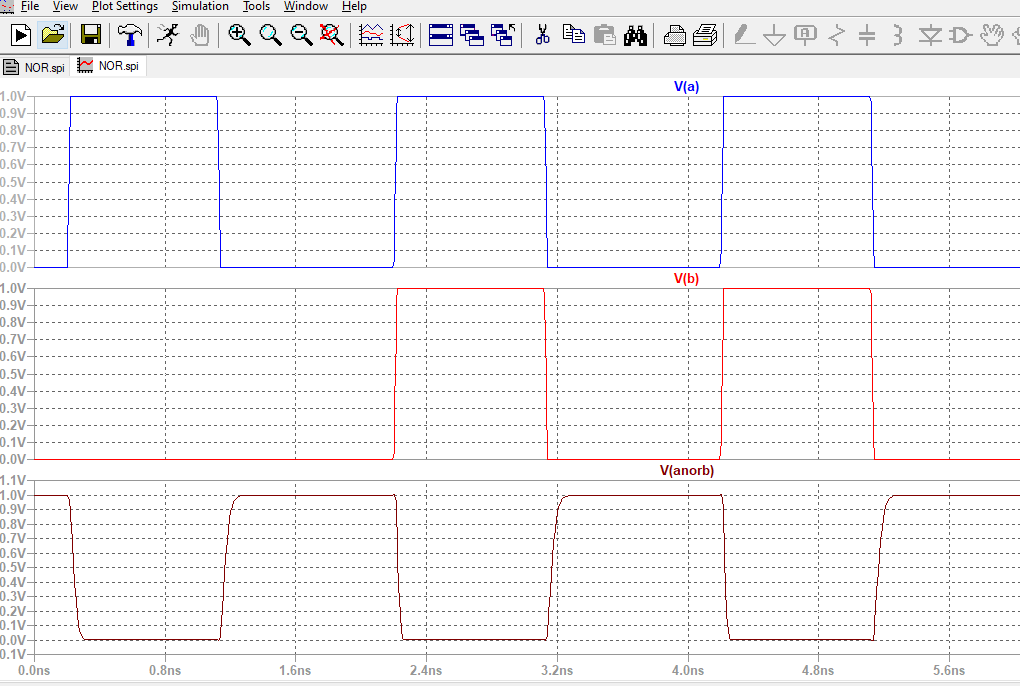


Fig 6: Waveform from Layout of input and output for 5fF

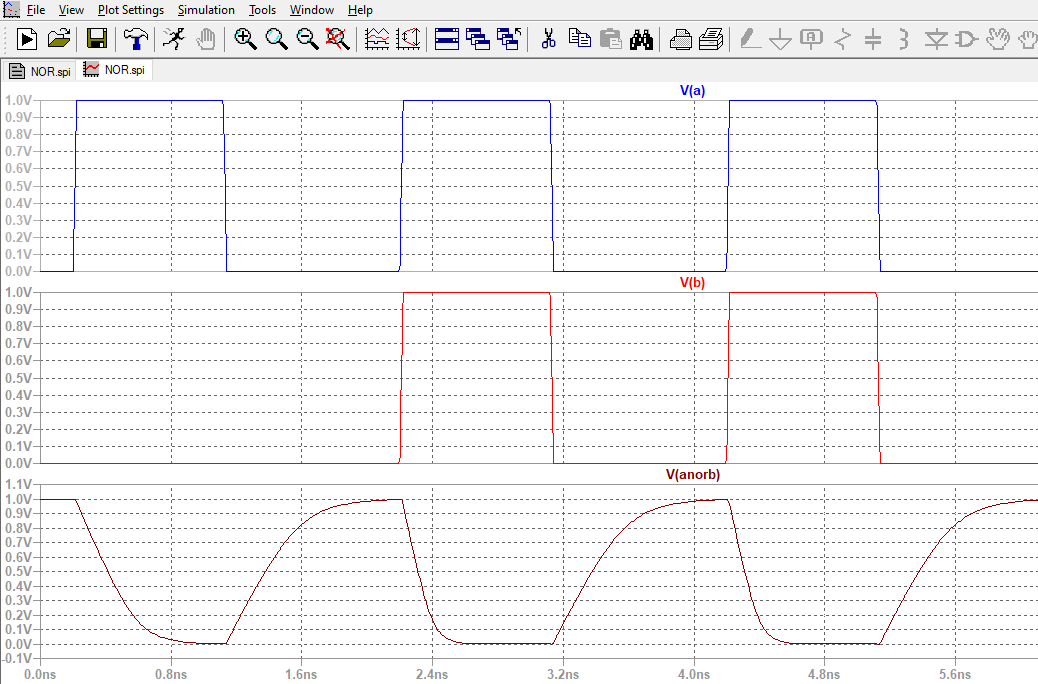


Fig 7: Waveform from Layout of input and output for 5fF

## Second standard cell : 2-input NAND gate Schematic-

Fig – 1. NAND Schematic

**NAND gate sizing-** For choosing the sizes, I have applied following signal and measured its rise and fall time.

VIN1 A 0 PULSE 0 'SUPPLY' 100PS 20PS 20PS 300PS 500PS VIN2 B 0 PULSE 0 'SUPPLY' 640PS 20PS 20PS 200PS 500PS

And changed the sizes of p-MOS and n-MOS such that its rise and fall time becomes equal. The sizes of the n-MOS and p-MOS, for which rise and fall time are equal, I have chosen that size.

n-MOS=6 p-MOS=10

## Layout with the DRC log

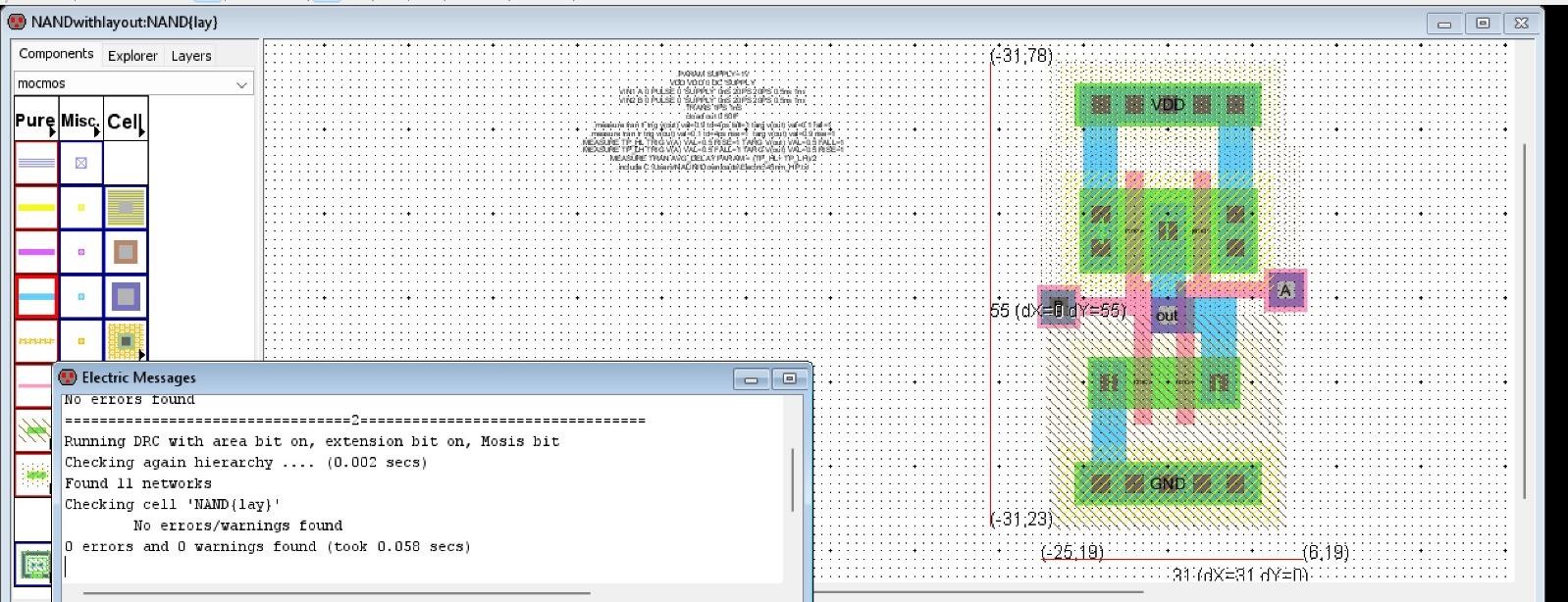


Fig – 2. NAND with DRC log

## Layout with the LVS log

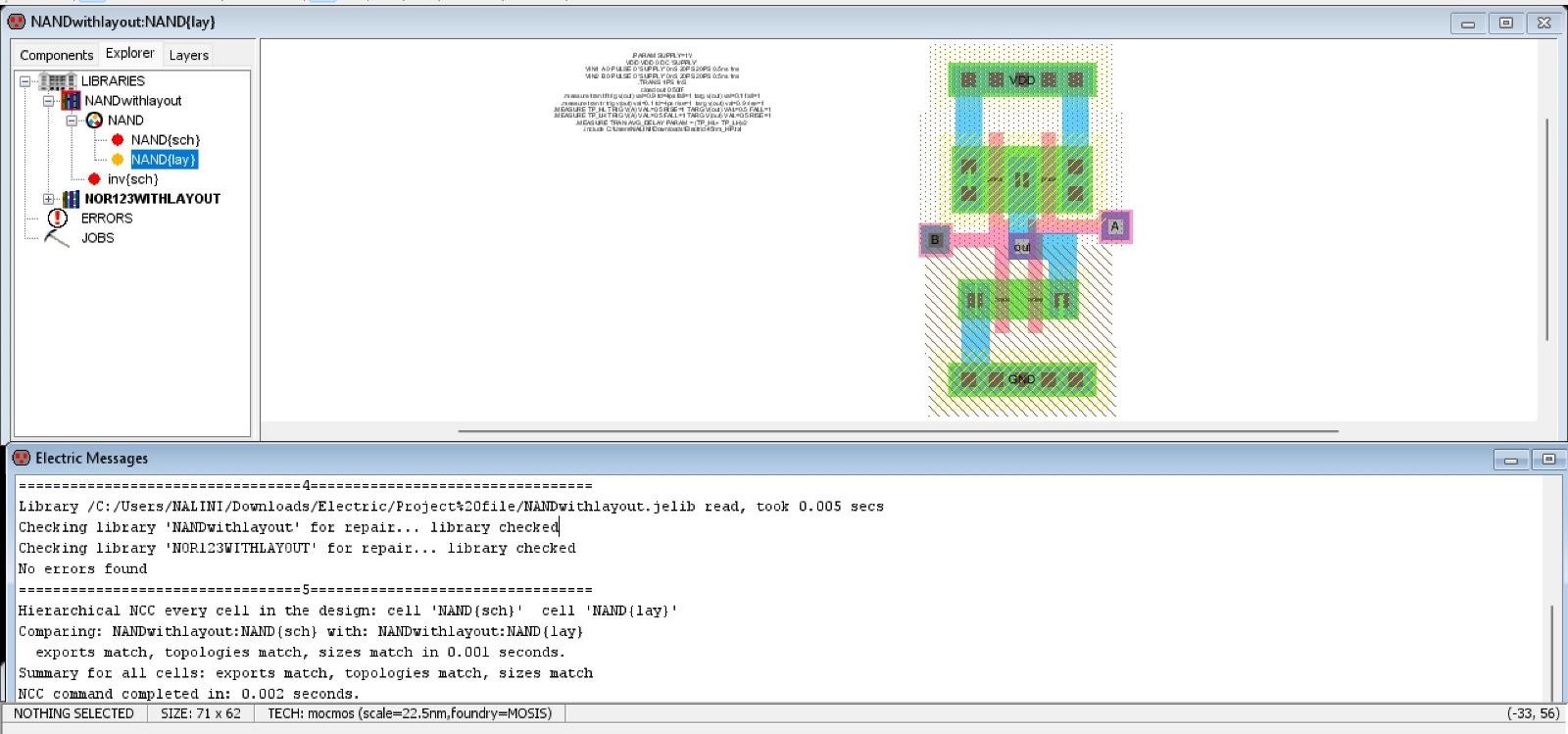


Fig – 3. NAND with LVS log

## Propagation delay-

Table – 1. Propagation delays from schematic

|  |  |  |  |
| --- | --- | --- | --- |
| Load (CL) | tphl | tplh | tp |
| 5 fF | 3.39 x 10-11 | 1.24 x 10-11 | 2.31 x 10-11 |
| 50 fF | 2.94 x 10-10 | 6.18 x 10-11 | 17.79 x 10-11 |

Table – 2. Propagation delays from layout

|  |  |  |  |
| --- | --- | --- | --- |
| Load (CL) | tphl | tplh | tp |
| 5 fF | 4.01 x 10-11 | 1.26 x 10-11 | 2.63 x 10-11 |
| 50 fF | 5.92 x 10-10 | 1.55 x 10-10 | 3.73 x 10-10 |

## Power consumption

Table – 3. Power Consumption

|  |  |  |
| --- | --- | --- |
|  | CL = 5 fF | CL = 50 fF |
| Schematic | -5.88 uW | -40.73 uW |
| Layout | -6.03 uW | -40.82 uW |

## Waveforms-

Input values used for generating waveforms-

VIN1 A 0 PULSE 0 'SUPPLY' 100PS 20PS 20PS 300PS 500PS VIN2 B 0 PULSE 0 'SUPPLY' 640PS 20PS 20PS 200PS 500PS

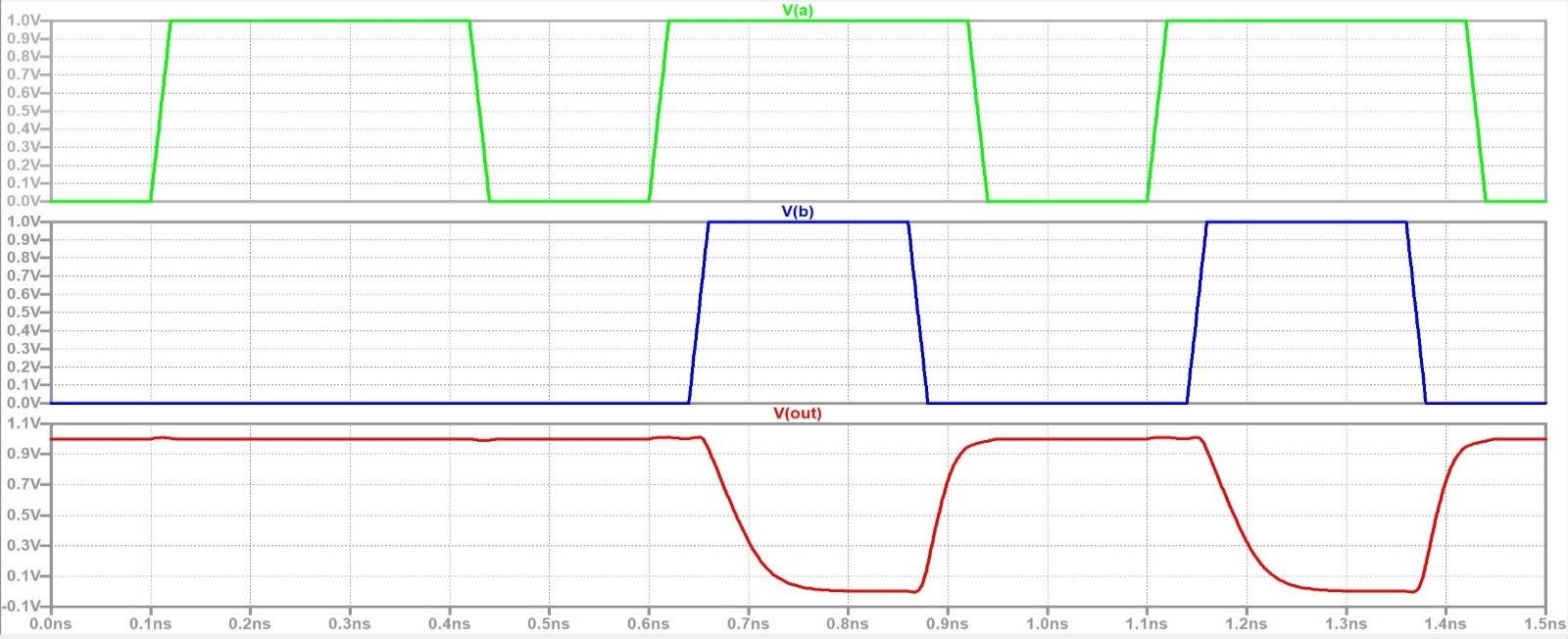


Fig – 4. Waveform from schematic with CL = 5 fF

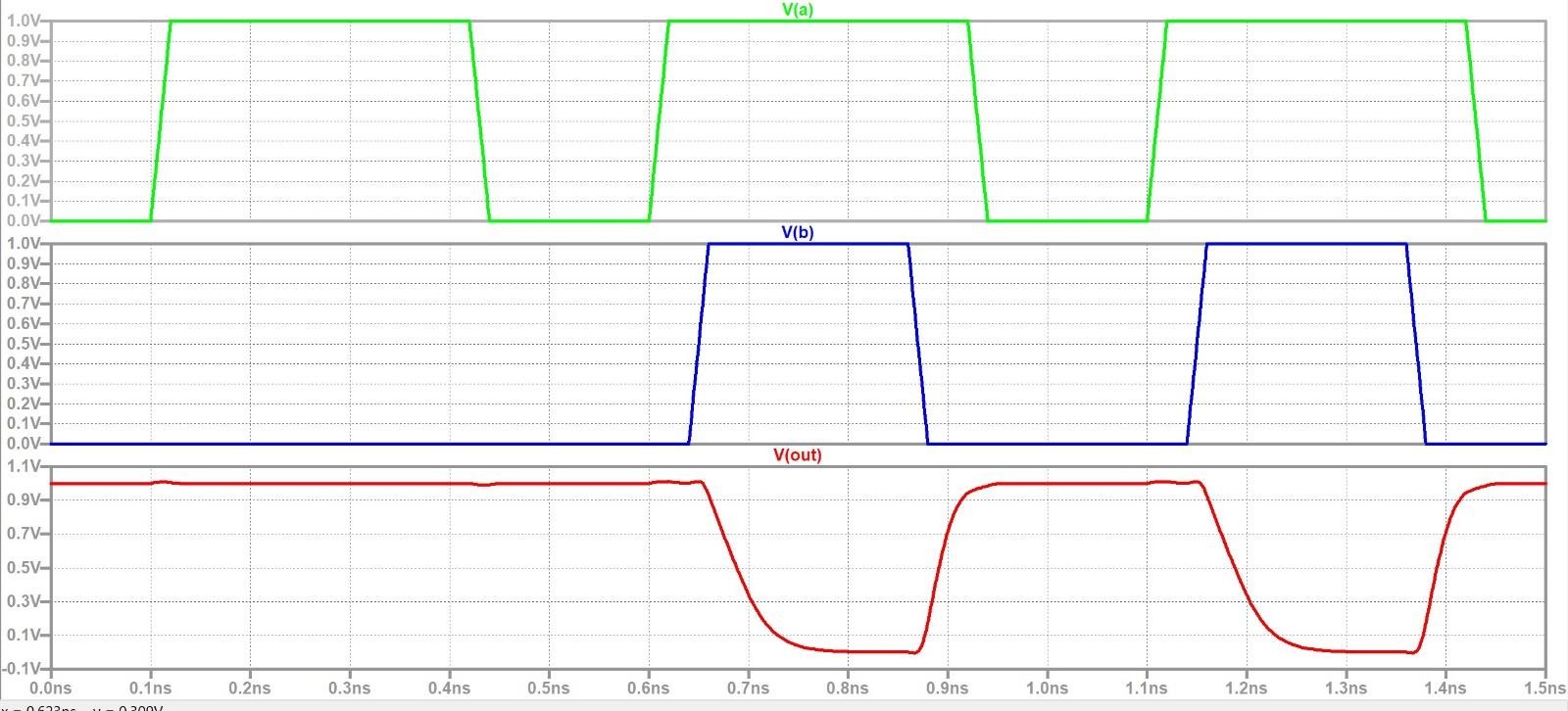


Fig – 5. Waveform from layout with CL = 5 fF

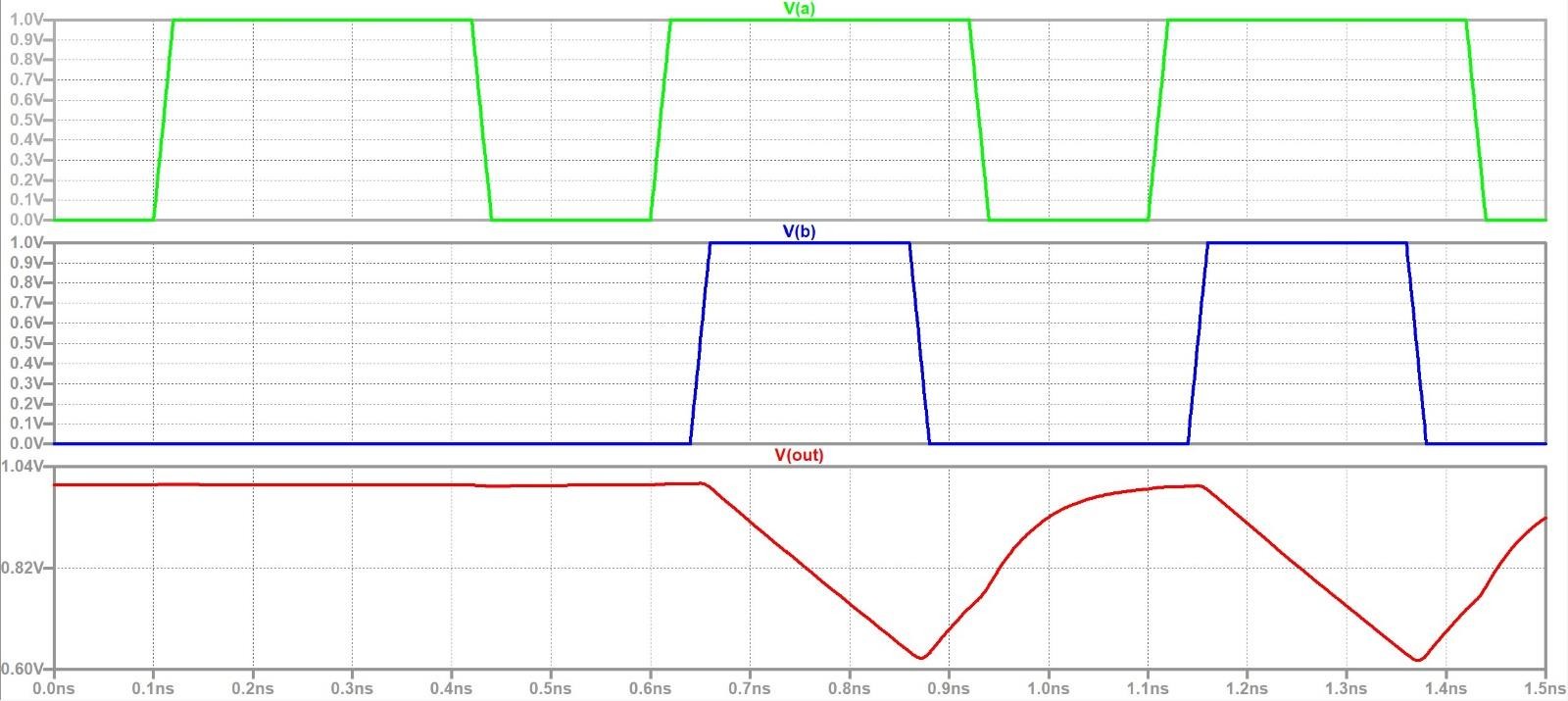


Fig – 6. Waveform from schematic with CL = 50 fF

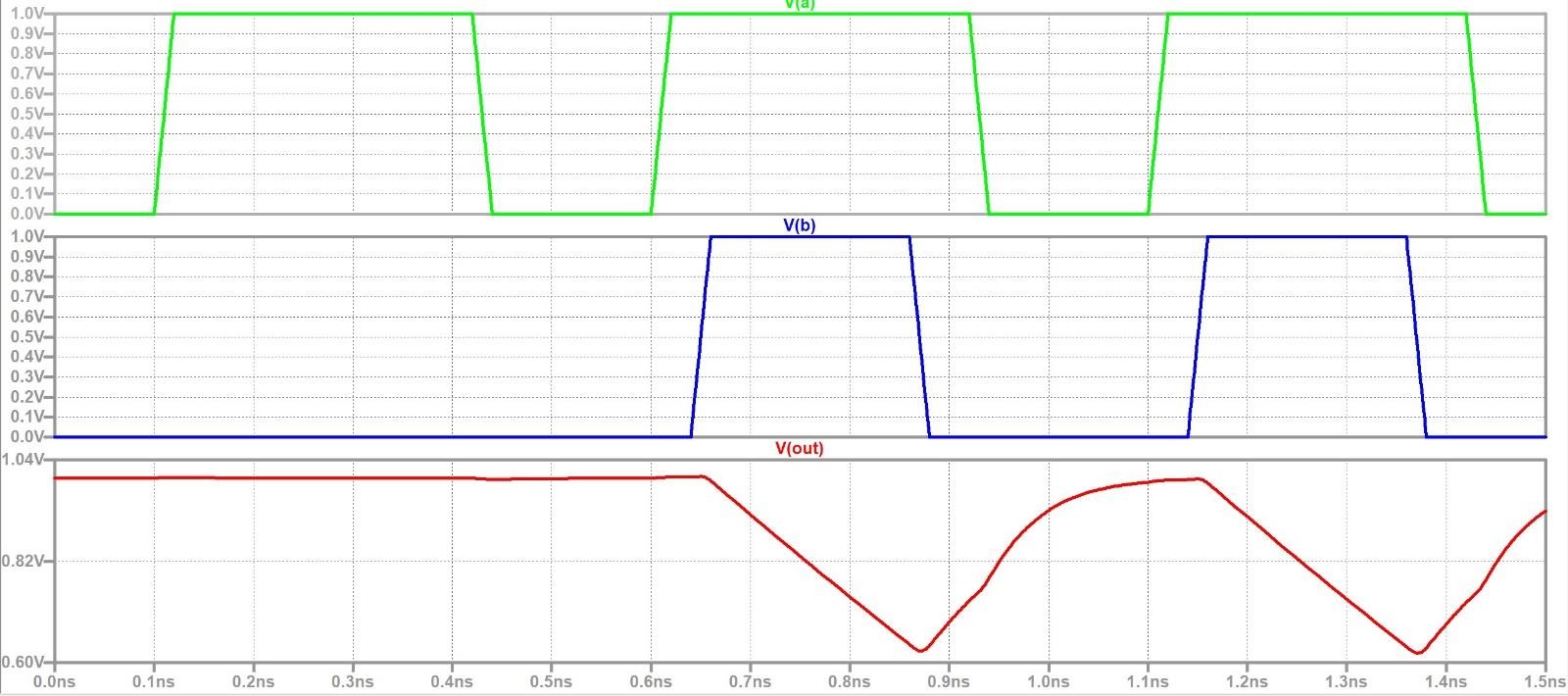


Fig – 7. Waveform from layout with CL = 50 fF