Paper ID (EL114)

DIGITAL LOGIC DESIGN (EL 114)

B.Tech 2nd Semester (2015-16)

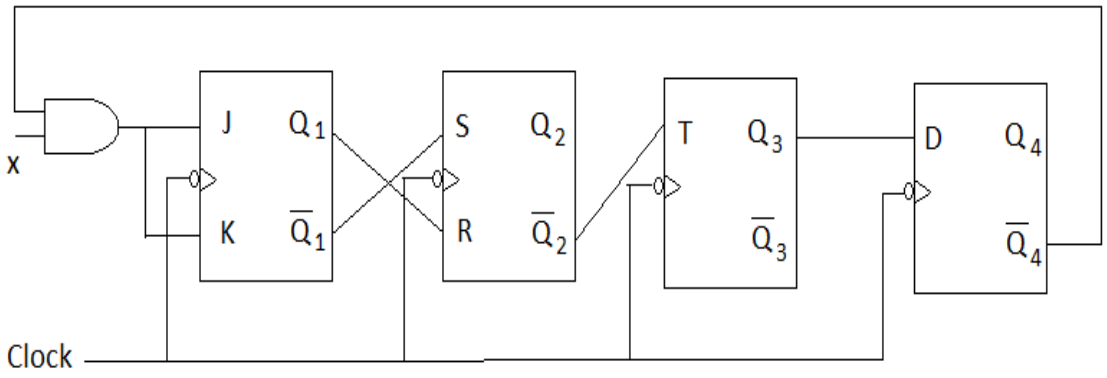
Time: 03 Hours **Maximum Marks: 60**

Answer all the questions.

1. Obtain truth table of a combinational circuit which takes a BCD digit (A,B,C,D) and gives excess-3 codes (E,F,G,H). Assume that all the non-BCD numbers give don't care output. Obtain the simplest PLA implementation of the Boolean functions E,F,G and H which uses minimum number of product terms. (8)

2. Suppose two two-bit numbers, B_1B_0 and A_1A_0, are to be compared. The comparator will have three outputs: B=A, B>A and B<A. Assume that A and B are unsigned positive integers. Design the comparator using a suitable PAL with minimum number of AND gates. (8)

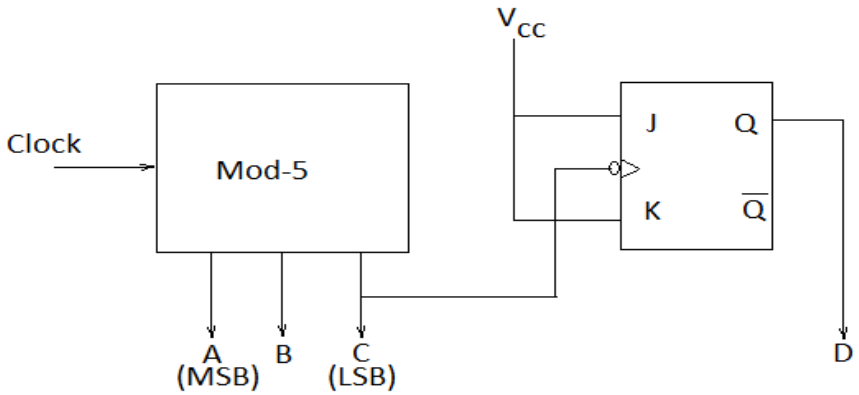
3. For the following figure, draw the timing diagram for the outputs of each flip-flop for the input sequence X= 1 1 0 0 1 0. Assume that all flip-flops are initially 0. (8)



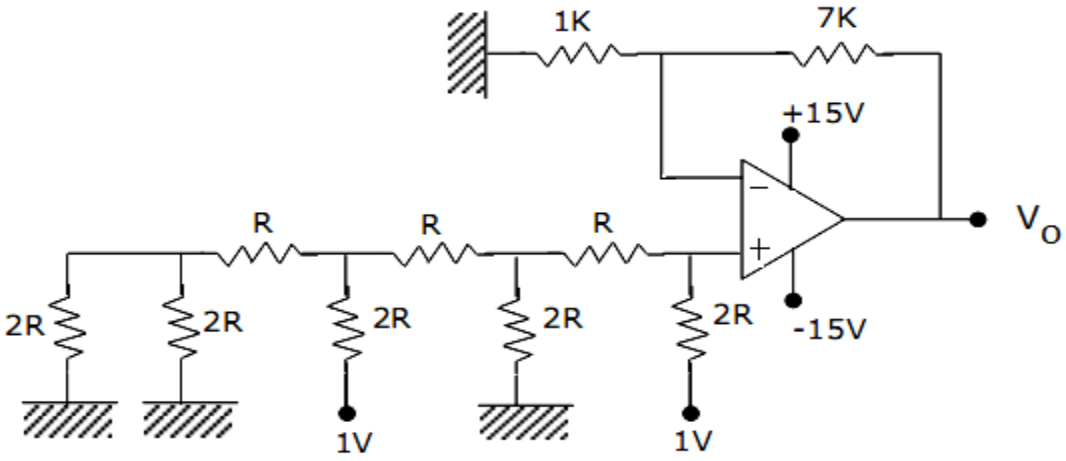
4. Design a counter using T flip-flops for the following repeated binary sequence: 0,3,1,6,4. Assume that counter will return to 0 from all unused states. (8)

5. For the following problem show a state diagram and a state transition table, and then implement the system using D flip-flop.
   Design a Mealy system whose output is 1 iff the last four inputs were 1001. Assume that overlapping is allowed. (8)

6. Consider the following circuit with a binary Mod-5 ripple counter and a JK flip-flop as shown below. Find the modulus of the resulting counter with outputs A,B,C,D and draw the wave forms. (8)



7. A 4-bit R-2R ladder-type DAC with non-inverting amplifier is shown in the figure below. Determine the output voltage V_0. (6)



8. The output of a 3-bit Johnson counter is fed to a D/A converter as shown below. Assume that the outputs of the counter are cleared initially. Draw the waveform of V_0 for a complete count sequence of the Johnson counter. Assume that maximum value of V_0 for $Q_2Q_1Q_0$=111 is 7 volts.

(6)