Chap. 5 INPUT/OUTPUT

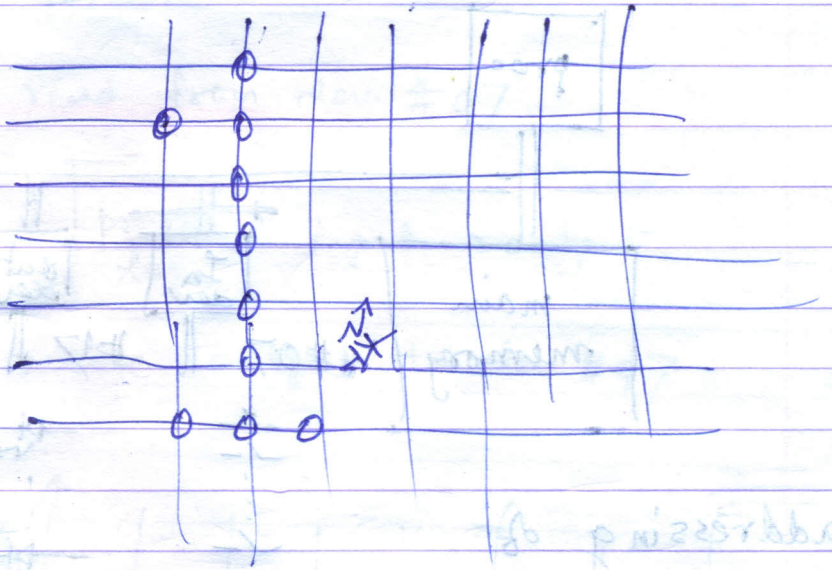
* I/O code - "significant fraction" of the total OS
* no system is complete w/o at least basic I/O

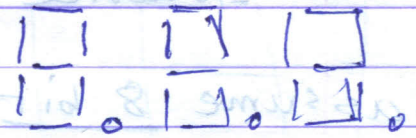
PRINCIPLES OF I/O HARDWARE

- interfaces & "levels of abstraction"
- consider a very simple set-up

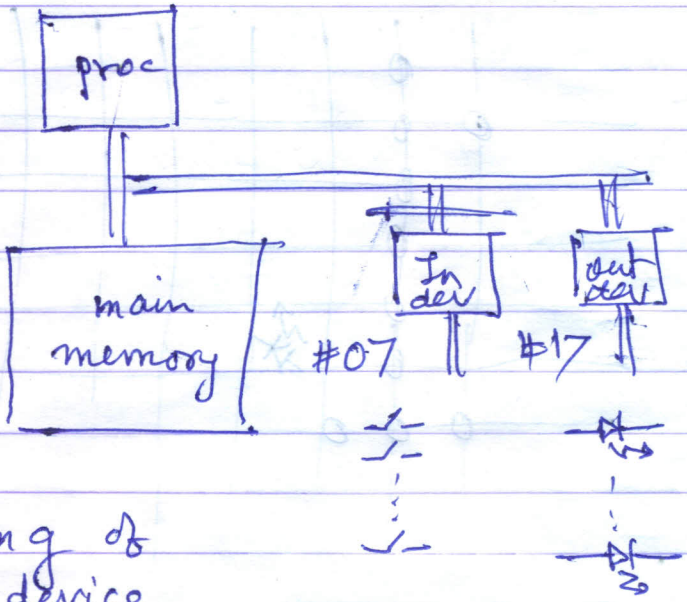
I/O devices block devices vs character devices
see Fig. 5-1 data rate ranges from 10 bytes/sec to 20 GB/sec

- "wait loop" vs. "interrupts"
- "serial" vs. "parallel"
- consider a ~~eee~~ couple of typical I/O devices





7 segment
LED

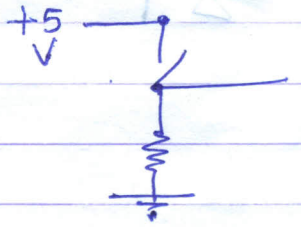


* addressing of I/O device

assume 8 bit I/O addresses

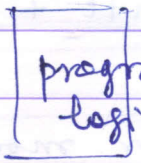
IN dev no., R_i

OUT dev. no., R_j



loop forever

{ read from dev. #07

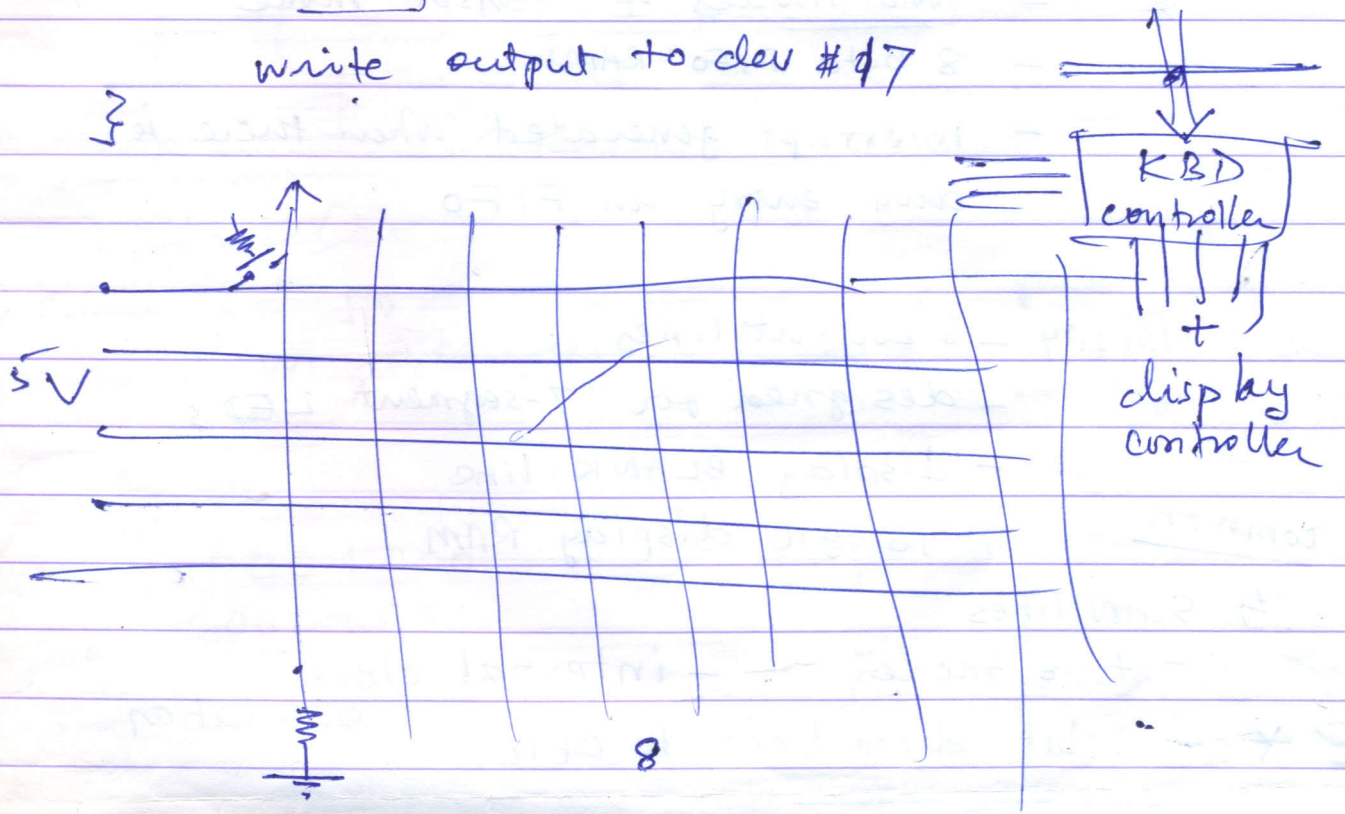


input → output

ASCII

write output to dev #07

}



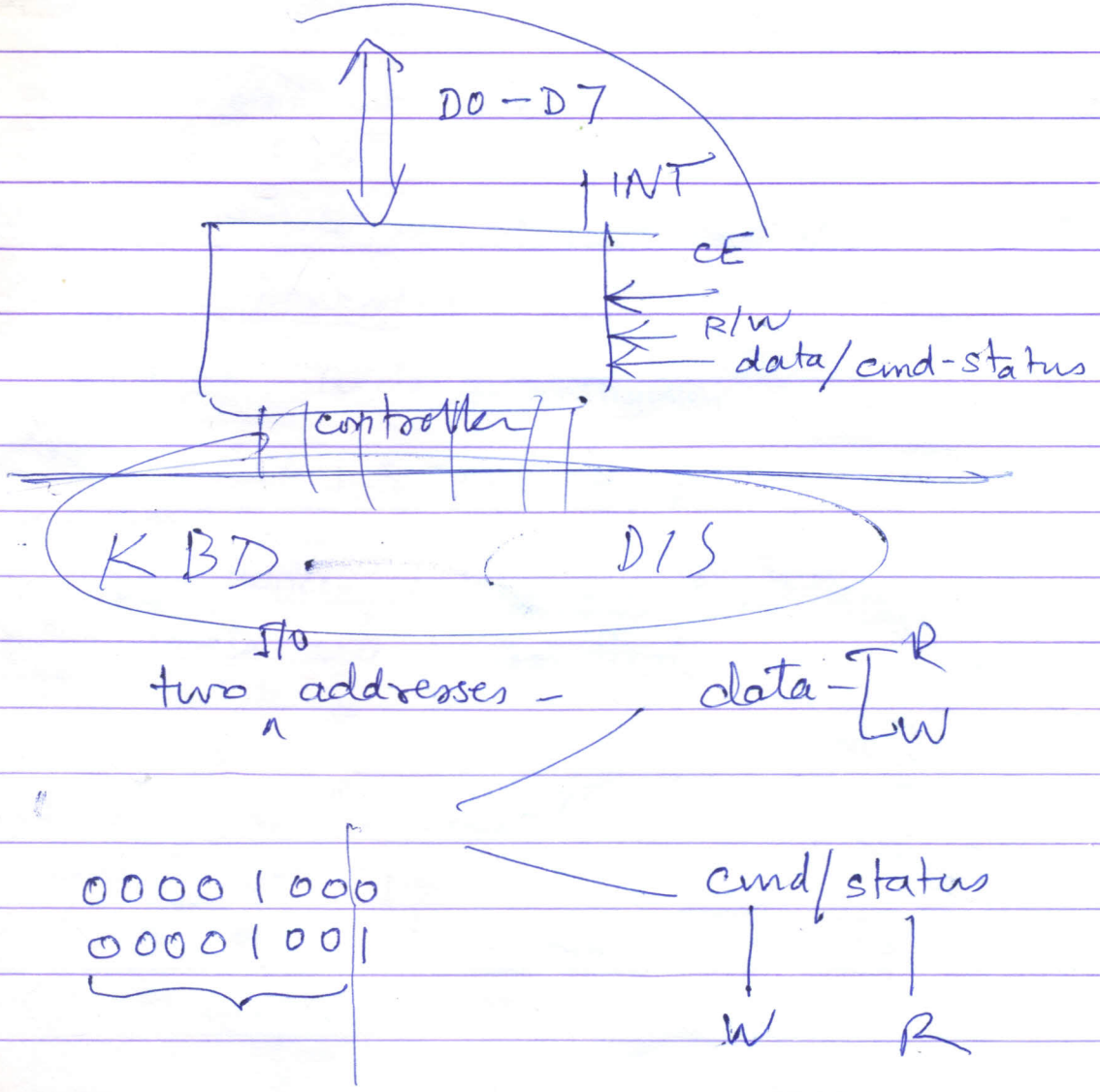
Example of a simple device controller

Intel 8279 Keyboard Display Controller

KBD – 8 return lines + shift + ctrl
- key debouncing
- * two modes + sensor mode
- 8 byte FIFO RAM
- interrupt generated when there is any entry in FIFO

DISPLAY – 8 output lines
- designed for 7-segment LEDs
- display BLANK line
- 16 byte display RAM

common
4 SCAN lines
- two modes
- internal clock generation
- * 8 bit data lines to CPU


D0 - D7
INT
CE
R/W
data/cmd-status
controller
KBD
DIS
I/O
two addresses -
data -
R
W
00001000
00001001
cmd/status
W
R