Paper ID (EL114)

DIGITAL LOGIC DESIGN (EL 114)

B.Tech 2nd Semester (2015-16)

Time: 02 Hours **Maximum Marks: 40**

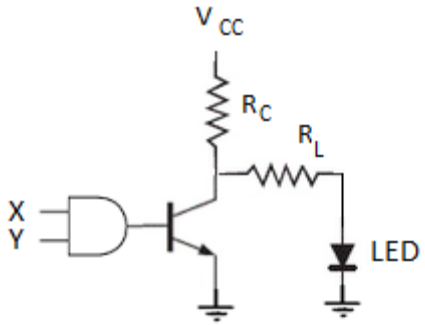
Instructions to the candidates:

a) **Section A is compulsory.**
b) **Answer any two questions from Section B.**

Section A

1. Answer all the questions. (10×2)

i) Consider the following figure. If X=0 and Y=1, then will the LED glow? Justify your answer.



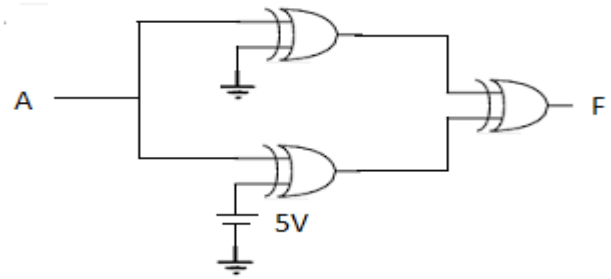
ii) If $Y = A + \bar{B}$ and $Z = \bar{A}.B$, then what is the relation between Y and Z.

iii) If $(X)_{\bar{2}}$ represents 2's complement of X, then prove that $((X)_{\bar{2}})_{\bar{2}} = X$.

iv) Design a digital system to add one with a 4-bit binary number $a_3\ a_2\ a_1\ a_0$ using four half-adders.

v) $\sqrt{121} = 11$ is correct for at least one number system. Determine the possible radices.

vi) What is the expression of the output F for the following figure?



vii) Convert Gray code 100101 to the corresponding binary number.

viii) 1011 is a 5421 BCD number. What is its decimal value?

ix) Convert $(2F.1)_{16}$ to octal.

x) Express the following function into canonical sum-of-products form.

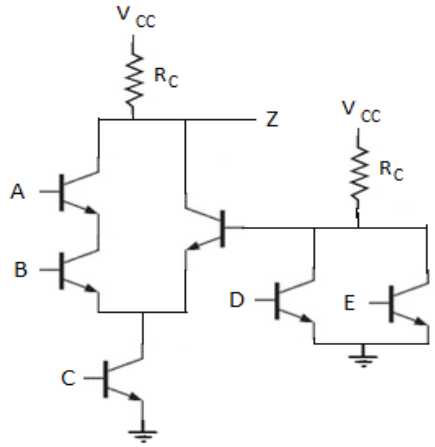
$$F(A, B, C, D) = \bar{A}$$

Section B

2. (5+3+2)

i) Draw and explain the operation of the TTL NAND.

ii) Write a Boolean expression for Z in terms of A, B, C, D and E.



iii) Using theorems of Boolean algebra prove that

$$A.B + A.\bar{B} + \bar{A}.B = A + B$$

3. ((2+2)+4+2)

i) Add the following numbers in binary number system with 2's complement:

a) $(14)_{10}$ + $(-25)_{10}$

b) $(-20)_{10}$ + $(-17)_{10}$

ii) Using a Karnaugh map, write simple sum of products expression for F, where $F = \bar{A}.\bar{D}.B + B.\bar{C}$ and $A.B.C.\bar{D}$ is a don't-care state. Then implement the above function using NAND gates.

iii) Design a combinational circuit with three inputs (A, B, C) and one output F. The output is 1 when A + C = 0 or AC = 1; otherwise the output is 0. Draw a logic diagram using a single logic gate.

4. (5+5)

i) Write the truth table of the binary full adder and simplify it using K-map and realize that using NAND gates.

ii) Design a combinational circuit that accepts a 4-bit binary number and generates the corresponding 4-bit Gray code.