Lab 10

EL 114 Digital Logic Design

Notes:

- In your lab-book, remember to write your steps/methods, and the observations/results
- Get TA's signature after completing each question.

In this Lab you need to familiarize yourself with the Silos simulator tool to write and simulate Verilog codes.

1. Learn use of Silos simulator by writing the Verilog code to simulate a half-adder; where a, b are 1-bit inputs and sum, carry are 1-bit outputs.

2. Write the verilog code for a full-adder, that takes in three 1-bit inputs, a, b and carryin, and gives sum and carryout 1-bit outputs.

3. Write the verilog code for a 4-bits full-adder.