

Lab 6

EL 114 Digital Logic Design

Notes:

- In your lab-book, remember to write your steps/methods, and the observations/results
- Get TA's signature after completing each question.

- All the following questions are to be done in Logisim.
- Make sure you draw each new schematic using "Add circuit" option in the Project menu, so that you can later make use of the instances of that particular schematic/circuit to build larger schematics.

1. Draw schematic of a 4-to-1 MUX with active high ENABLE input.
2. Implement $F(A, B, C, D) = \sum m(1,5,9,10,14,15)$ using 16-to-1 MUX.
3. Implement $F(X, Y, Z) = \sum m(0,3,6,7)$ using 4-to-1 MUX and other necessary gates.
4. Implement $F(X, Y, Z) = \sum m(0,2,3,6,7)$ using 2-to-1 MUX and other necessary gates.
5. Implement $F(A, B, C, D) = \sum m(0,1,3,8,9,11,12)$ using 4-to-1 MUX and other necessary gates.
6. Design 8-to-1 MUX using two 4-to-1 MUXs and one 2-to-1 MUX.
7. Design 1-bit full adder using 1-to-8 deMUX and other necessary gates.
8. Design 1-bit full subtractor using 1-to-8 deMUX and external NOR gates.