Lab 9

EL 114 Digital Logic Design

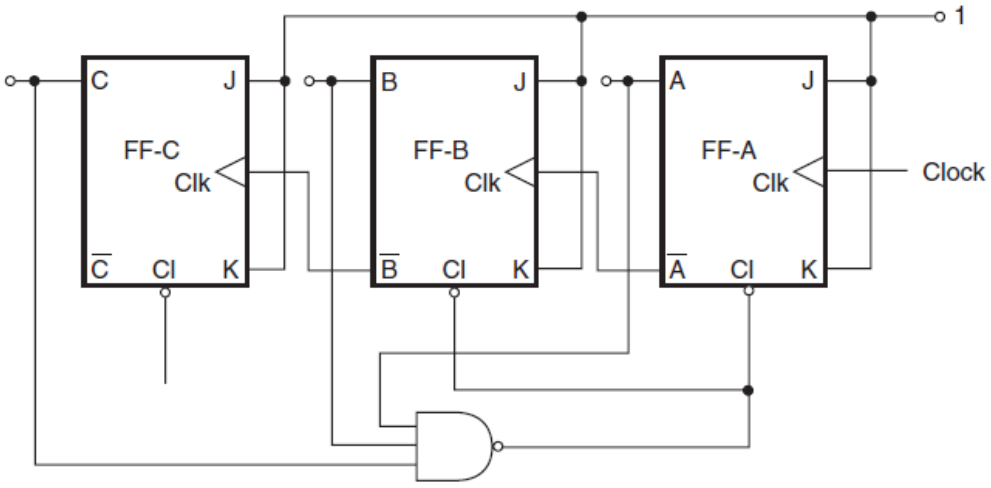
Notes:

- In your lab-book, remember to write your steps/methods, and the observations/results
- Get TA's signature after completing each question.

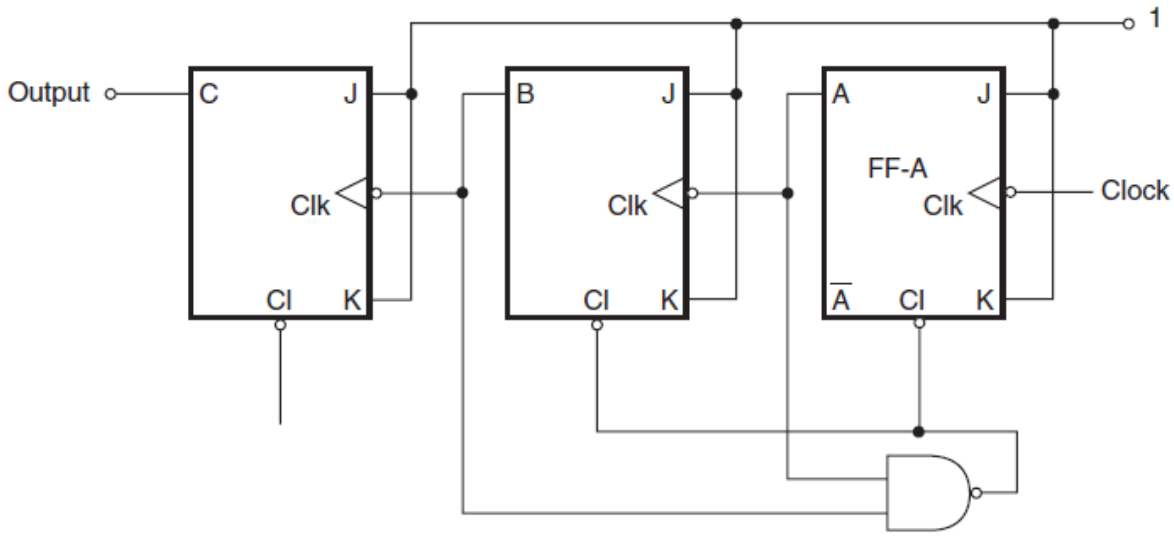
- All the following questions are to be done in Logisim.
- Make sure you draw each new schematic using "Add circuit" option in the Project menu, so that you can later make use of the instances of that particular schematic/circuit to build larger schematics.

1. Design clocked S-R, J-K, D and T flip-flops using NAND gates and write their corresponding truth tables.
2. Determine the count sequences of the following counters.

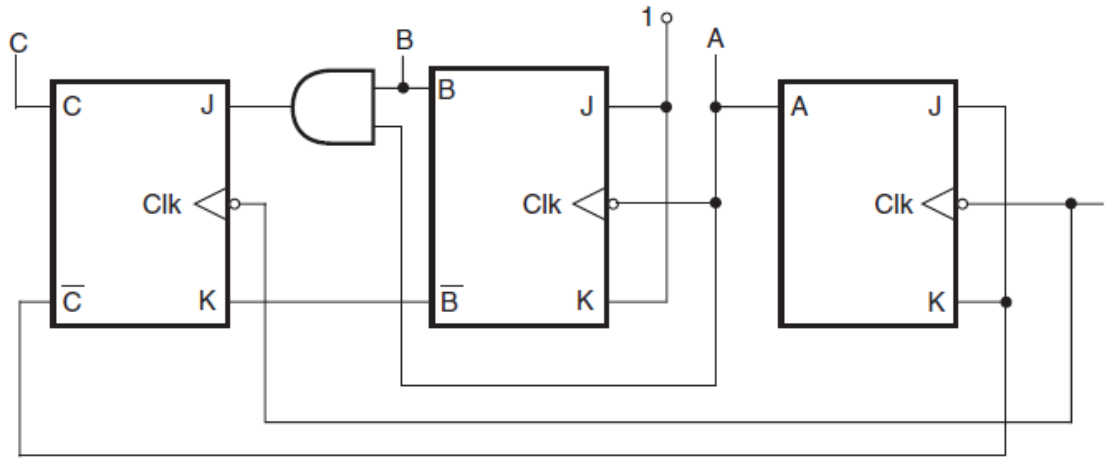
   a) For the following figure, write the sequence of the output states observed on C (MSB), B and A starting with all the flip-flops cleared.



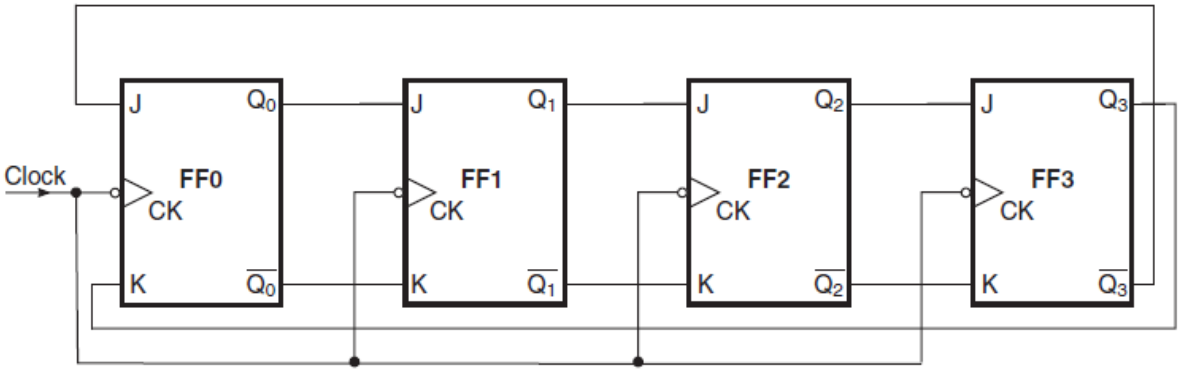
b) For the following figure, write the sequence of the output states observed on C (MSB), B and A starting with all the flip-flops cleared.



c) For the following figure, write the sequence of the output states observed on C (MSB), B and A starting with all the flip-flops cleared.



d) For the following figure, write the sequence of the output states observed on Q_3 (MSB), Q_2, Q_1 and Q_0 starting with all the flip-flops cleared.



e) For the following figure, write the sequence of the output states observed on C (MSB), B and A starting with all the flip-flops cleared.