Introduction to Digital Design
SAMPLE FINAL EXAM
– closed books and notes –
(8 problems, 180 minutes)
PLEASE BE SYSTEMATIC, ORGANIZED, and NEAT:
– this will be considered in the grading.

Name: ____________________

Problem	Points	Score
1	10	
2	8	
3	10	
4	14	
5	10	
6	8	
7	10	
8	10	
Total	80	

Problem 1. (10 points)

a) Give a state diagram and state/output table of a Mealy machine which implements the following behavior:

$$z(t) = \begin{cases} x'(t) & \text{if } x(t) = 0 \text{ and } x(k) = 0 \text{ for all } k < t \\ 0 & \text{if } x(t) = 1 \text{ and } x(k) = 0 \text{ for all } k < t \\ x(t) & \text{otherwise} \end{cases} \tag{1}$$

b) Illustrate the time behavior for the input sequence shown bellow. Assume that $x(k) = 0$ for $k < 0$.

t	0	1	2	3	4	5	6
$x(t)$	0	0	1	0	1	1	0
$z(t)$							

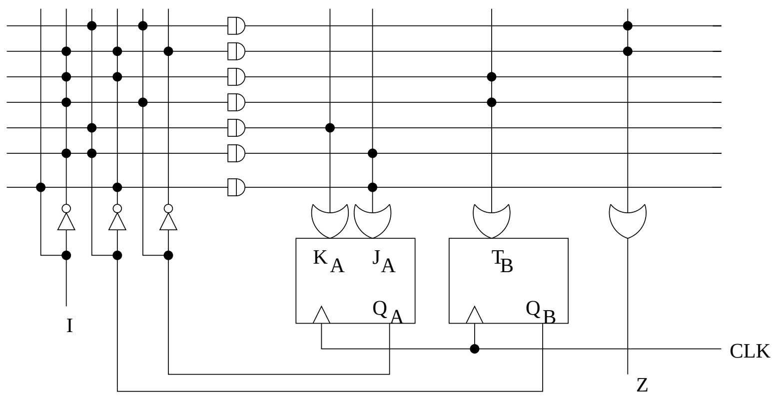
c) Is this a finite-memory system? Explain your answer.

Problem 2. (8 points)

Find an equivalent finite state machine with a minimum number of states. Show all partitions and the minimal state table.

PS	$x = 0$	$x = 1$
A	E,0	C,0
B	C,0	A,0
C	B,0	G,0
D	G,0	A,0
E	F,1	B,0
F	E,0	D,0
G	D,0	G,0

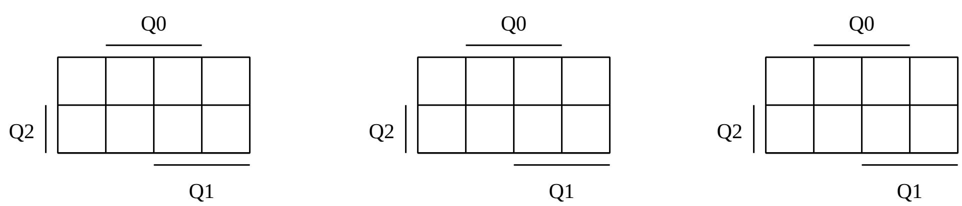
Problem 3. (10 points) Derive the state transition/output table for the implementation of the finite state machine shown in the figure below. The next state and output functions are implemented by a PLA structure. The machine has one input I and one output Z. Show expressions for the flip-flop inputs.



PS($Q_A Q_B$)	I	J_A	K_A	T_B	NS	Z

Problem 4. (14 points) (a) Design a cyclic counter with the output sequence $0, 1, 3, 7, 6, 4, 0, 1, \ldots$ (of period 6) using JK flip-flops and AND, OR, NOT gates if needed. Assume that the input $x = 1$ always. Select a state assignment that is the same as the coding for the output, that is $z(t) = s(t)$. Show the state/output table. Minimize all expressions. Show the logic diagram of the counter.

State/output table:



$J_0 =$________________________

$K_0 =$________________________

$J_1 =$________________________

$K_1 =$________________________

$J_2 =$________________________

$K_2 =$________________________

Problem 4 (cont.) (b) Design the cyclic counter defined in part (a) using the "one flip-flop per state" approach with D flip-flops. To obtain the output, use a 8-input binary encoder. Show all connections. How is the counter initialized?

Problem 5. (10 points) Design a combinational network that finds the largest and the second largest of four nonnegative integers A, B, C, D. Each integer is represented by four bits. You may use only the following module types: 4×2-input multiplexer and four-bit comparator. The two-bit output of the comparator is $z = (z_1, z_0)$. If the first integer is larger than the second, the output is $z = 10$. If the second number is larger, the output is $z = 01$ and if the numbers are equal, the output is $z = 00$). Indicate all inputs and connections on the modules being used.

Problem 6. (8 points)

a) Complete the following table assuming true-and-complement number systems. If there is a problem in completing the table, explain. All implicit and explicit values are given in the decimal number system.

Number system	Number of digits n	Signed integer x	Representation value x_R	Digit-vector X
2's compl.	7	-39		
1s' compl.	8		167	
2's compl.				100100100
2's compl.	6	-43		

b) Compute $z = a + 2b - c$ in 2's complement for $a = -7$, $b = 12$, and $c = -97$. Perform calculations on bit-vectors representing a, b and c and show every step of your work. How many bits should z have to represent the correct result? Check your work by showing, for each step, the corresponding values in decimal number system.

Problem 7. (10 points)

a) Design a 4-bit by 2-bit multiplier module M42. The operands are positive: the multiplicand is $X = (x_3, x_2, x_1, x_0)$, the multiplier is $Y = (y_1, y_0)$, and the product $p = (p_5, ..., p_0)$. You are allowed to use AND gates, full-adders (FA) and half-adders (HA) only.

b) Using two M42 modules from part a), and extra full-adders (FA) and half-adders (HA), design a 4 by 4 multiplier. Show clearly all modules and connections. Label the inputs and outputs assuming $X = (x_3, x_2, x_1, x_0)$ and $Y = (y_3, y_2, y_1, y_0)$ as inputs and Z bit-vector as the output. Make the design as fast and simple as possible.

c) Determine the critical path in the 4 by 4 multiplier and its delay. Assume that the low to high and high to low propagation delays are the same. For AND gate, the delay is t_g. The sum and carry-out delays of the full-adder are $t_s = t_c = t_f$ and of the half-adder t_h.

Problem 8. (10 points)

Design a sequential system specified by the following state transition and output table using a modulo-8 counter with parallel load as the state register, a 8-to-1 multiplexer for the CNT input and NAND gates. Assume LD = CNT'. The design must take advantage of the count and parallel mode capabilities of the counter. Show all your work.

PS $Q_2Q_1Q_0$	Input $x = 0$	Input $x = 1$
000	000,0	001,0
001	000,0	010,0
010	000,0	011,0
011	100,0	011,0
100	101,0	001,0
101	000,1	001,0
	NS, z	NS, z