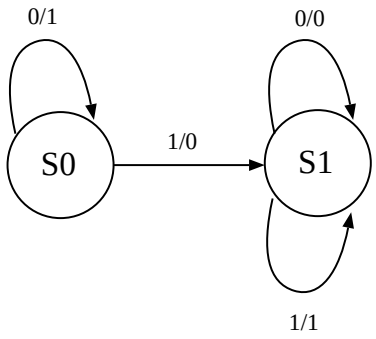
Introduction to Digital Design
SAMPLE FINAL EXAM
- Solutions –

Problem 1. (10 points)

a) Give a state diagram and state/output table of a Mealy machine which implements the following behavior:

$$z(t) = \begin{cases} x'(t) & \text{if } x(t) = 0 \text{ and } x(k) = 0 \text{ for all } k < t \\ 0 & \text{if } x(t) = 1 \text{ and } x(k) = 0 \text{ for all } k < t \\ x(t) & \text{otherwise} \end{cases} \quad (1)$$



PS	x=0	x=1
S0	S0,1	S1,0
S1	S1,0	S1,1
	NS,z	

b) Illustrate the time behavior for the input sequence shown bellow. Assume that $x(k) = 0$ for $k < 0$.

t	0	1	2	3	4	5	6
$x(t)$	0	0	1	0	1	1	0
$z(t)$	1	1	0	0	1	1	0

c) Is this a finite-memory system? Explain your answer.

No; the output cannot be determined from the last m inputs for any fixed integer m.

Problem 2. (8 points)

Find an equivalent finite state machine with a minimum number of states. Show all partitions and the minimal state table.

PS	$x = 0$	$x = 1$
A	E,0	C,0
B	C,0	A,0
C	B,0	G,0
D	G,0	A,0
E	F,1	B,0
F	E,0	D,0
G	D,0	G,0

The partitions are:

P1 = (A B C D F G)(E)

P2 = (A F)(B C D G)(E)

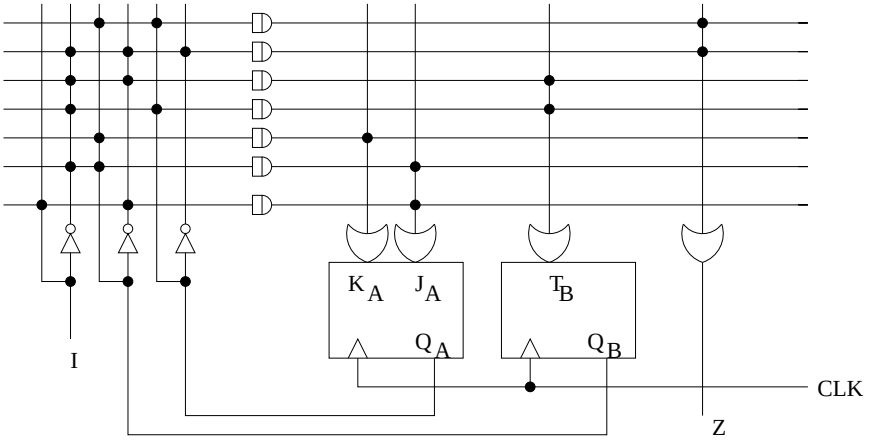
P3 = (A F)(B D)(C G)(E)

P4 = (A)(F)(B D)(C G)(E) = P5

The minimal state table is:

PS	$x = 0$	$x = 1$
A	E,0	C,0
B	C,0	A,0
C	B,0	C,0
E	F,1	B,0
F	E,0	B,0

Problem 3. (10 points) Derive the state transition/output table for the implementation of the finite state machine shown in the figure below. The next state and output functions are implemented by a PLA structure. The machine has one input I and one output Z. Show expressions for the flip-flop inputs.



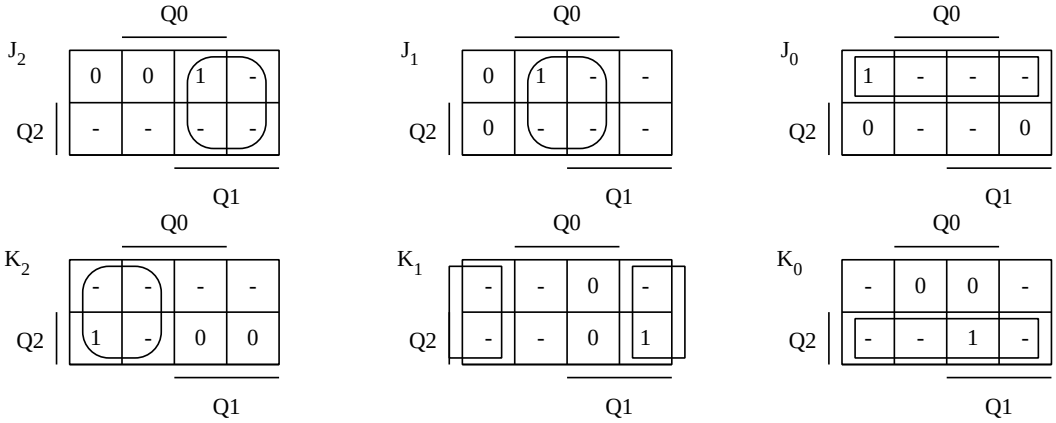
$$
\begin{aligned}
J_A &= Q_B I' + Q'_B I \\
K_A &= Q_B \\
T_B &= Q'_B I' + Q_A I' \\
Z &= Q_A Q_B + Q'_A Q'_B I'
\end{aligned}
$$

PS($Q_A Q_B$)	I	J_A	K_A	T_B	NS	Z
00	0	0	0	1	01	1
00	1	1	0	0	10	0
01	0	1	1	0	11	0
01	1	0	1	0	01	0
10	0	0	0	1	11	0
10	1	1	0	0	10	0
11	0	1	1	1	00	1
11	1	0	1	0	01	1

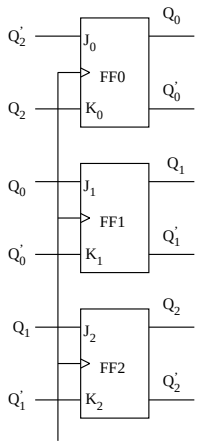
Problem 4. (14 points) (a) Design a cyclic counter with the output sequence $0, 1, 3, 7, 6, 4, 0, 1, \ldots$ (of period 6) using JK flip-flops and AND, OR, NOT gates if needed. Assume that the input $x = 1$ always. Select a state assignment that is the same as the coding for the output, that is $z(t) = s(t)$. Show the state/output table. Minimize all expressions. Show the logic diagram of the counter.

State/output table:

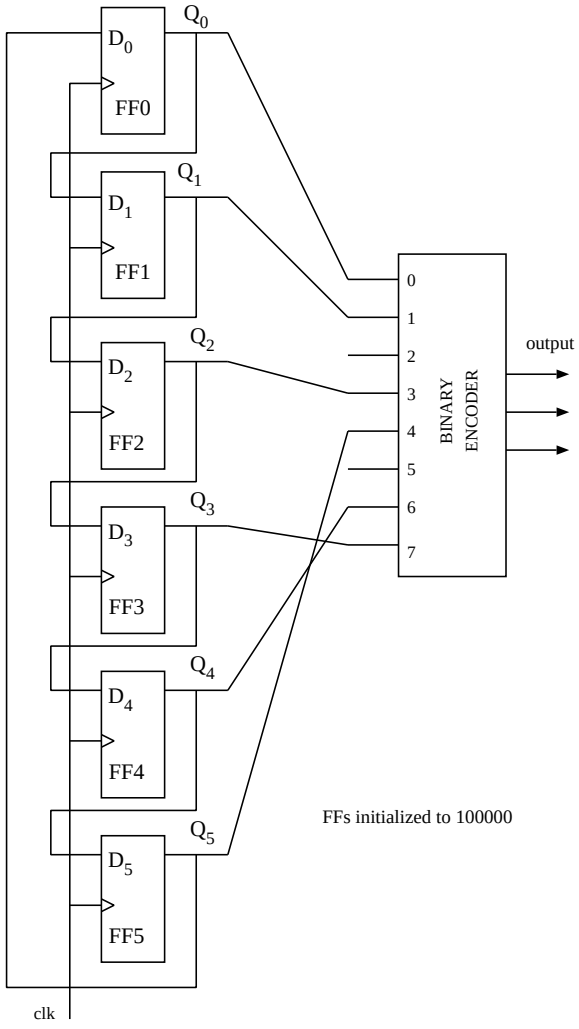
PS	NS	J_2K_2	J_1K_1	J_0K_0
000	001	0-	0-	1-
001	011	0-	1-	-0
010	—	–	–	–
011	111	1-	-0	-0
100	000	-1	0-	0-
101	—	–	–	–
110	100	-0	-1	0-
111	110	-0	-0	-1



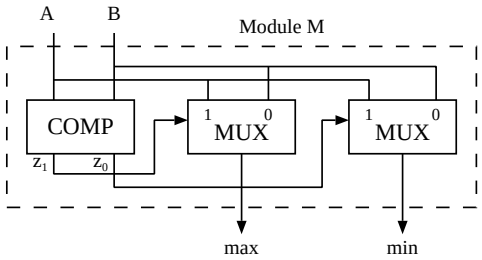
$J_0 = Q_2'\ K_0 = Q_2\ J_1 = Q_0\ K_1 = Q_0'\ J_2 = Q_1\ K_2 = Q_1'$

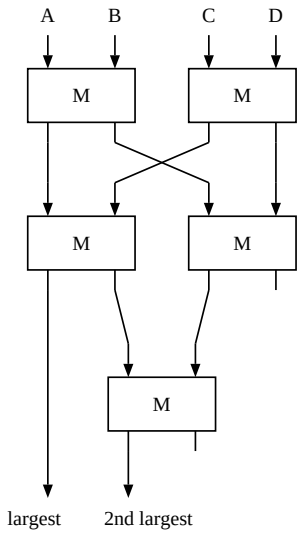


Problem 4 (cont.) (b) Design the cyclic counter defined in part (a) using the "one flip-flop per state" approach with D flip-flops. To obtain the output, use a 8-input binary encoder. Show all connections. How is the counter initialized?


D0
FF0
Q0
D1
FF1
Q1
D2
FF2
Q2
D3
FF3
Q3
D4
FF4
Q4
D5
FF5
Q5
clk
0
1
2
3
4
5
6
7
BINARY
ENCODER
output
FFs initialized to 100000

Problem 5. (10 points) Design a combinational network that finds the largest and the second largest of four nonnegative integers A, B, C, D. Each integer is represented by four bits. You may use only the following module types: 4×2-input multiplexer and four-bit comparator. The two-bit output of the comparator is $z = (z_1, z_0)$. If the first integer is larger than the second, the output is $z = 10$. If the second number is larger, the output is $z = 01$ and if the numbers are equal, the output is $z = 00$). Indicate all inputs and connections on the modules being used.





Problem 6. (8 points)

a) Complete the following table assuming true-and-complement number systems. If there is a problem in completing the table, explain. All implicit and explicit values are given in the decimal number system.

Number system	Number of digits n	Signed integer x	Representation value x_R	Digit-vector X
2's compl.	7	-39	89	1011001
1s' compl.	8	-89	167	10100111
2's compl.	9	-220	292	100100100
2's compl.	6	-43	NA	NA

b) Compute $z = a + 2b - c$ in 2's complement for $a = -7$, $b = 12$, and $c = -97$. Perform calculations on bit-vectors representing a, b and c and show every step of your work. How many bits should z have to represent the correct result? Check your work by showing, for each step, the corresponding values in decimal number system.

a =	111001	(-7)
b =	001100	(12)
2b=	011000	(24)
c =	10011111	(-97)
a+2b =	010001	(17)
z=a+2b-c =	01110010	(114)

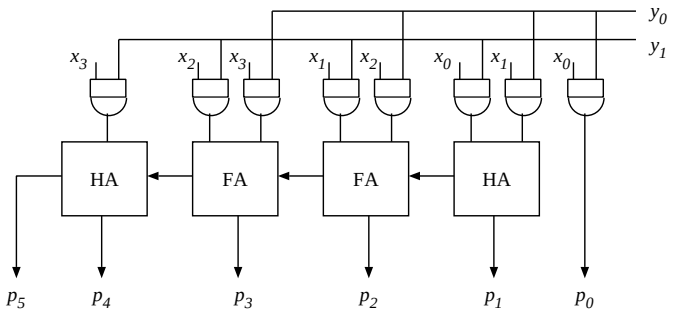
The result z has 8 bits.

Problem 7. (10 points)

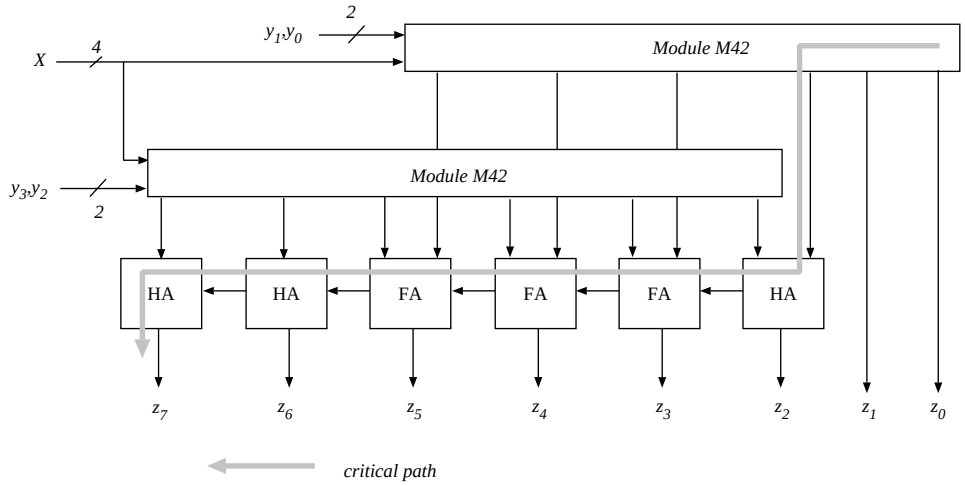
a) Design a 4-bit by 2-bit multiplier module M42. The operands are positive: the multiplicand is $X = (x_3, x_2, x_1, x_0)$, the multiplier is $Y = (y_1, y_0)$, and the product $p = (p_5, ..., p_0)$. You are allowed to use AND gates, full-adders (FA) and half-adders (HA) only.

		x_3	x_2	x_1	x_0
				y_1	y_0
		x_3y_0	x_2y_0	x_1y_0	x_0y_0
	x_3y_1	x_2y_1	x_1y_1	x_0y_1	
p_5	p_4	p_3	p_2	p_1	p_0

Module M42:



b) Using two M42 modules from part a), and extra full-adders (FA) and half-adders (HA), design a 4 by 4 multiplier. Show clearly all modules and connections. Label the inputs and outputs assuming $X = (x_3, x_2, x_1, x_0)$ and $Y = (y_3, y_2, y_1, y_0)$ as inputs and Z bit-vector as the output. Make the design as fast and simple as possible.



c) Determine the critical path in the 4 by 4 multiplier and its delay. Assume that the low to high and high to low propagation delays are the same. For AND gate, the delay is t_g. The sum and carry-out delays of the full-adder are $t_s = t_c = t_f$ and of the half-adder t_h.

$T_{critical_path} = t_g + 4t_h + 4t_f$

Problem 8. (10 points)

Design a sequential system specified by the following state transition and output table using a modulo-8 counter with parallel load as the state register, a 8-to-1 multiplexer for the CNT input and NAND gates. Assume LD = CNT'. The design must take advantage of the count and parallel mode capabilities of the counter. Show all your work.

	PS	Input	Input
	$Q_2Q_1Q_0$	$x=0$	$x=1$
S_0	000	000,0	001,0
S_1	001	000,0	010,0
S_2	010	000,0	011,0
S_3	011	100,0	011,0
S_4	100	101,0	001,0
S_5	101	000,1	001,0
		NS, z	NS, z

don't care counter states: S_6 and S_7

$CNT = S_0x + S_1x + S_2x + S_3x' + S_4x' \quad LD = CNT'$

$I_2I_1I_0$

000 if $S_1x' + S_5x' + S_0x'$

001 if $S_4x + S_5x$

011 if S_3x

$I_2 = 0 \quad I_1 = S_3x = Q_1Q_0x \quad I_0 = (Q_2 + Q_1Q_0)x \quad z = Q_2Q_0x'$