Lab 4

EL 114 Digital Logic Design

Notes:

- In your lab-book, remember to write your steps/methods, and the observations/results
- Get TA's signature after completing each question.

- All the following questions are to be done in logisim.
- Make sure you draw each new schematic using "Add circuit" option in the Project menu, so that you can later make use of the instances of that particular schematic/circuit to build larger schematics.

1. Use K-map and draw a minimum two-level circuit (corresponding to sum of products expressions) with AND gates and one OR gate for each of the following functions. Again, implement the same function with only NAND gates. Verify your circuits with truth tables.

   a) $F(A,B,C,D) = \sum m(0,3,4,5,7,8,12,13,15)$
   b) $F(A,B,C,D) = \sum m(6,9,11,12,14) + \sum d(0,1,2,4,8)$

2. Use K-map and draw a minimum two-level circuit (corresponding to product of sums expressions) with OR gates and one AND gate for each of the following functions. Again, implement the same function with only NOR gates. Verify your circuits with truth tables.

   a) $F(A,B,C,D) = \sum m(1,3,4,6,9,11,12,14)$
   b) $F(A,B,C,D) = \sum m(5,6,11) + \sum d(0,1,2,4,8,15)$

3. a) Draw the gate-level schematic for a Half-adder .
   b) Draw the schematic for a Full-adder using the instances of the above Half-adder, and other necessary gates.

4. Design the XOR and XNOR gates with only NAND gates. Again design the same (i.e., the XOR and XNOR gates) with only NOR gates.