SHIVANI BATHLA

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RESEARCH INTERESTS

Hardware accelerators, Deep learning, Large Language Models, Optimization, Automated reasoning, Constraint satisfaction, Sampling and belief propagation based algorithms, Ising models, Causal inference, Graph representation learning

EDUCATION

Ph.D. in Electrical Engineering — Jul 2017 – May 2024
Indian Institute of Technology Madras — Chennai, India
GPA: 9.6/10
Thesis: Approximate Bayesian inference in probabilistic graphical models
Advisor: Prof. Vinita Vasudevan

M.S. (by Research) in Electrical Engineering — Jul 2014 – Jun 2017
Indian Institute of Technology Madras — Chennai, India
GPA: 9.4/10
Thesis: Reduction of glitch power dissipation in digital circuits
Advisor: Prof. Nitin Chandrachoodan, Dr. Rahul M Rao

B.E. (Hons.) in Electronics & Instrumentation — Aug 2007 – Jul 2011
Birla Institute Of Technology & Science, Pilani — Pilani, India
GPA: 9.1/10

RESEARCH PROJECTS

Approximate Bayesian inference in probabilistic graphical models

- Developed a novel framework (*IBIA*) for approximate inference in probabilistic graphical models like Bayesian networks, Markov random fields and factor graphs. These models are fundamental tools in probabilistic machine learning that allow for systemic modeling of uncertainty, causality and domain knowledge of complex systems.
- Designed algorithms for inference of three widely used probabilistic reasoning queries (a) partition function, (b) posterior marginals, and (c) maximum a-posteriori assignment.
- Evaluated and compared results with several other variational methods and sampling-based methods implemented in solvers like libDAI, Merlin, SampleSearch, PGMax, SMILE, and optimization frameworks like Toulbar, and Gurobi.
- Evaluation over benchmarks from multiple domains including computer vision tasks like image segmentation and object detection, pedigree analysis, medical diagnosis, and weighted constraint satisfaction problems. The proposed framework gives state-of-the-art accuracy with competitive runtimes.

Probabilistic graphical models for solving discrete optimization problems — Ongoing

- Formulation of graphical models for problems like finding the maximum cut of a weighted graph and minimum cost Steiner trees, and models for Boolean satisfiability problem (SAT) and for counting the number of satisfying solutions.
- Evaluation and analysis of the performance of different inference techniques with existing solvers.

Estimation of circuit design metrics using Bayesian inference techniques

- Developed Bayesian network models for computation of circuit design metrics used for dynamic power estimation, circuit reliability analysis, and error analysis in probabilistic circuits. Fast and accurate computation of these metrics is needed within optimization frameworks to get designs with improved performance.
- Evaluated performance of proposed models with different inference methods showing improved accuracy and speedup.

Simulation based model for estimation and reduction of glitch power dissipation in digital circuits

- Glitches are unwanted/spurious transitions that do not impact circuit functionality but contribute to power dissipation.
- Developed an algorithm for the identification of generated and propagated glitches during event-driven logic simulation.
- Designed heuristics to measure the contribution of each signal in the circuit to the total glitch power dissipation. These metrics help predict portions of the design where reduction techniques likely to yield maximum benefit.
- Developed and implemented algorithms for glitch power reduction guided by proposed metrics.
- Demonstrated that the proposed metrics give lower power solutions than existing ones.

PUBLICATIONS

- **S. Bathla** and V. Vasudevan, "Approximate inference of marginals using the IBIA framework," in *Conference on Neural Information Processing Systems (**NeurIPS**)*, 2023.
- **S. Bathla** and V. Vasudevan, "IBIA: An incremental build-infer-approximate framework for approximate inference of partition function," *Transactions on Machine Learning Research (**TMLR**), 2023. Selected for presentation at Symposium of Advances in Approximate Bayesian Inference (**AABI**)*, 2024.
- **S. Bathla** and V. Vasudevan, "A framework for reliability analysis of combinational circuits using approximate Bayesian inference," *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, 2023.
- **S. Bathla**, R. M. Rao, and N. Chandrachoodan, "A simulation-based metric to guide glitch power reduction in digital circuits," *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, 2018.
- V. Devanathan, H. Ellur, M. Imran, and **S. Bathla**, "Hierarchical, physical-aware, built-in self-repair of embedded memories," in *Design Automation Conference (Designer Track)*, 2013.
- V. Devanathan, R. Mehrotra, P. S. V. Kumar, V. Sarkar, M. B. Imran, and **S. Bathla**, "Novel approaches for effective and optimized memory test flow in nanoscale technologies," in *VLSI Test Symposium (IP Session)*, 2012.

Preprint

- **S. Bathla** and V. Vasudevan, *MPE inference using an incremental build-infer-approximate paradigm*, 2022. arXiv: 2206.01954.

AWARDS & HONORS

- **Inference competition organized by *Conference on Uncertainty in Artificial Intelligence (UAI)*, 2022** : Submitted solver IBIA, which won the following positions (https://uaicompetition.github.io/uci-2022/results/final-leader-board).
  - Task PR (partition function): **1st position** in the 1 hr category, 2nd position in the 20 min category.
  - Task MAR (marginal probabilities): **2nd position** in the 20 min and 1 hr categories.
- Selected for Google Research Week 2024.
- Recipient of Google Travel Grant (2023) for presenting paper at NeurIPS.
- Among top 1% certified in NPTEL course on Deep Learning (2018).
- Rank 9 in Junior Mathematical Olympiad (2003) organized by the Indian Mathematical Olympiads Foundation.

RELEVANT COURSEWORK

- Machine learning and pattern recognition
- Probability foundations
- Linear algebra
- Optimization methods

ONLINE CERTIFICATIONS

- Deep Learning | NPTEL | Link
- Introduction to Tensorflow | Coursera | Link
- Probabilistic Graphical Models | Coursera | Link
- Automated reasoning | Coursera | Link

WORK EXPERIENCE

Design Engineer

Texas Instruments (India) Pvt. Ltd.

Jul 2011 – May 2014 — Bengaluru, India

- Development and support of automated memory datapath generation for TI's built-in self-test solution.
- Enhancement of on-chip self-repair solution for incremental repair.
- Development of regression framework for testing memory and logic in circuits.
- Evaluation of 3rd Party vendor Memory IPs and Memory BIST solutions.

INTERNSHIP

IBM India Private Limited

May 2015–Dec 2015 — Bengaluru, India

Project: Analytical model for glitch power estimation

Texas Instruments (India) Pvt. Ltd.

Jan 2011–Jul 2011 — Bengaluru, India

Project: Automation of RTL generation for memory testchip

National Institute of Science, Technology and Development Studies

Jun 2009–Jul 2009 — New Delhi, India

Study-oriented project: Outsourcing in the field of semiconductor chip design

SKILLS

- Languages - Python, Perl, C, Tcl, MATLAB
- Tools/Libraries - Tensorflow, PyTorch, Numpy, SciPy, Scikit-learn, Pandas, Matplotlib

REFEREES

Prof. Vinita Vasudevan — vinita@ee.iitm.ac.in

Prof. Nitin Chandrachoodan — nitin@ee.iitm.ac.in