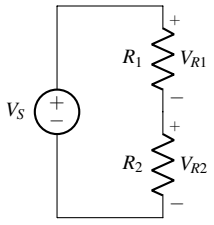
EECS 16A Designing Information Devices and Systems I
Spring 2020 Discussion 10A

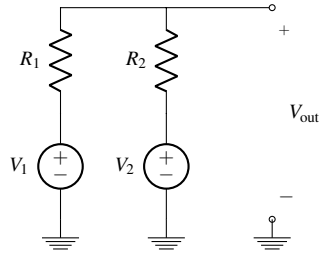
For Reference: Example Circuits

Voltage Divider



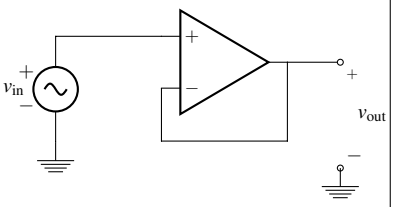
$$V_{R2} = V_S\left(\frac{R_2}{R_1+R_2}\right)$$

Voltage Summer



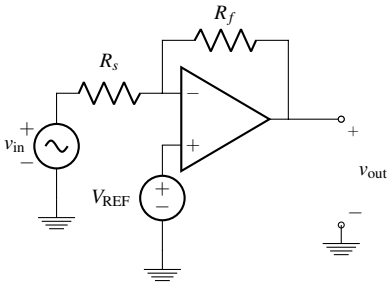
$$V_{\text{out}} = V_1\left(\frac{R_2}{R_1+R_2}\right) + V_2\left(\frac{R_1}{R_1+R_2}\right)$$

Unity Gain Buffer



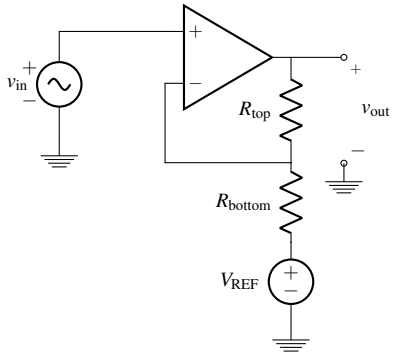
$$\frac{v_{\text{out}}}{v_{\text{in}}} = 1$$

Inverting Amplifier



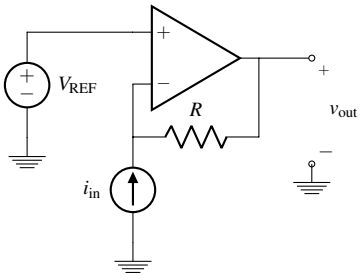
$$v_{\text{out}} = v_{\text{in}}\left(-\frac{R_f}{R_s}\right) + V_{\text{REF}}\left(\frac{R_f}{R_s}+1\right)$$

Non-inverting Amplifier



$$v_{\text{out}} = v_{\text{in}}\left(1+\frac{R_{\text{top}}}{R_{\text{bottom}}}\right) - V_{\text{REF}}\left(\frac{R_{\text{top}}}{R_{\text{bottom}}}\right)$$

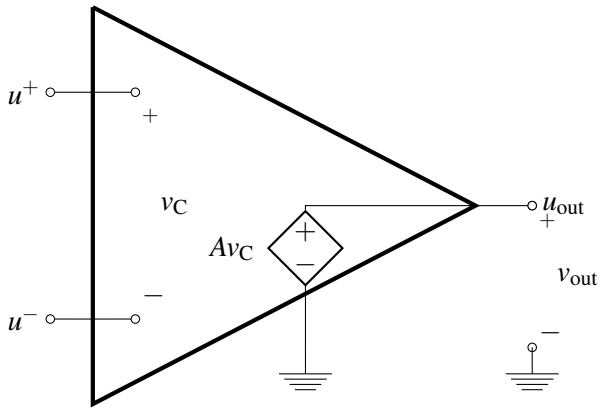
Transresistance Amplifier



$$v_{\text{out}} = i_{\text{in}}(-R) + V_{\text{REF}}$$

1. Op-Amp Rules and Negative Feedback Rule

Here is an equivalent circuit of an op-amp (where we are assuming that $V_{SS} = -V_{DD}$) for reference:



(a) What are the currents flowing into the positive and negative terminals of the op-amp (i.e., what are I^+ and I^-)? Based on this answer, what are some of the advantages of using an op-amp in your circuit designs?

Answer:

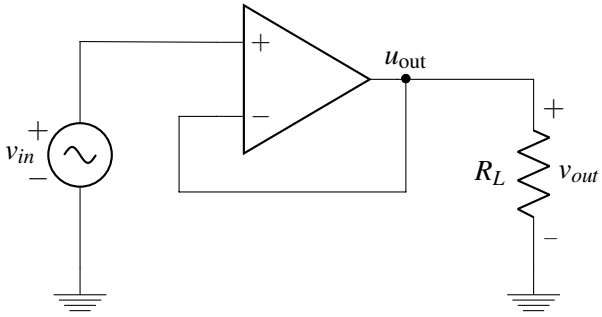
The u^+ and u^- terminals have no closed circuit connection between them, and therefore no current can flow into or out of them. This is very good because we can connect an op-amp to any other circuit, and the op-amp will not disturb that circuit in any way because it does not load the circuit (it is an open circuit).

(b) Suppose we add a resistor of value R_L between u_{out} and ground. What is the value of v_{out}? Does your answer depend on R_L? In other words, how does R_L affect Av_C? What are the implications of this with respect to using op-amps in circuit design?

Answer:

Notice that u_{out} is connected directly to a controlled/dependent voltage source, and therefore v_{out} will always have to be equal to Av_C regardless of what R_L is connected to the op-amp. This is very advantageous because it means that the output of the op-amp can be connected to any other circuit (except a voltage source), and we will always get the desired/expected voltage out of the op-amp.

For the rest of the problem, consider the following op-amp circuit in negative feedback:



(c) Assuming that this is an ideal op-amp, what is v_{out}?

Answer:

Recall for an ideal op-amp in negative feedback, we know from the negative feedback rule that $u^+ = u^-$. In this case, $u^- = u_{out} = u^+$.

(d) Draw the equivalent circuit for this op-amp and calculate v_{out} in terms of A, v_{in}, and R_L for the circuit in negative feedback. Does v_{out} depend on R_L? What is v_{out} in the limit as $A \to \infty$?

Answer:

Notice that the op-amp can be modeled as a voltage-controlled voltage source. Thus, we have the following equation:

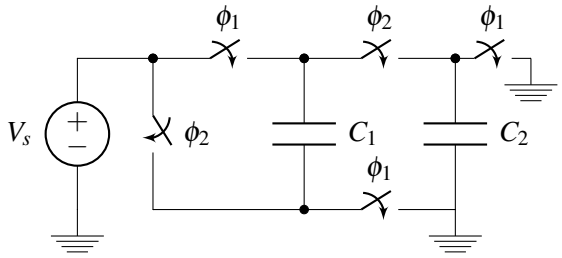
$$\begin{aligned} v_{\text{out}} &= A(v_{in} - v_{\text{out}}) \\ v_{\text{out}} + Av_{\text{out}} &= Av_{in} \\ v_{\text{out}} &= v_{in}\frac{A}{1+A} \end{aligned}$$

Thus, as $A \to \infty$, $v_{\text{out}} \to v_{\text{in}}$. This is the same as what we get after applying the op-amp rule.

Notice that output voltage does not depend on R. Thus, this circuit acts like a voltage source that provides the same voltage read at u^+ without drawing any current from the terminal at u^+. This is why the circuit is often referred to as a "unity gain buffer," "voltage follower," or just "buffer."

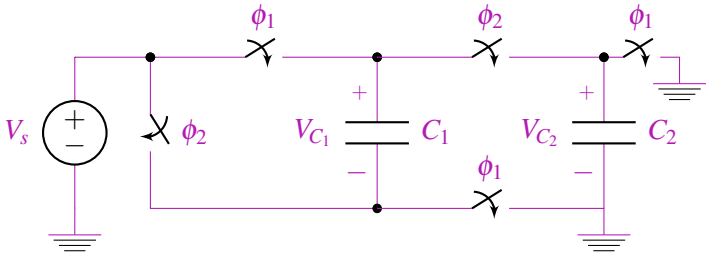
2. Charge Sharing Algorithm

For the switch capacitor circuit below, calculate the value of all node voltages at the end phase 2, as a function of the voltage source V_s and the capacitors C_1, C_2.



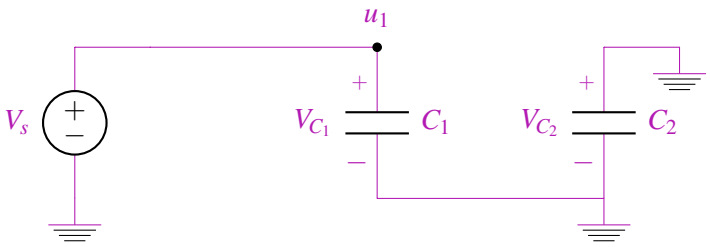
Answer:

Step 1: Label the voltages across all the capacitors. Choose whichever direction (polarity) you want for each capacitor - this means you can mark any one of the plates with the "+" sign, and then you can mark the other plate with the "−" sign. Just make sure you stay consistent with this polarity across phases.

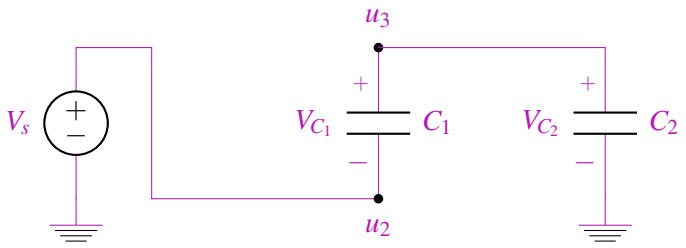


Step 2: Draw the equivalent circuit during both phases (Phase 1: ϕ_1 closed, ϕ_2 open - Phase 2: ϕ_1 open, ϕ_2 closed). Also, label all node voltages on the circuit for both phases. No need to try and maintain the same names, since certain nodes of the phase 1 circuit might be merged or split in phase 2.

Phase 1:



Phase 2:



Step 3: Identify all "floating" nodes in your circuit during phase 2. A floating node is a node out of or into which no charge can flow. You can identify those nodes as the nodes connected only to capacitor plates, op amp inputs or comparator inputs. These will be the nodes where we apply charge sharing.

In this case the only node that is floating during phase 2 is node u_3. (Node u_2 is connected to the voltage source, i.e. $u_2 = V_s$, and the 3^{rd} node is the ground node).

Step 4: For steps 4-6 we will **examine each phase 2 floating node individually**. Pick a floating node from the ones you found in step 3 and identify all capacitor plates connected to that node during phase 2. Then, calculate the charge on each of these plates during phase 1.
To do so, identify all nodes in your circuit during phase 1. Label all node voltages, and write the voltages across each capacitor as functions of node voltages (step 2 should help you with that). Do this according to the polarities you have selected. Then the charge is found as $Q = CV_C$ (where V_C is the voltage *across* a capacitor).
Careful: The plate marked with the "−" sign will have $Q = -CV_C$ and the plate marked with the "+" sign will have $Q = CV_C$ stored onto them.
Careful 2: We assume here that you know all node voltages during phase 1. If you don't, before starting this procedure calculate the node voltages you need using one of the previously introduced circuit analysis techniques (most likely KVL will do the job).

Looking at our single floating node we can see that the "+" plates of C_1 and C_2 are connected to it during phase 2. Let's calculate the charge on these plates during **phase** ϕ_1.

$$\begin{aligned} Q_{u_3}^{\phi_1} &= V_{C_1}C_1 + V_{C_2}C_2 \\ &= (V_s - 0)C_1 + 0 \\ &= V_sC_1 \end{aligned}$$

Step 5: Find the total charge on each of the floating nodes during phase 2 as a function of node voltages. Use the same process as in Step 4, but this time using the node voltages during phase 2 to write the voltages across each capacitor. Make sure you kept the polarity same and pay attention to the sign of each plate.

$$\begin{aligned} Q_{u_3}^{\phi_2} &= V_{C_1}C_1 + V_{C_2}C_2 \\ &= (u_3 - u_2)C_1 + (u_3 - 0)C_2 \\ &= (u_3 - V_s)C_1 + u_3C_2 \end{aligned}$$

Step 6: Equate the total charge calculated in phase 1 (Step 4) to the total charge calculated in phase 2 (Step 5) (charge conservation).

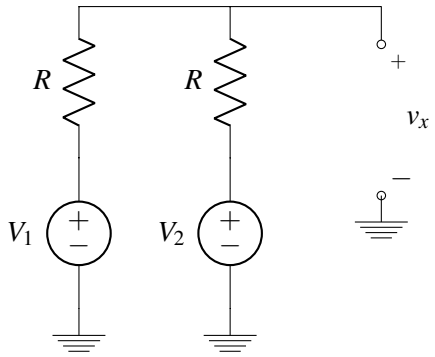
$$\begin{aligned} Q_{u_3}^{\phi_1} &= Q_{u_3}^{\phi_2} \\ V_sC_1 &= (u_3 - V_s)C_1 + (u_3 - 0)C_2 \\ u_3 &= \frac{2C_1}{C_1 + C_2}V_s \end{aligned}$$

Step 7: Repeat steps 4-6 for every floating node. This will give you one equation per floating node (i.e. if you have m floating nodes you will have m equations). You can then solve the system of equations to find the node voltages during phase 2 (unknowns). It should have a unique solution!

In this problem we did not go through step 7 since we only had one floating node during phase 2. This means we have only one unknown node voltage (u_3) for which we solved using our single equation from Step 6. We will be using step 7 in our second example!

3. Dividers for Days

(a) Solve the following circuit for v_x.



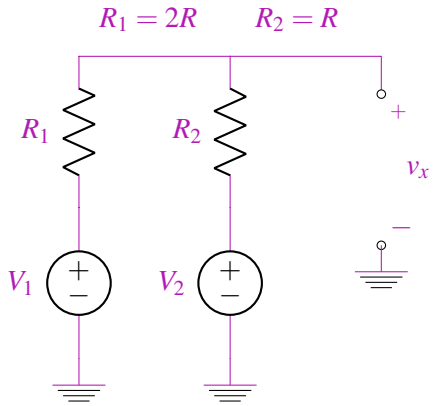
Answer:

$$v_x = \frac{1}{2}V_1 + \frac{1}{2}V_2$$

(b) You have access to two voltage sources, V_1 and V_2. You can use two resistors (as long as $0 \leq R < \infty$). How would you design a circuit that produces a voltage $v_x = \frac{1}{3}V_1 + \frac{2}{3}V_2$?

Answer:

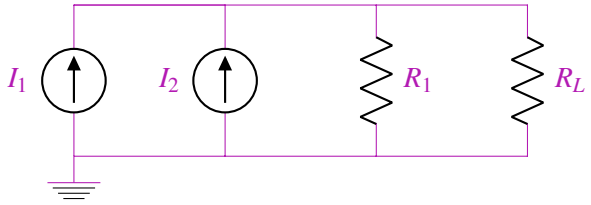
Use superposition. Even if you know the voltage summer, make sure you know the analysis with KVL/KCL. Using any nonzero values for R:



(c) You have two current sources I_1 and I_2. You also have a load resistor $R_L = 6\,\text{k}\Omega$. Similar to the first part, you can use whatever resistors you want (as long as they are finite integer values). How would you design a circuit such that the current running through R_L is $I_L = \frac{2}{5}(I_1 + I_2)$?

Answer:

Use superposition, so think of the two currents as one summed current. Use KCL to determine how to divide the currents.



$$R_L = 6\,\text{k}\Omega, R_1 = 4\,\text{k}\Omega$$

