EECS 16A Designing Information Devices and Systems I
Fall 2016 Babak Ayazifar, Vladimir Stojanovic Homework 7

This homework is due October 18, 2016, at Noon.

Optional Problems: We **do not** grade these problems. Nevertheless, you are responsible for learning the subject matter within their scope.
Bonus Problems: We **do** grade these problems. Doing them will provide an unspecified amount of extra credit; not doing them will not affect your homework grade negatively. We will specify if the problem is in or out of scope.

1. Homework process and study group

Who else did you work with on this homework? List names and student ID's. (In case of hw party, you can also just describe the group.) How did you work on this homework?
Working in groups of 3-5 will earn credit for your participation grade.

Solution: I worked on this homework with...

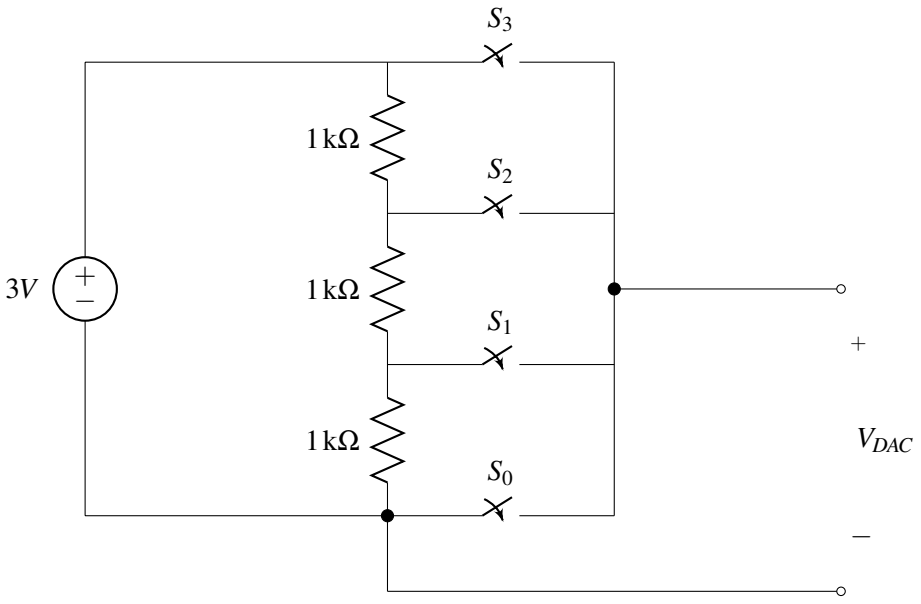
I first worked by myself for 2 hours, but got stuck on Problem 5 so I went to office hours on...

Then I went to homework party for a few hours, where I finished the homework.

2. (Optional) Digital-to-Analog Converter using Voltage Dividers and Summers

Like most microcontrollers, the one included on your LaunchPad has a "Digital-to-Analog Converter" (or DAC for short) that can translate the binary numbers you work with in software in to actual analog voltages. In this problem we will be exploring the design of one such DAC, and the issues we may face when that DAC needs to produce a voltage across a particular resistor.

Fortunately, rather than starting from scratch, one of your colleagues has provided the starting implementation (which would convert 2-bit digital numbers ranging in value from 0 to 3) shown below:



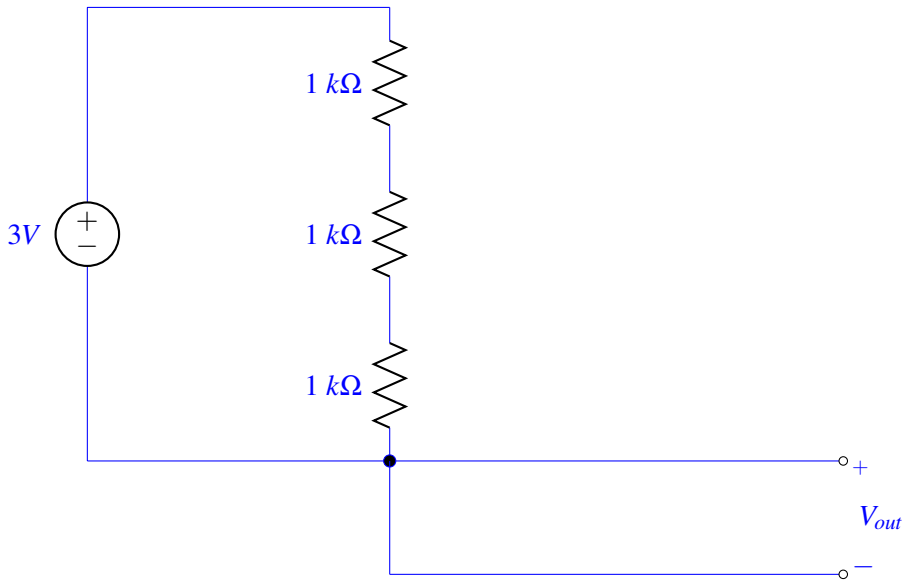
In this design, if the binary number is equal to k, then switch S_k would be closed (i.e., turned on, connected) and all of the other switches would open (i.e., turned off, disconnected). So, for example, if the digital number is 2, then S_2 would be on and S_0, S_1, and S_3 would be off.

(a) For the preliminary design provided by your colleague, fill in the table below that provides the V_{DAC} produced by each binary number k.

k	V_{DAC}
0	
1	
2	
3	

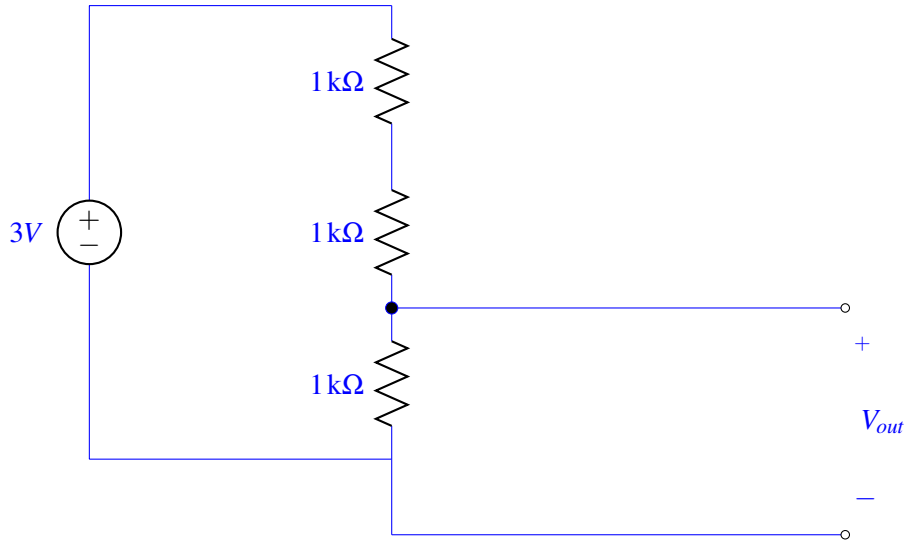
Solution: Let's draw the circuit for each value of k in order to compute what V_{out} is for that configuration:

$k = 0$

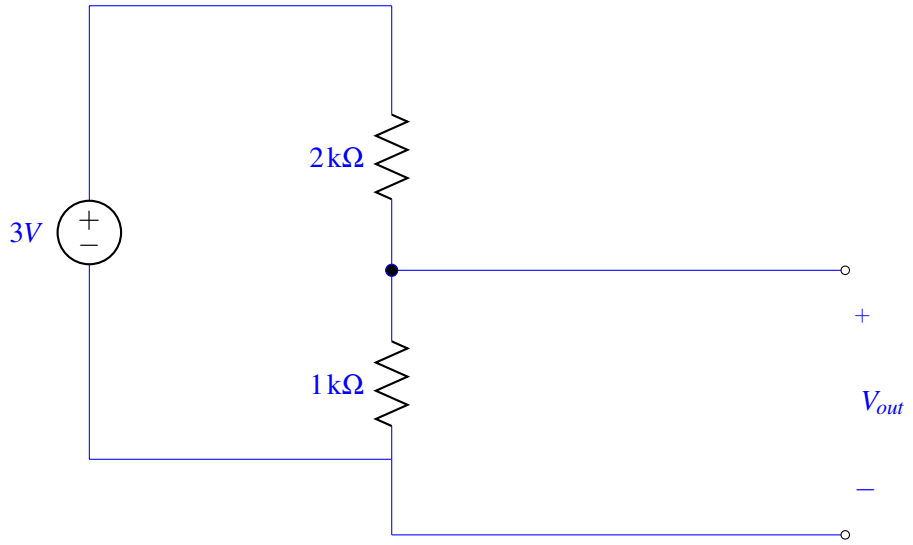


In this case, without doing any math we can see that V_{out} is equal to 0 V since we are measuring the voltage across a short circuit.

$k = 1$

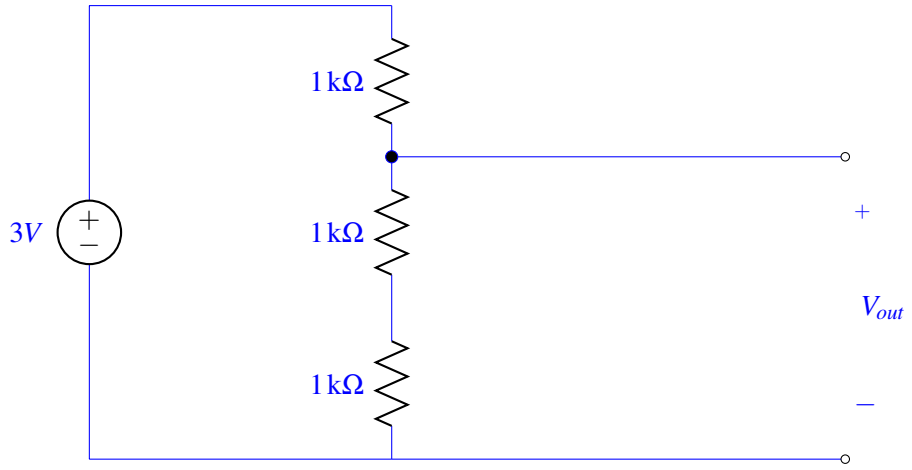


In this configuration, the circuit can be redrawn to match the format of the voltage divider by combining the upper two 1 kΩ resistors in to a single 2 kΩ resistor:

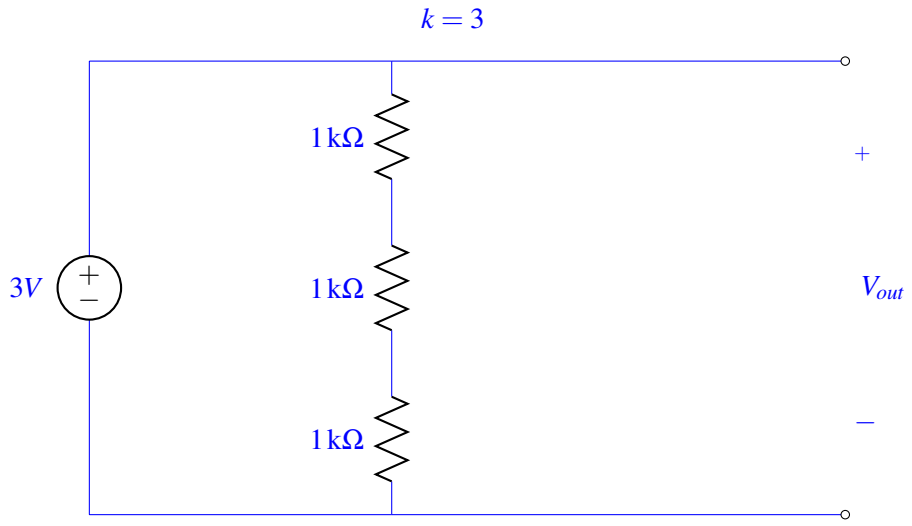


Therefore, in this configuration $V_{out} = \frac{1\,\text{k}\Omega}{2\,\text{k}\Omega+1\,\text{k}\Omega} \cdot 3\,\text{V} = 1\,\text{V}$.

$$k = 2$$



Much like we did with $k = 1$, this circuit can be simplified in to a voltage divider, just this time with the bottom resistors combined in to their series equivalent. Therefore, $V_{out} = \frac{2\,\text{k}\Omega}{2\,\text{k}\Omega + 1\,\text{k}\Omega} \cdot 3\,\text{V} = 2\,\text{V}$.

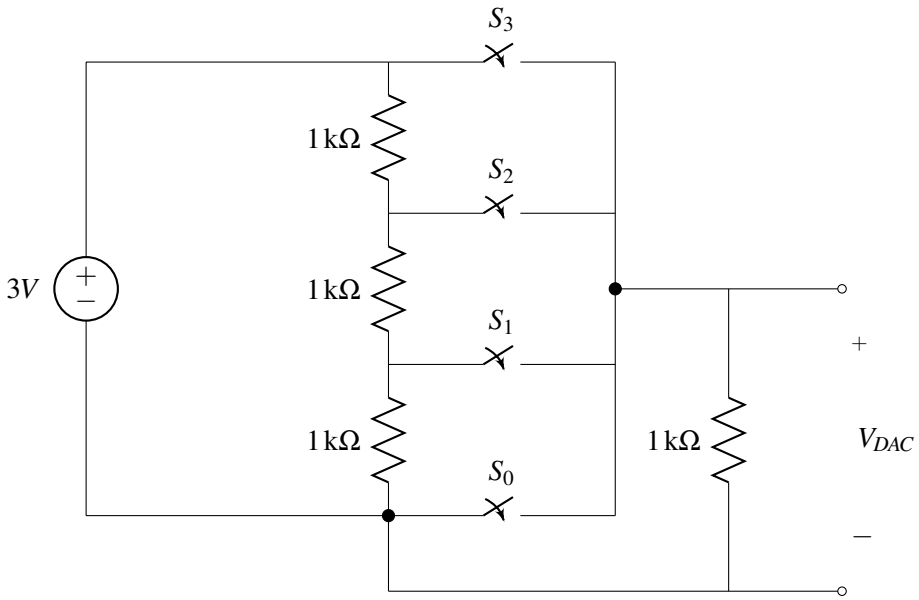


In this case we should notice that V_{out} is being measured directly across the 3 V voltage source, and thus $V_{out} = 3\,\text{V}$.

So, to complete to the table:

k	V_{DAC}
0	0 V
1	1 V
2	2 V
3	3 V

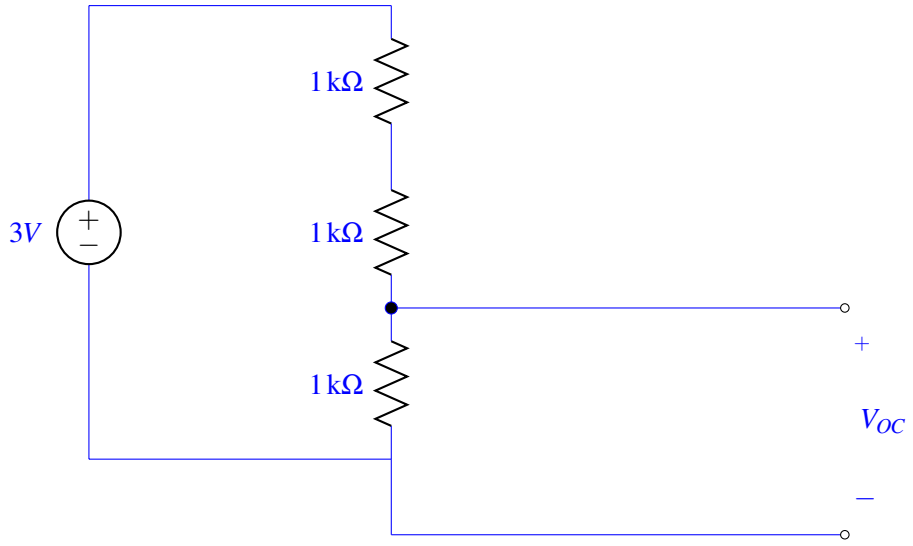
(b) Now let's take a look at what happens when we connect this DAC design to a resistor at its output (as shown below):



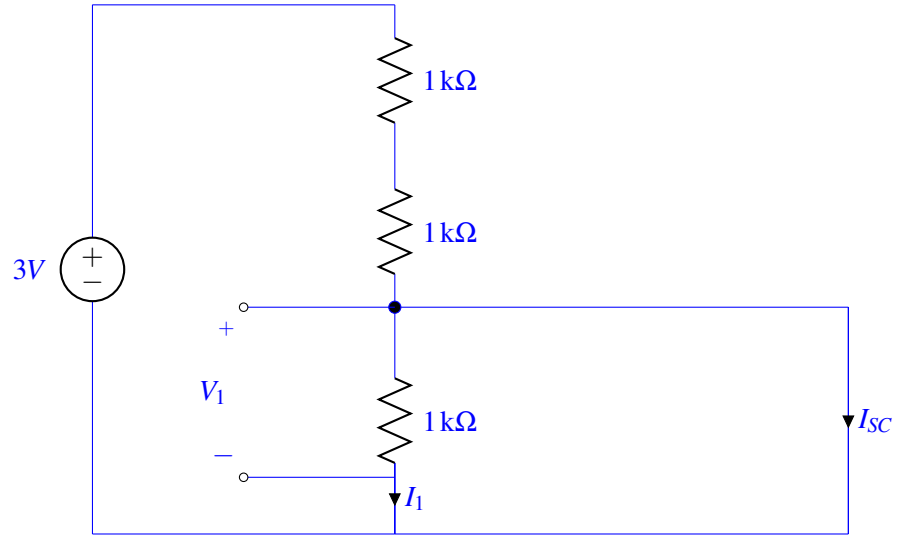
Derive the Thevenin equivalent circuit for the DAC in each of the configurations (i.e., for each of S_0 – S_3 each being on), and use these equivalent circuits to re-populate the table (repeated below):

k	V_{DAC}
0	
1	
2	
3	

Solution: As we saw in part (a), for $k = 0$ the DAC circuit boils down to a short circuit across V_{out}, and so we don't even have to do any work to find the Thevenin equivalent (a short circuit remains a short circuit - i.e., $V_{th} = 0\,\text{V}$, $R_{th} = 0\,\Omega$). V_{out} also remains completely unaffected and equals 0 V.
Now let's derive the Thevenin equivalent for $k = 1$ by finding V_{OC} and I_{SC}:



$$V_{out} = \frac{1\,\text{k}\Omega}{2\,\text{k}\Omega + 1\,\text{k}\Omega} \cdot 3\,\text{V} = 1\,\text{V}$$

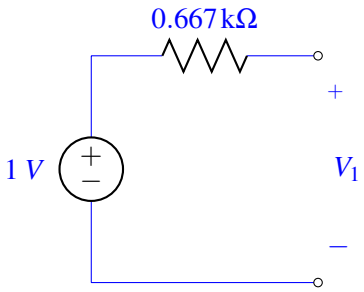


Because of that circuit, $V_1 = 0\,\text{V}$, and $I_1 = 0\,\text{A}$.

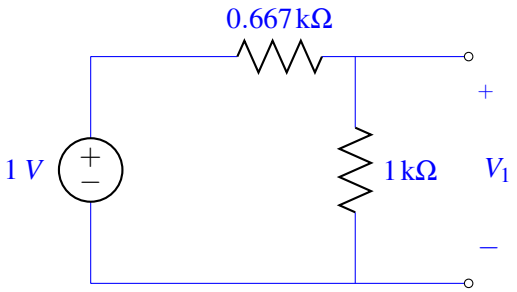
Therefore $I_s = I_{SC} = \frac{3\,\text{V}}{1\,\text{k}\Omega + 1\,\text{k}\Omega}$.

$$I_{SC} = 1.5\,\text{mA}$$

Recalling that $R_{th} = \frac{V_{OC}}{I_{SC}} = \frac{1\,\text{V}}{1.5\,\text{mA}} = 0.667\,\text{k}\Omega$, the Thevenin equivalent circuit in this case is:

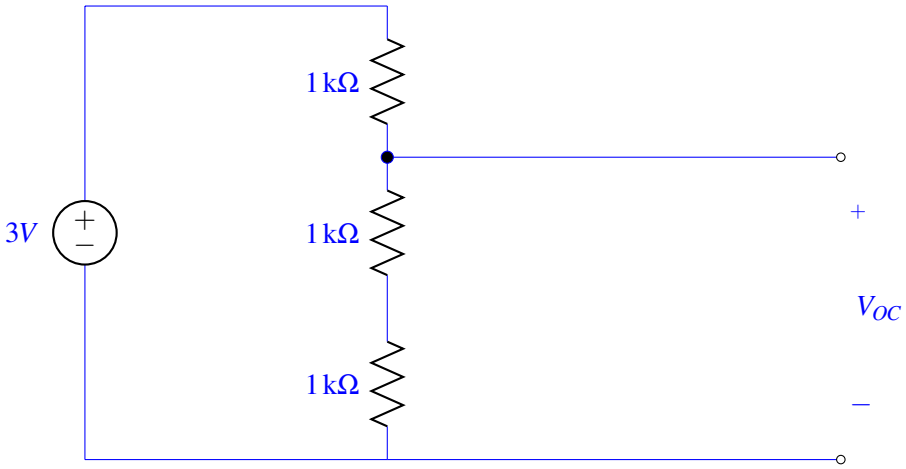


Therefore, when we connected the 1 kΩ resistor across V_{out}, we get:

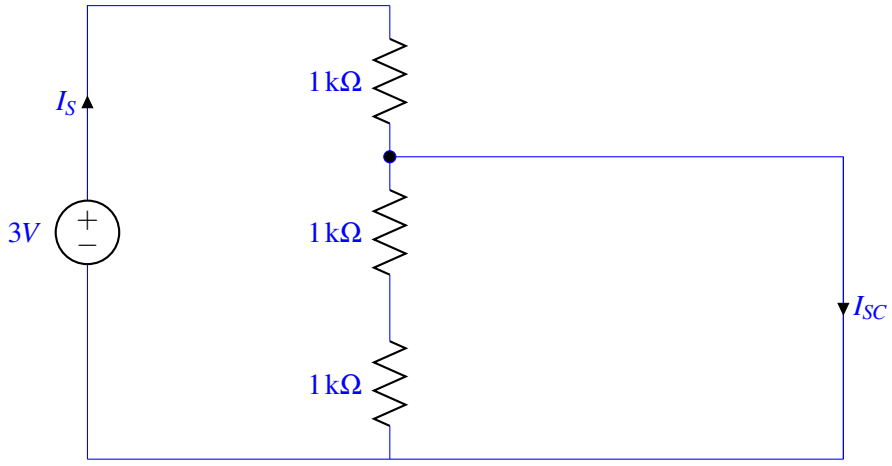


$$V_{out} = \frac{1\,\text{k}\Omega}{1\,\text{k}\Omega + 0.667\,\text{k}\Omega} \cdot 1\,\text{V} = 0.6\,\text{V}$$

Now let's derive the Thevenin equivalent for $k = 2$ by once again finding V_{OC} and I_{SC}:



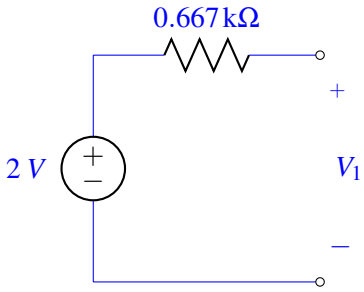
$$V_{out} = \frac{2\,\text{k}\Omega}{2\,\text{k}\Omega + 1\,\text{k}\Omega} \cdot 3\,\text{V} = 2\,\text{V}$$



For essentially the same reasons as $k = 1$, $I_S = I_{SC}$.

$$I_{SC} = \frac{3\,\text{V}}{1\,\text{k}\Omega} = 3\,\text{mA}$$

Therefore, $R_{th} = \frac{2\,\text{V}}{3\,\text{mA}} = 0.667\,\text{k}\Omega$, and the Thevenin equivalent circuit for $k = 2$ is:



Similarly, when we connect the 1 kΩ resistor across V_{out}, we once again end up with a simple voltage divider, so that

$$V_{out} = \frac{1\,\text{k}\Omega}{1\,\text{k}\Omega + 0.667\,\text{k}\Omega} \cdot 2\,\text{V} = 1.2\,\text{V}$$

Finally, for $k = 3$, as also explained in part (a), the DAC circuit simply boils down to a fixed voltage source (3 V), and so the Thevenin equivalent is just that as well (i.e., $V_{th} = 3\,\text{V}$, $R_{th} = 0\,\Omega$), with V_{out} completely unaffected by the addition of the 1 kΩ resistor (i.e., V_{out} still equals 3 V). So, to complete the table:

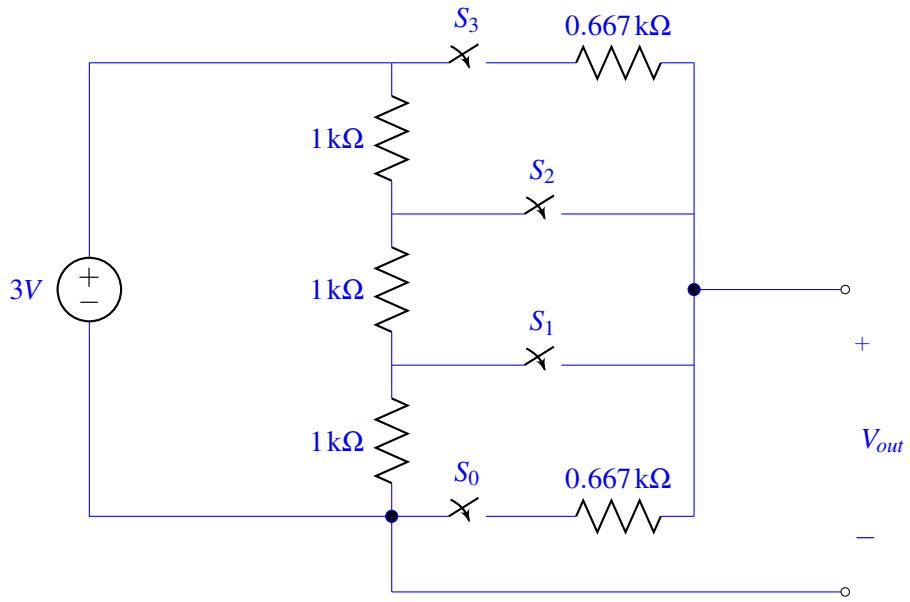
k	V_{DAC}
0	0 V
1	0.6 V
2	1.2 V
3	3 V

(c) Use the Thevenin equivalent circuits you derived in part (b) to explain why you got only two of the entries in the table for part (b) to be different than the entries in the table for part (a). Be as specific as possible; what is it about the Thevenin equivalent circuits that would affect how the ideal V_{DAC} (which is the result from part (a)) is altered by the 1 kΩ resistor?

Solution: The key is to realize that in two of the configurations for the DAC circuit - specifically, $k = 0$ and $k = 3$, the Thevenin equivalent resistance is 0 Ω, and hence no matter what we connect at the output of the circuit, the output voltage will remain unchanged. In contrast, for $k = 1$ and $k = 2$, the Thevenin equivalent resistance in both cases is non-zero (specifically, 0.667 kΩ), and hence connecting a resistance across V_{out} results in a voltage divider that makes the output voltage lower than what we calculated in part (a).

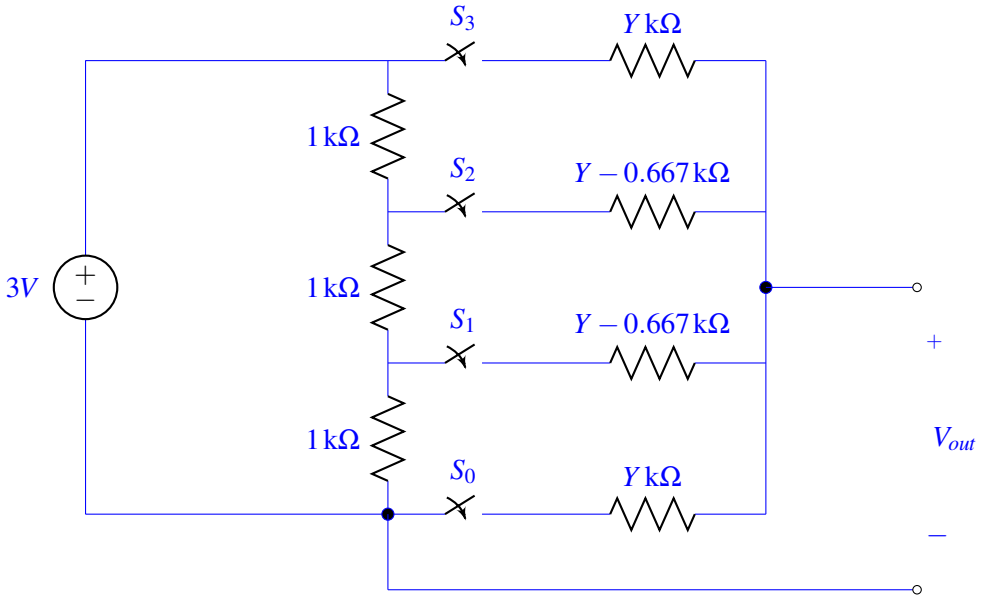
(d) Modify the design from part (b) so that the VDAC output once again has ideally spaced levels despite the presence of the 1 kΩ resistor at the output. In other words, your goal is to modify the circuit so that for $k = 0, 1, 2, 3$, $V_{out} = 0, z, 2z, 3z$, where z is an arbitrary number.

Solution: From part (c), we noticed that the reason $k = 0$ and $k = 3$ had their output voltage unchanged was that R_{th} in those cases ended up being 0 Ω, while for $k = 1$ and $k = 2$ R_{th} was 0.667 kΩ. We don't (yet) have a way of modifying the circuit so that $R_{th} = 0\,\Omega$ for $k = 1$ and $k = 2$, so instead our best bet is to modify the circuit to make R_{th} equal to 0.667 kΩ for $k = 0$ and $k = 3$ (i.e., to make R_{th} constant regardless of k). This means we need to some kind of series resistance, but we need to do this in a way that wouldn't affect the circuit (or it's Thevenin equivalent) in the other two configurations. The easiest way to do that is as shown below:



With this design and the 1 kΩ resistor connected across V_{out}, we would find that $V_{out} = 0.6\,\text{V} \cdot k$.

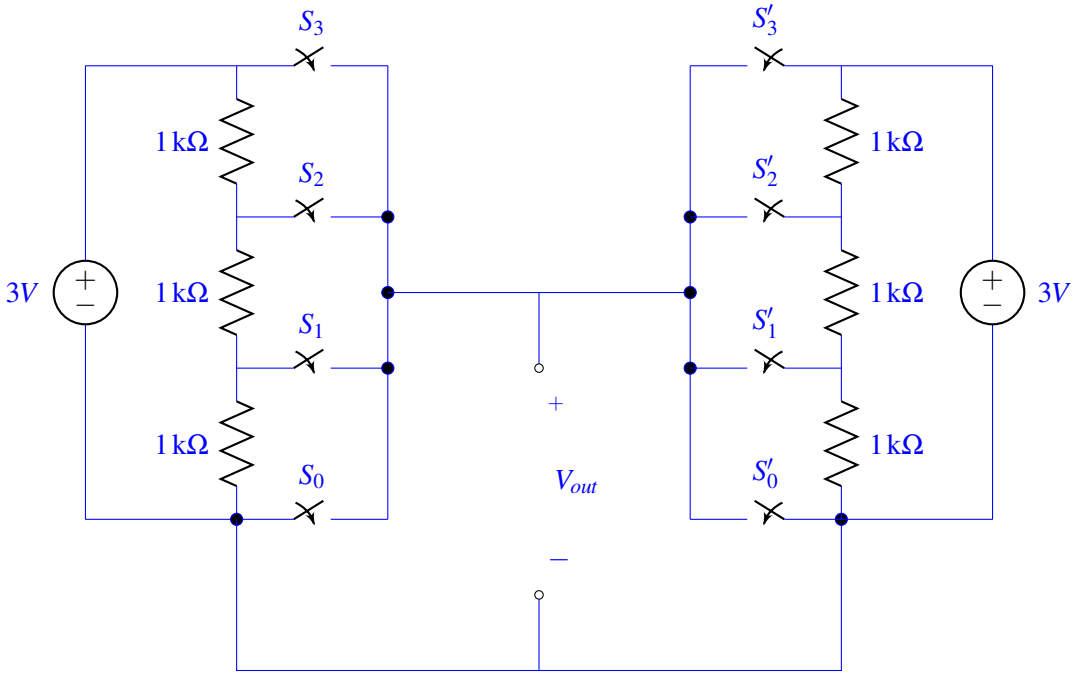
Note that another perfectly valid solution would be to insert series resistors after all four of the switches as shown below:



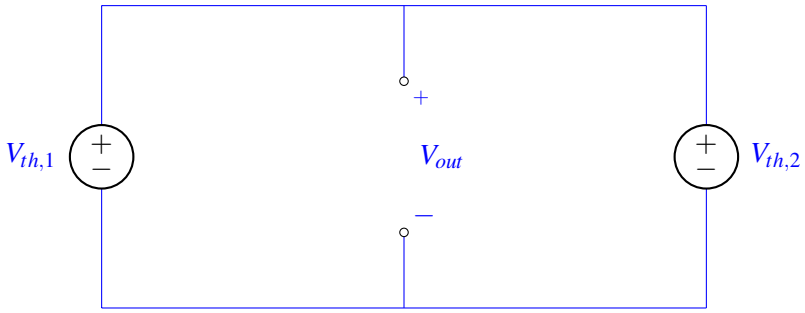
In this case, if we connect a $1\,\text{k}\Omega$ resistor across V_{out}, then $V_{out}(k) = \left(\frac{1}{(1+Y)\cdot 1\,\text{V}}\right)\cdot k$.

(e) Now let's say that we actually have two binary numbers k_1 and k_2 (each of which can take on values of 0, 1, 2, or 3), and that we now want to enable our microcontroller to produce an analog output $V_{sum} = \frac{1}{4}k_1 + \frac{3}{4}k_2$. (Note that for this part V_{sum} can be measured by an open-circuit - i.e., you do not need to worry about your circuit being connected to anther external resistor.) Based on all of your work in this problem so far, design a new circuit that achieves this goal. (Hint: you might want to use superposition and Thevenin equivalence to analyze what would happen if you connected two of the DAC circuits from part (a) together.)

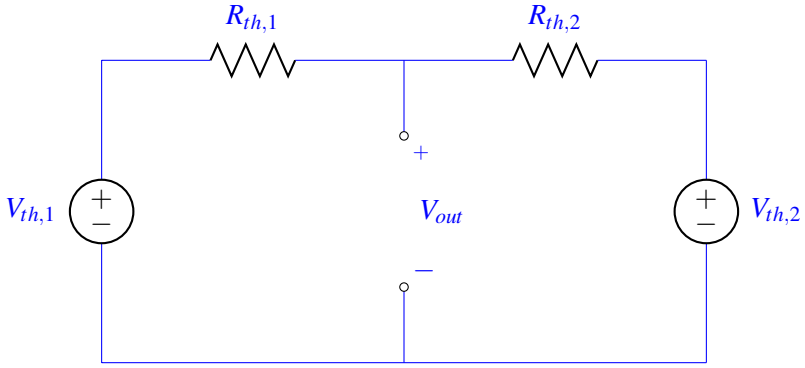
Solution: Let's first sketch what happens if we connect two of the DAC circuits from part (a) together:



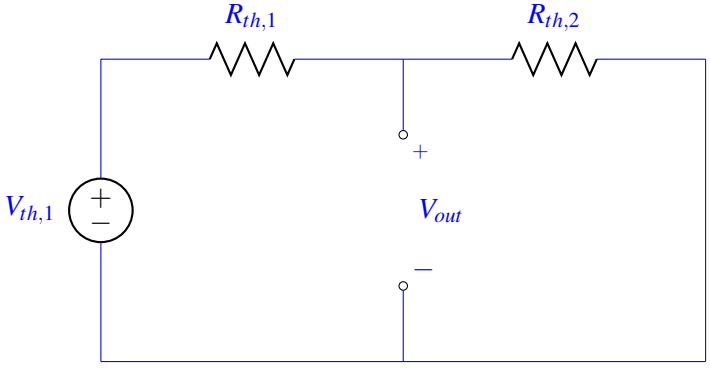
Rather than exhaustively attempting to analyze all of the different scenarios for each combination of k_1 and k_2, let's use some of the intuition we gained from our previous examination of the the Thevenin equivalent circuit for each DAC. In fact, if we refer to the Thevenin equivalent circuit of the DAC for k_1 using $V_{th,1}$, $R_{th,1}$, and to the Thevenin equivalent circuit of the DAC for k_2 using $V_{th,2}$, $R_{th,2}$, we can actually quickly conclude that this design simply won't work because of one pathological case that will give us a hint as to how to move forward. Specifically, imagine that $R_{th,1} = R_{th,2} = 0\,\Omega$, but that $V_{th,1} \neq V_{th,2}$ (as shown below). This is one of those case we covered in lecture where we said "something blows up", because we have two ideal voltage sources trying to set V_{out} to a specific (but different) value. In other words, there is simply no way for both KVL and the ideal voltage source conditions to be obeyed.



This pathological case arises because of the fact that our original DAC design from part (a) had configurations in it where $R_{th} = 0\,\Omega$. As we saw in part (d) however (for different reasons), we can modify the DAC circuit such that it has a constant R_{th} regardless of the value of k. If we do this and analyzing the Thevenin equivalents of the two DAC's connected together, we now get the following circuit:

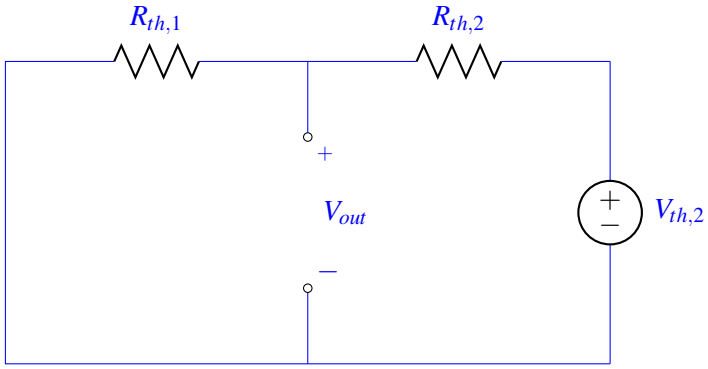


Just like we saw in lecture, we can analyze this circuit using superposition; as a first step, let's compute the contribution to V_{out} due to $V_{th,1}$:



$$V_{out,1} = \frac{R_{th,2}}{R_{th,1} + R_{th,2}} \cdot V_{th,1}$$

Now, let's compute the contribution due to $V_{th,2}$:

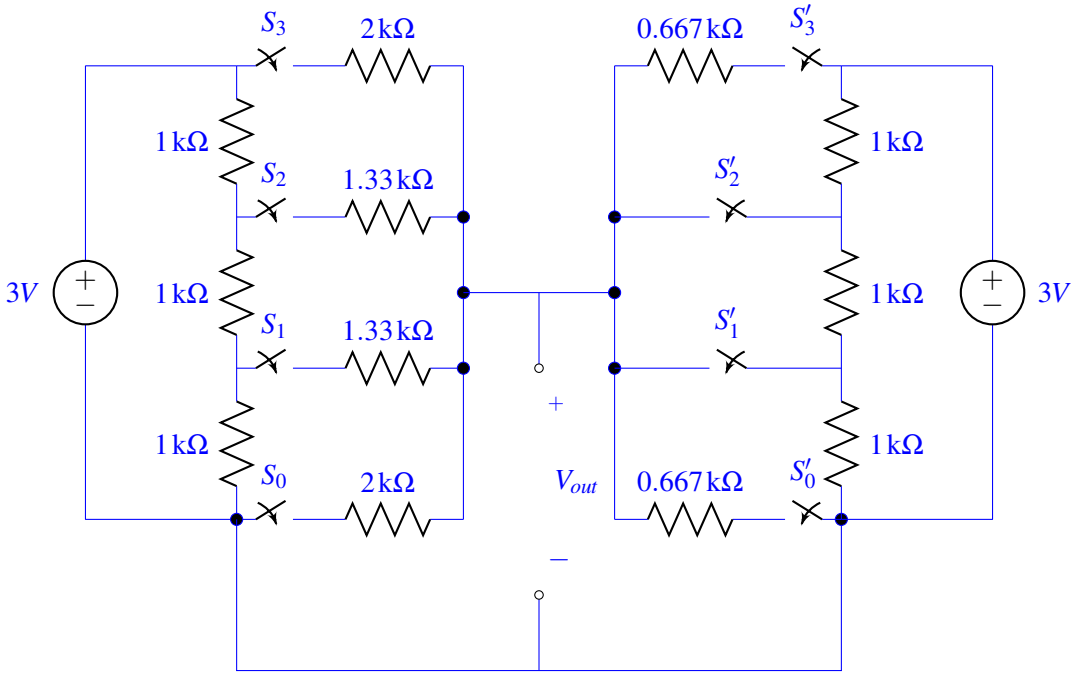


$$V_{out,2} = \frac{R_{th,1}}{R_{th,1} + R_{th,2}} \cdot V_{th,2}$$

Finally, summing up the two contributions, we get that:

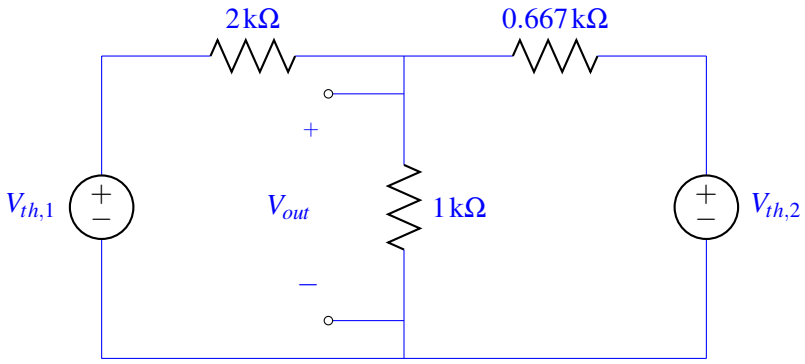
$$V_{out} = \left(\frac{R_{th,2}}{R_{th,1} + R_{th,2}}\right) \cdot V_{th,1} + \left(\frac{R_{th,1}}{R_{th,1} + R_{th,2}}\right) \cdot V_{th,2}$$

Notice that is essentially exactly the form we were looking for, so really all we need to do if figure out how to set $R_{th,1}$ and $R_{th,2}$ to make the coefficients in front of $\frac{V_{th,1}}{V_{th,2}}$ equal to $\frac{1}{4}$ and $\frac{3}{4}$. As should hopefully be obvious, picking $R_{th,1} = 3 \cdot R_{th,2}$ achieves exactly this objective. So, to choose some actual values in a way that minimizes the amount of modifications we need to introduce to each individual DAC design, let's go with $R_{th,2} = 0.667\,\text{k}\Omega$ and $R_{th,1} = 2\,\text{k}\Omega$. Therefore, our final design will be:

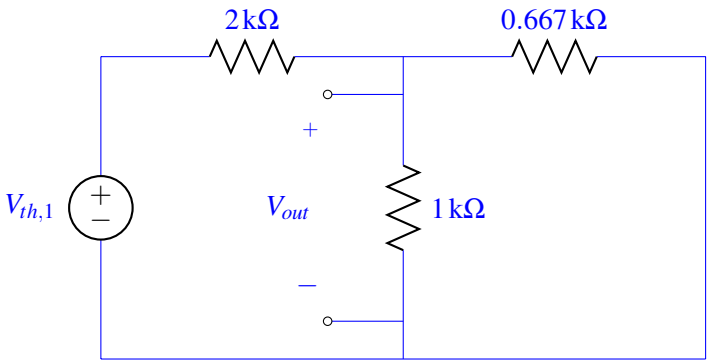


(f) Now take your design from part (e) and connect a 1 kΩ resistor across V_{sum} - how does this alter the relationship between V_{sum} and k_1, and k_2? (Try to answer this by doing as little additional work as possible vs. what you've already done.)

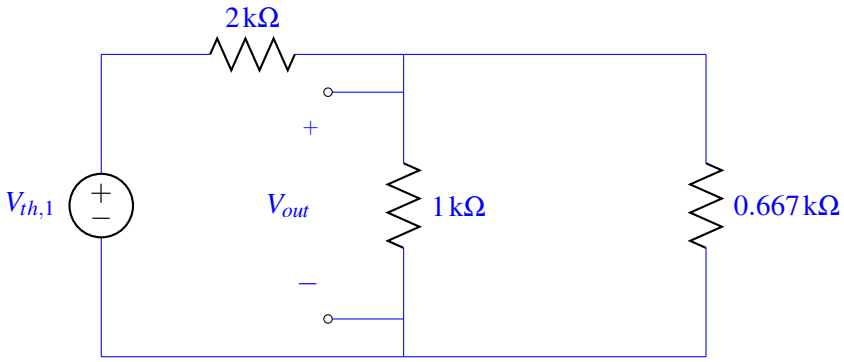
Solution: The easiest way to do this is to once again use our Thevenin equivalent circuits and analyze the situation using superposition:



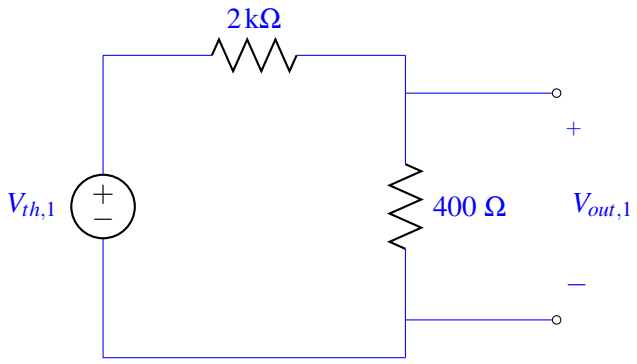
As usual with superposition, let's figure out the contribution due to $V_{th,1}$:



Re-drawing, this is the same as:

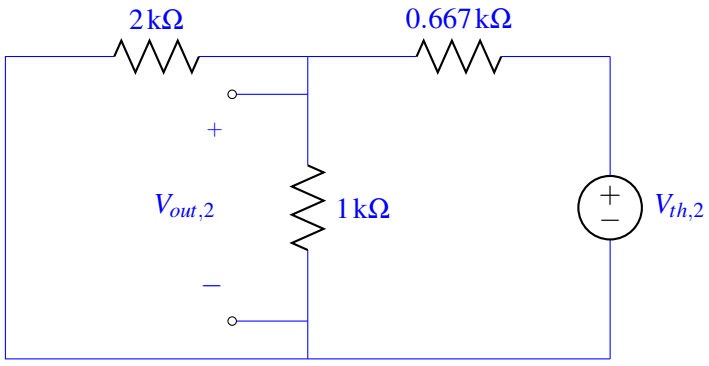


This is equivalent to:

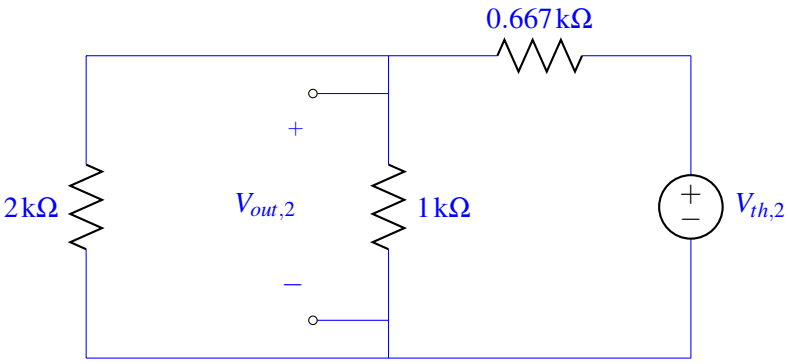


$$\text{Therefore } V_{out,1} = \frac{0.4\,\text{k}\Omega}{0.4\,\text{k}\Omega + 2\,\text{k}\Omega} \cdot V_{th,1} = \frac{1}{6} \cdot V_{th,1}$$

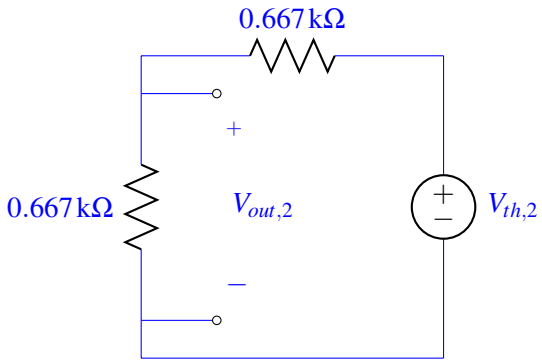
Now let's look at the contribution due to $V_{th,2}$:



This is identical to:



This is equivalent to:



Therefore,

$$V_{out,2} = \frac{0.667\,\text{k}\Omega}{0.667\,\text{k}\Omega + 0.667\,\text{k}\Omega} \cdot V_{th,2} = \frac{1}{2} \cdot V_{th,2}$$

Summing up the two contributions, we find that

$$V_{out} = \frac{1}{6} \cdot V_{th,1} + \frac{1}{2} \cdot V_{th,2} = \frac{2}{3} \cdot \left(\frac{1}{4} V_{th,1} + \frac{3}{4} V_{th,2} \right)$$

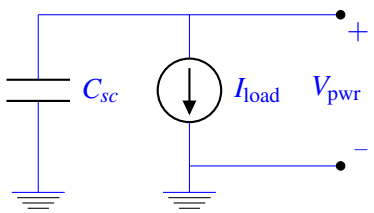
3. Super-Capacitors

In order to enable small devices for the "Internet of Things" (IoT), many companies and researchers are currently exploring alternative means of storing and delivering electrical power to the electronics within these devices. One example of these are "super-capacitors" - the devices generally behave just like a "normal" capacitor, but have been engineered to have extremely high values of capacitance relative to other devices that fit in to the same physical volume.

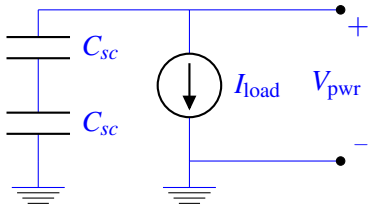
Your startup named **IoT4eva** is designing a new device that will revolutionize the process of making pizza, and you've been put in charge of selecting an energy source for it. You can't find a battery that quite suits your needs, so you decide to try out some super capacitors in various configurations. The super capacitors will be charged up to a certain voltage in the factory, and will then act as the power supply (source of voltage) for the electronics in your device.

(a) Assuming that the electronics in your device can be modeled as drawing a constant current with a value of I_{load}, draw circuit models for your device using the following configurations of super-capacitors as the power supply for the electronics:

i. a single super-capacitor
Solution:

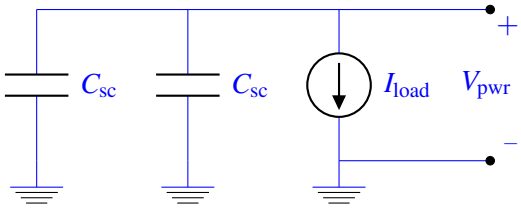


ii. two super-capacitors stacked in series
Solution:



iii. two super-capacitors connected in parallel

Solution:



(b) If each super-capacitor is charged to an initial voltage V_{init} and has a capacitance of C_{sc}, for each of the three configurations above, write an expression for the voltage supplied to your electronics as a function of time after the device has been activated (t).

Solution:

Let the initial voltage each super capacitor is charged to be V_{init}. We'll now consider the three situations

- Config 1: **Single super capacitor**
  In this case, the initial voltage that the super capacitor provides is V_{init} and the intial charge stored in it is then given by $Q_{\text{init}} = V_{\text{init}}C_{\text{sc}}$. Let the voltage at any time (t) be defined by $V_{\text{pwr}}(t)$. The charge drained by the constant current source in time t is given by $I_{\text{load}}t$. The effective charge stored in the capacitor after time t is given by $Q(t) = Q_{\text{init}} - I_{\text{load}}t$. Therefore,

$$\begin{aligned} V_{\text{pwr}}(t) &= \frac{Q(t)}{C_{\text{sc}}} \\ &= \frac{Q_{\text{init}} - I_{\text{load}}t}{C_{\text{sc}}} \\ &= \frac{V_{\text{init}}C_{\text{sc}} - I_{\text{load}}t}{C_{\text{sc}}} \\ &= V_{\text{init}} - \frac{I_{\text{load}}t}{C_{\text{sc}}} \end{aligned}$$

- Config 2: **Two super capacitors in series**
  In this case, the initial voltage that the effective super capacitor provides is $2V_{\text{init}}$ and the effective capacitance is $C_{\text{eff}} = \frac{C_{\text{sc}}}{2}$. Then, the initial effective charge stored in them is then given by $Q_{\text{init}} = 2V_{\text{init}}C_{\text{eff}} = 2V_{\text{init}}\frac{C_{\text{sc}}}{2} = V_{\text{init}}C_{\text{sc}}$. Let the voltage at any time (t) be defined by $V_{\text{pwr}}(t)$. The charge drained by the constant current source in time t is given by $I_{\text{load}}t$. The effective charge stored in the combination after time t is given by $Q(t) = Q_{\text{init}} - I_{\text{load}}t$. Therefore,

$$\begin{aligned} V_{\text{pwr}}(t) &= \frac{Q(t)}{C_{\text{eff}}} \\ &= \frac{Q_{\text{init}} - I_{\text{load}}t}{C_{\text{eff}}} \\ &= \frac{V_{\text{init}}C_{\text{sc}} - I_{\text{load}}t}{C_{\text{eff}}} \\ &= 2V_{\text{init}} - \frac{2I_{\text{load}}t}{C_{\text{sc}}} \end{aligned}$$

- Config 3: **Two super capacitors in parallel**
  In this case, the initial voltage that the effective super capacitor provides is V_{init} and the effective capacitance is $C_{\text{eff}} = 2C_{\text{sc}}$. Then, the initial effective charge stored in them is then given by $Q_{\text{init}} = V_{\text{init}}C_{\text{eff}} = 2V_{\text{init}}C_{\text{sc}}$. Let the voltage at any time (t) be defined by $V_{\text{pwr}}(t)$. The charge drained by the constant current source in time t is given by $I_{\text{load}}t$. The effective charge stored in the combination after time t is given by $Q(t) = Q_{\text{init}} - I_{\text{load}}t$. Therefore,

$$\begin{aligned} V_{\text{pwr}}(t) &= \frac{Q(t)}{C_{\text{eff}}} \\ &= \frac{Q_{\text{init}} - I_{\text{load}}t}{C_{\text{eff}}} \\ &= \frac{2V_{\text{init}}C_{\text{sc}} - I_{\text{load}}t}{C_{\text{eff}}} \\ &= V_{\text{init}} - \frac{I_{\text{load}}t}{2C_{\text{sc}}} \end{aligned}$$

(c) Now let's assume that your electronics require some minimum voltage V_{min} in order to function properly. For each of the three super-capacitor configurations, write an expression you could use to calculate the lifetime of the device.

Solution:

The lifetime of a device is the time it takes for the $V_{\text{pwr}}(t)$ to hit the threshold V_{min}. For each of the three configurations, let's find out the lifetime (denoted by t_0)

- Config 1: **Single super capacitor**
  Let us calculate at what time t_0 does $V_{\text{pwr}}(t)$ equal V_{min}. We know from the previous part that

$$V_{\text{pwr}}(t) = V_{\text{init}} - \frac{I_{\text{load}}t}{C_{\text{sc}}}$$

  Substituting $V_{\text{pwr}}(t) = V_{\text{min}}$, we get

$$t_0 = \frac{(V_{\text{init}} - V_{\text{min}})C_{\text{sc}}}{I_{\text{load}}}$$

- Config 2: **Two super capacitors in series**
  Let us calculate at what time t_0 does $V_{\text{pwr}}(t)$ equal V_{min}. We know from the previous part that

$$V_{\text{pwr}}(t) = 2V_{\text{init}} - \frac{2I_{\text{load}}t}{C_{\text{sc}}}$$

  Substituting $V_{\text{pwr}}(t) = V_{\text{min}}$, we get

$$t_0 = \frac{(2V_{\text{init}} - V_{\text{min}})C_{\text{sc}}}{2I_{\text{load}}}$$

- Config 3: **Two super capacitors in parallel**
  Let us calculate at what time t_0 does $V_{\text{pwr}}(t)$ equal V_{min}. We know from the previous part that

$$V_{\text{pwr}}(t) = V_{\text{init}} - \frac{I_{\text{load}}t}{2C_{\text{sc}}}$$

  Substituting $V_{\text{pwr}}(t) = V_{\text{min}}$, we get

$$t_0 = \frac{(V_{\text{init}} - V_{\text{min}})2C_{\text{sc}}}{I_{\text{load}}}$$

Note: We could have also figured it out by finding out how much charge needs to be removed to cause the voltage at the effective capacitance to drop to V_{min}. Thus we have

$$\Delta Q = (V_{\text{init}} - V_{\text{min}})C_{\text{eff}}$$

which gives us

$$t_0 = \frac{\Delta Q}{I_{\text{load}}}$$

(d) Assuming that a single super-capacitor doesn't provide you sufficient lifetime and so you have to spend the extra money (and device volume) for another super-capacitor. Which configuration would you pick and why would you pick one over the other?

- Config 2: two super-capacitors stacked in series
- Config 3: two super-capacitors connected in parallel

Solution:

It is not obvious from the previous part whether configuration 2 or 3 will provide a longer lifetime. In fact, it depends on what V_{init} is with respect to V_{min}. Let us now see what conditions we need on V_{init} such that the parallel configuration provides a longer lifetime *i.e.,* $t_{0,\text{ parallel}} > t_{0,\text{ series}}$. From the previous part we get

$$\frac{(V_{\text{init}} - V_{\text{min}})2C_{\text{sc}}}{I_{\text{load}}} \geq \frac{(2V_{\text{init}} - V_{\text{min}})C_{\text{sc}}}{2I_{\text{load}}}$$

$$2(V_{\text{init}} - V_{\text{min}}) \geq V_{\text{init}} - \frac{V_{\text{min}}}{2}$$

$$V_{\text{init}} \geq \frac{3}{2}V_{\text{min}}$$

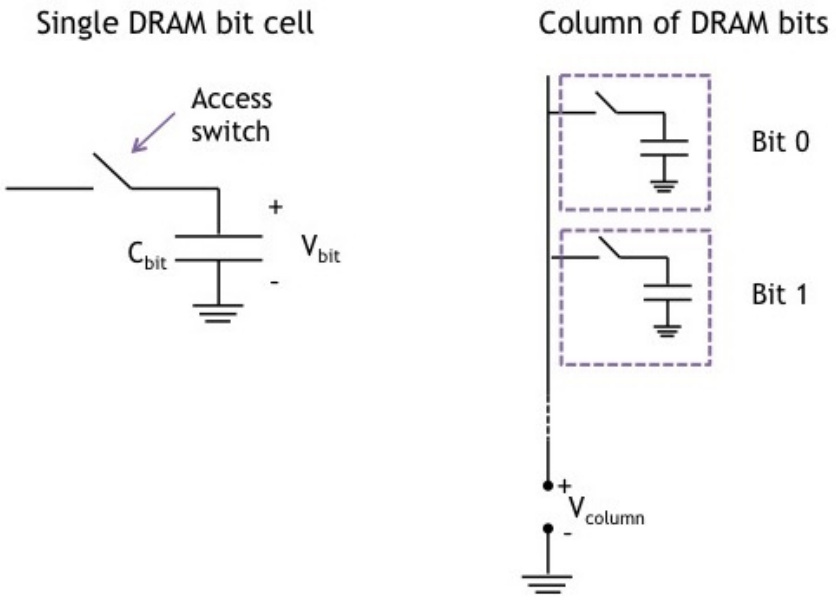
Thus we see that when $V_{\text{init}} \geq \frac{3}{2}V_{\text{min}}$, the parallel configuration is better; otherwise the series configuration is better.

4. Dynamic Random Access Memory (DRAM)

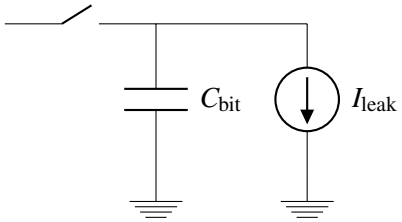
Nearly all devices that include some form of computational capability (phones, tablets, gaming consoles, laptops, ...) use a type of memory known as Dynamic Random Access Memory (DRAM). DRAM is where the "working set" of instructions and data for a processor are typically stored, and the ability to pack an ever increasing number of bits on to a DRAM chip at low cost has been critical to the continued growth in computational capability of our systems. For example, a single DRAM chip today can store > 8 billion bits and is sold for $\sim \$3-5$.

At the most basic level and as shown below, every bit of information that a DRAM can store is associated with a capacitor. The amount of charge stored on that capacitor (and correspondingly, the voltage across the capacitor) sets whether a "1" or a "0" is stored in that location. As also shown below, in order to pack as many bits together as possible on to a single chip, rather than running a massive number of wires to access every single bit of the DRAM individually, the bits are arranged in to a set of columns, where each column uses a single wire to access information from one of the bits; By turning on the access switch within the particular bit cell via the single column wire, the corresponding bit is accessed (while leaving all of the switches in the rest of the cells off).

Building even on only what we've learned about capacitors so far, because of the underlying simplicity of this structure we can understand a lot about how DRAMs work and are designed. Thus, in this problem we will examine some of the issues and tradeoffs that actual DRAM designers deal with when engineering their products.



(a) In any real capacitor, there is always a path for charge to "leak" off of the capacitor and cause it to eventually discharge. In DRAMs the dominant path for this leakage to happen is through the access switch, but let's ignore this for now and assume that this leakage can be modeled as shown below:



This leakage is actually responsible for the "D" in "DRAM" - the memory is "dynamic" because after a cell is written by storing some charge on to its capacitor, if you leave the cell alone for too long, the value you wrote in will disappear because the charge on the capacitor leaked away.

Let's now try to use some representative numbers to compute how long a DRAM cell can hold its value before the information leaks away. Let $C_{\text{bit}} = 18fF$ (note that $1fF = 10^{-15}F$) and the capacitor is initially charged to 1.2V to store a "1". V_{bit} must be > 0.8V in order for the circuits outside of the column to properly read out the bit stored in the cell as "1". What is the maximum value of I_{leak} that would allow the DRAM cell retain its value for $>$ 1ms?

Solution:

We want the time that a cell can read out a '1' to be $t_{\text{store}} = 1ms$. We are given that $V_{\text{init}} = 1.2V$ and $V_{\text{min}} = V_{\text{bit}} = 0.8V$. To get an expression for the leakage rate, we differentiate

$$Q_{\text{bit}} = V_{\text{bit}} C_{\text{bit}}$$

obtaining

$$I_{\text{leak}} = \frac{dV_{\text{bit}}}{dt} C_{\text{bit}}$$

Assuming a constant leakage rate, we have

$$I_{\text{leak}} = \frac{\Delta V_{\text{bit}}}{\Delta t} C_{\text{bit}} \tag{1}$$

$$= \frac{V_{\text{init}} - V_{\text{min}}}{t_{\text{store}}} C_{\text{bit}} \tag{2}$$

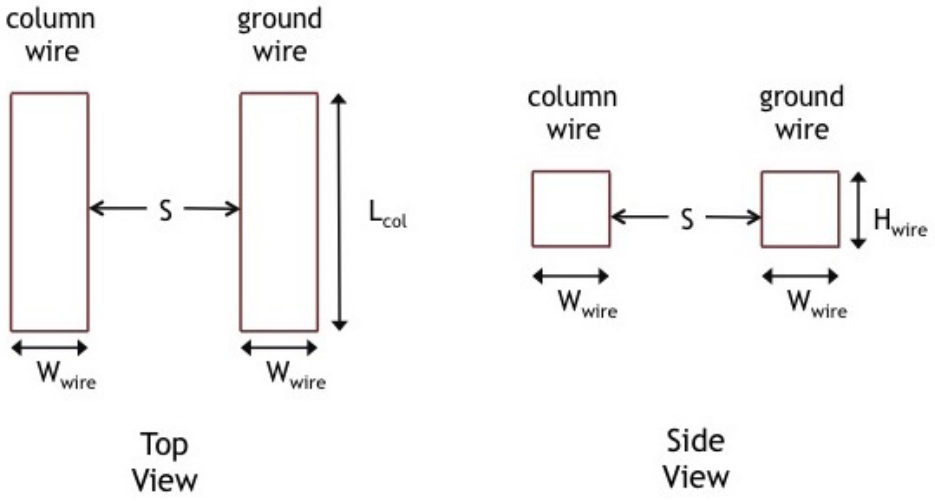
Plugging in the values from above we get

$$I_{\text{leak}} = \frac{(1.2V - 0.8V) \times 18fF}{10^{-3}s} \tag{3}$$

$$= 7.2pA \tag{4}$$

(b) One of the key decisions a DRAM designer has to make is how many cells to include on a single column. Packing more cells on a single column reduces the total number of wires in the chip, saving some chip space and hence cost (chip cost is strongly related to the physical size of the chip), but as we will see next, making the column too long may stop the DRAM from working properly.

Every time we add another DRAM cell on to the column, the wire that connects all of these cells together must get longer. As shown below, the column wire runs next to another wire that is connected to ground (the same ground that is connected to one side of the capacitors in the DRAM cells). This means that the column wire will have some capacitance to ground.



Let's assume that each DRAM cell that gets added also adds an additional length 0.5μm (i.e., 0.5×10^{-6} m) to the column and ground wires. The spacing between the column and ground wires $S = 0.1\mu$m and the height of the wire $H_{\text{wire}} = 0.5\mu$m. If we put 1024 DRAM cells on each column, what is the capacitance between the column wire and the ground wire? Note that you can assume that the two wires are separated by air but in a real chip they would be separated by silicon dioxide, but we'll ignore that for this exercise. You should also assume that all of the capacitance is purely parallel plate. Recall that the capacitance of a two parallel plates separated by air is $C = \frac{\varepsilon A}{d}$, where A is the area of the plate, d is the perpendicular distance between the two plates, and $\varepsilon = 8.854 \cdot 10^{-12} \frac{\text{F}}{\text{m}}$ is the permittivity of air.

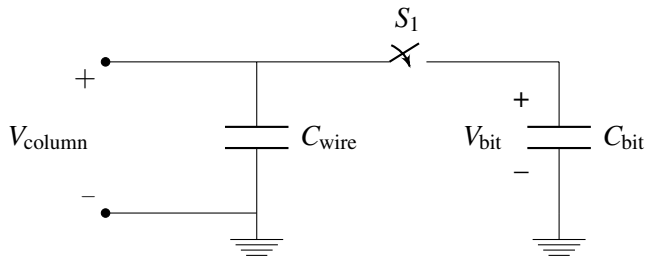
Solution:

Treating this as a purely parallel plate capacitor, we get the following:

$$\begin{aligned} C &= \frac{\varepsilon A}{d} \\ &= \frac{\varepsilon(H_{\text{wire}} L_{\text{col}})}{S} \\ &= \frac{\varepsilon 1024(0.5\times10^{-6})(0.5\times10^{-6})}{0.1\times10^{-6}} \\ &= 22.65fF \end{aligned}$$

(c) In order to read out the value of an individual cell, we turn on the access switch within that cell to connect the capacitor to the column wire, and then read out the resulting voltage on the column wire relative to ground. Note that before this readout operation occurs, the column wire is connected to ground to make sure that its capacitance is discharged, i.e. there is no charge on the wire before it is connected to the capacitor.

The situation described above can be modeled using the circuit shown below; note that for simplicity we will ignore the leakage current and its effects from here on out. If $C_{\text{bit}} = 18fF$, $C_{\text{wire}} = 20fF$ (note this may or may not be your answer to part b), and the DRAM cell has a 0 stored in it (i.e., V_{bit} is set to 0V before S_1 is turned on), what is V_{column} after switch S_1 is turned on (i.e., makes a connection between the capacitor and column wire)? What will V_{column} be in the case that the DRAM cell has a 1 stored in it, meaning the V_{bit} is set to 1.2V before S_1 is turned on?



Solution:

If the cell stores a '0', then V_{column} would be $0V$ because $V_{\text{bit}} = 0V$ initially (before the switch is turned on).

If the cell stores a '1', then V_{column} would be the resultant voltage after the charge sharing has occured. $V_{\text{bit}} = 1.2V$ initially (before the switch is turned on) as the cell stores '1'. The charge corresponding to it is then shared with both the capacitors after the switch is turned on. Let's do this formally. The charge stored in the cell intially is Q_{bit}:

$$Q_{\text{bit}} = C_{\text{bit}} V_{\text{bit}}$$

This charge is now shared between the two capacitors. Thus we get

$$Q_{\text{bit}} = C_{\text{bit}} V_{\text{bit}} = (C_{\text{bit}} + C_{wire}) V_{\text{column}}$$
$$\frac{C_{\text{bit}}}{(C_{\text{bit}} + C_{wire})} V_{\text{bit}} = V_{\text{column}}$$
$$\frac{18}{38} V_{\text{bit}} = V_{\text{column}}$$
$$V_{\text{column}} = 0V \text{ if } V_{\text{bit}} = 0V$$
$$V_{\text{column}} = 0.568\text{V} \text{ if } V_{\text{bit}} = 1.2V$$

(d) The minimum voltage the readout circuit needs to reliably detect a "1" in a DRAM cell is 0.4V. Considering $C_{\text{bit}} = 18fF$, and using the same dimensions provided in part b) for the wires, what is the maximum number of cells that can be stacked together on to a single DRAM column while still meeting this minimum voltage requirement for the readout?

Solution:

Noting from the above that V_{column} depends on a ratio of C_{bit} and C_{wire}, we can substitude the minimum value required for successful readout V_{min} and solve for the maximum allowable C_{wire}:

$$\frac{18fF}{18fF + C_{\text{wire,max}}} V_{\text{bit}} = V_{\text{min}}$$
$$\frac{18fF}{18fF + C_{\text{wire,max}}} 1.2V = 0.4V$$
$$\frac{1.2}{0.4} 18fF = (18fF + C_{\text{wire,max}})$$
$$36fF = C_{\text{wire,max}}$$

After finding the maximum value for C_{wire}, we can use the solution from (b) to calculate the maximum number of cells n.

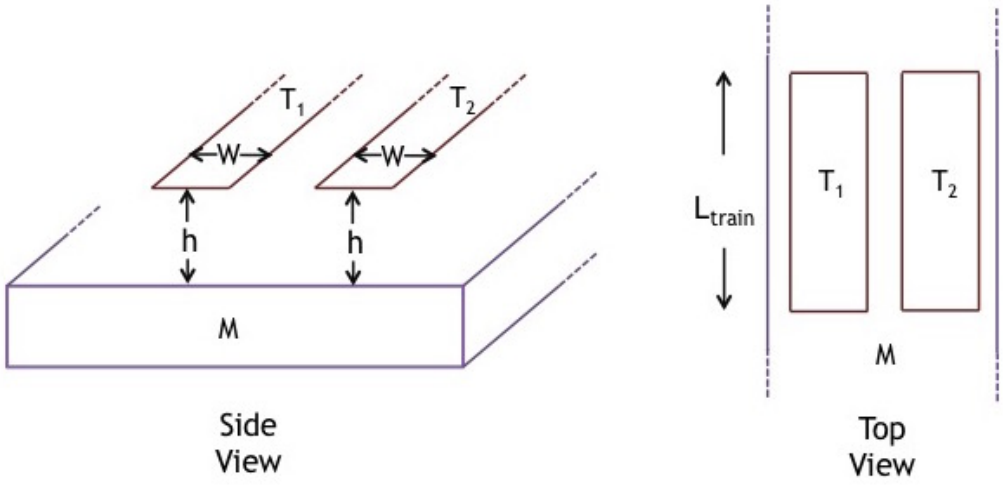
$$36 \times 10^{-15} = \frac{\varepsilon n (0.5 \times 10^{-6})(0.5 \times 10^{-6})}{0.1 \times 10^{-6}}$$
$$36 \times 10^{-9} = 2.5(n)\varepsilon$$
$$n = 1626$$

Note: Real DRAMs do things slightly differently in terms of the voltage they initially set the column wire to but use the same basic concept as described above.

5. Mag-lev Train Height Control System

One of the fastest forms of land transportation are trains that actually travel slightly elevated from ground using magnetic levitation (or "mag-lev" for short). Ensuring that the train stays at a relatively constant height above its "tracks" (the tracks in this case are what provide the force to levitate the train and propel it forward) is critical to both the safety and fuel efficiency of the train. In this problem we'll explore how we can use ideas very similar to the capacitive touchscreen we learned about in class (and in the lab) to realize such a height control system. (Note that real mag lev trains may use completely different and much more sophisticated techniques to perform this function, so if you e.g. get a contract to build such a train you'll probably want to do more research on the subject.)

(a) As shown below, let's imagine that all along the bottom of the train, we put two parallel strips of metal (T_1, T_2), and that on the ground below the train (perhaps as part of the track) we have one solid piece of metal (M).



Assuming that the entire train is at a uniform height above the track and ignoring any fringing fields (i.e., all capacitors are purely parallel plate), as a function of L_{train} (the length of the train), W (the width of T_1/T_2), and h (the height of the train off of the track), what is the capacitance between T_1 and M? How about the capacitance between T_2 and M?

Solution:

The distance between the plates (T_1 & M or T_2 & M) is h. The area of plate for the parallel plate capacitor is $A = WL_{\text{train}}$, thus using the formula for capacitance of a parallel plate capacitor we get:

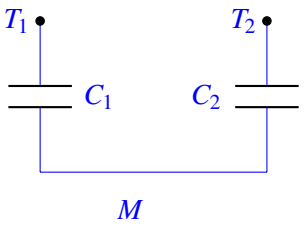
$$C = \frac{\varepsilon A}{d}$$

$$C_1 = \frac{\varepsilon W L_{\text{train}}}{h} \text{ (Capacitance between } T_1 \text{ and M)}$$

$$C_2 = \frac{\varepsilon W L_{\text{train}}}{h} \text{ (Capacitance between } T_2 \text{ and M)}$$

(b) Any circuit on the train can only make direct contact at T_1 and T_2. To detect the height of the train, it would only be able to measure the effective capacitance between T_1 and T_2. Draw a circuit model showing how the capacitors between T_1 and M and between T_2 and M are connected to each other.

Solution: The capacitors C_1 and C_2 are in series; to realize this, lets consider the train circuit which is in contact with T_1 and T_2. If there is current entering the plate T_1 the same current has to exit plate T_2. Thus the circuit can be modeled as follows:



(c) Using the same parameters as in part (a), provide an expression for the capacitance between T_1 and T_2.

Solution:

Since the two capacitors are in series, the effective capacitance between T_1 and T_2 is given by

$$\frac{1}{C_{\text{eff}}} = \frac{1}{C_1} + \frac{1}{C_2}$$

Thus we get

$$\frac{1}{C_{\text{eff}}} = \frac{h}{\varepsilon W L_{\text{train}}} + \frac{h}{\varepsilon W L_{\text{train}}}$$

$$C_{\text{eff}} = \frac{\varepsilon W L_{\text{train}}}{2h}$$

(d) Let's assume that instead of just detecting the height (by measuring the capacitance between T_1 and T_2), we also want to control it. Let's assume that the device we use to control the height takes in only one of only two commands: increase the height, or decrease the height. In particular, this device is controlled by an input voltage. If that voltage is 5V it will push the train higher above the track, and if it is 0V it will let the train move down closer to the track.

Assuming that the train is 100m long ($L_{\text{train}} = 100\text{m}$) and that the T_1/T_2 metals are each 1cm wide ($W = 1\text{cm}$), design a circuit that will drive the control device to make the train levitate 1cm above the track. Be sure to show how you circuit is connected to T_1 and T_2, and be as specific as possible in terms of the component values you would use. You can use any combination of switches, voltage sources, current sources, resistors, and op-amps you would like to implement this circuit.

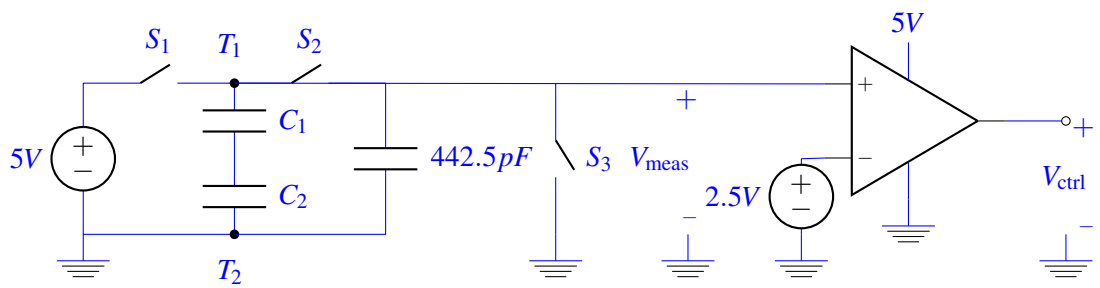
Solution:

The effective capacitance between T_1 and T_2 is inversely proportional to the height of the train. We are only allowed to measure the effective capacitance between T_1 and T_2, we can measure what the capacitance is to figure out what h is. Based on whether h is lower or higher, we can construct a circuit using comparators and switches and capacitors (to figure out whether capacitance and thus height is above or below the desired height) whose output can then drive the height controller mechanism.

First lets figure out what C_{eff} should be at the desired height:

$$C_{\text{eff}} = 8.85pF/m \times \frac{100m \cdot 10^{-2}m}{200^{-2}m} = 442.5pF$$

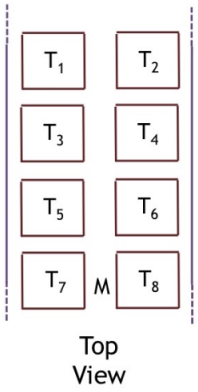
Let's use the same circuit as the touchscreen lab to measure C_{eff}. (Note that there are many other circuits that can measure the capacitance as well. Any consistent & functioning solution will receive full credit.)



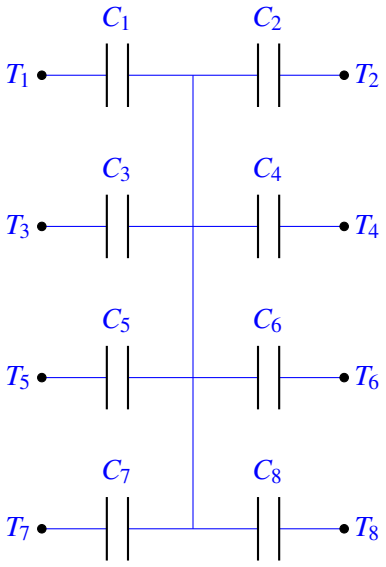
If the train is higher than it is supposed to be (which is $1cm$), then $C_{\text{eff}} < 442.5pF$. After charge sharing with the fixed $442.5pF$ capacitor, V_{meas} will therefore be $< 2.5V$, so $V_{\text{ctrl}} = 0V$ and the control device moves the train down. $442.5pF$ was chosen for the fixed capacitor so that the choice of V_{ref} will be $2.5V$ (which is a nice indicator if the height is below or above the threshold as the initial charging voltage is $5V$). Similarly, if the train is lower than it is supposed to be then $V_{\text{meas}} > 2.5V$, so $V_{\text{ctrl}} = 5V$ and the control device moves the train up.

(e) So far we've assumed that the height of the train off of the track is uniform along its entire length, but in practice this may not be the case. Suggest and sketch a modification to the basic sensor design (i.e., the two strips of metal T_1/T_2 along the entire bottom of the train) that would allow you to measure the height at the train at 4 different locations.

Solution:



One important thing to note about this circuit is that it works only if extra care is taken during the capacitance measurement circuit. The equivalent model for this is:



So the circuit needs separate switches on each T so that you can measure the capacitance between only two terminals (like T_1 & T_2) and the effect of other capacitors is nullified.

6. **Your Own Problem** Write your own problem related to this week's material and solve it. You may still work in groups to brainstorm problems, but each student should submit a unique problem. What is the problem? How to formulate it? How to solve it? What is the solution?