EHD-Lab1 (4th August 2018)

1) Design a Half Adder (HA), Full Adder (FA) and a 4-bit Ripple Carry Adder (RA) using Verilog. Use structural modeling. Design Sequence: Create HA module first and use it to create FA module. Use FA modules to create the 4-bit Ripple Carry Adder.
2) Write a test bench and validate the design by simulation.

Please submit the Verilog code, the testbench and the waveforms for all the three (HA, FA, RA) after zipping them into a folder named with your rollnumber.zip.