EHD_Report for Lab_2

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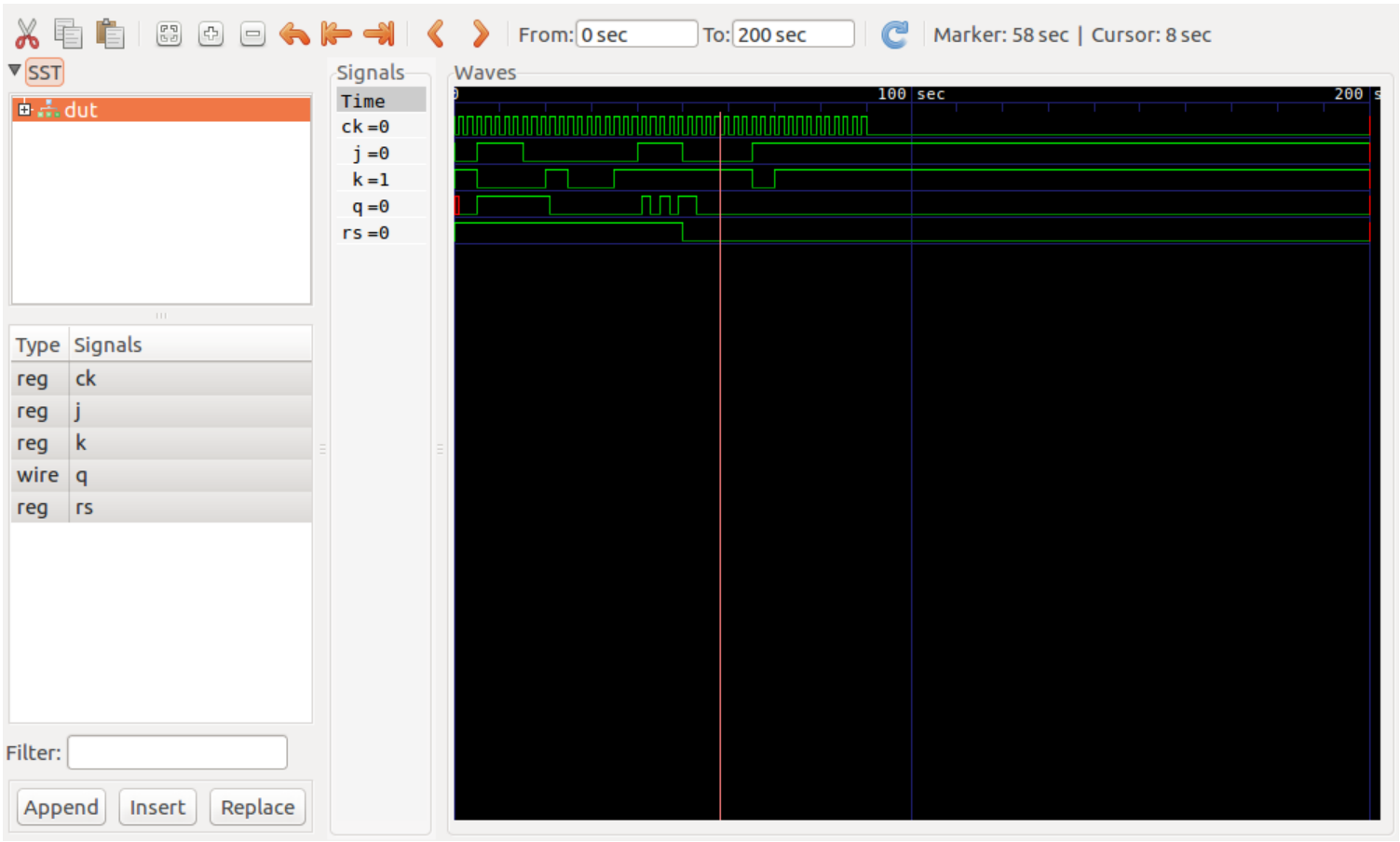
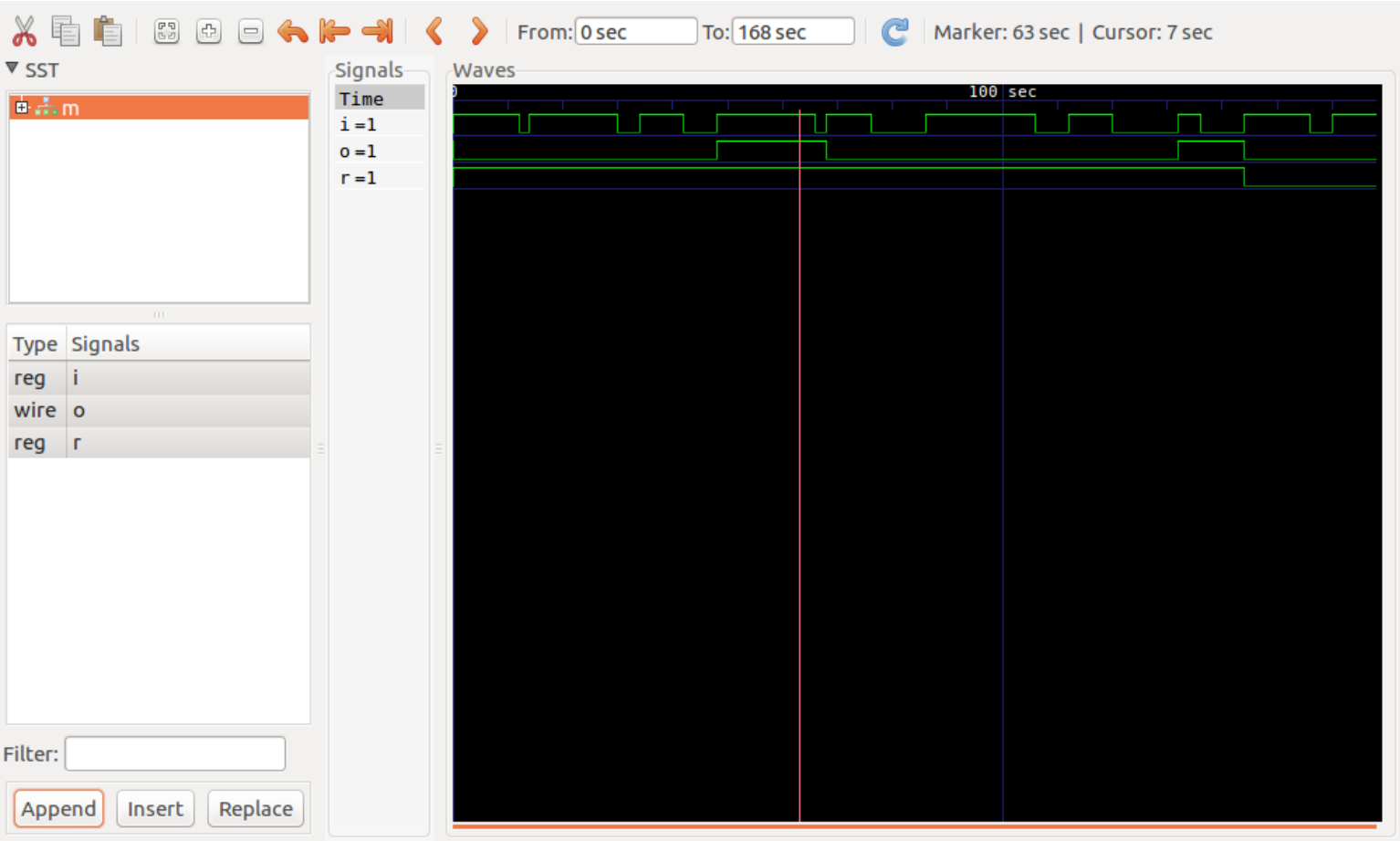
Roll: 2018122004
UG2 – ECD



The above image shows the respective jkff output
reset is considered active low



The above image is the pulse divide by 4 circuit
At every 4th rising clock edge, the output changes to 1 from 0 and stays like that for one clock cycle.