Embeddee Hardware Design

Lab_4 : 4 bit multiplier with pipeline

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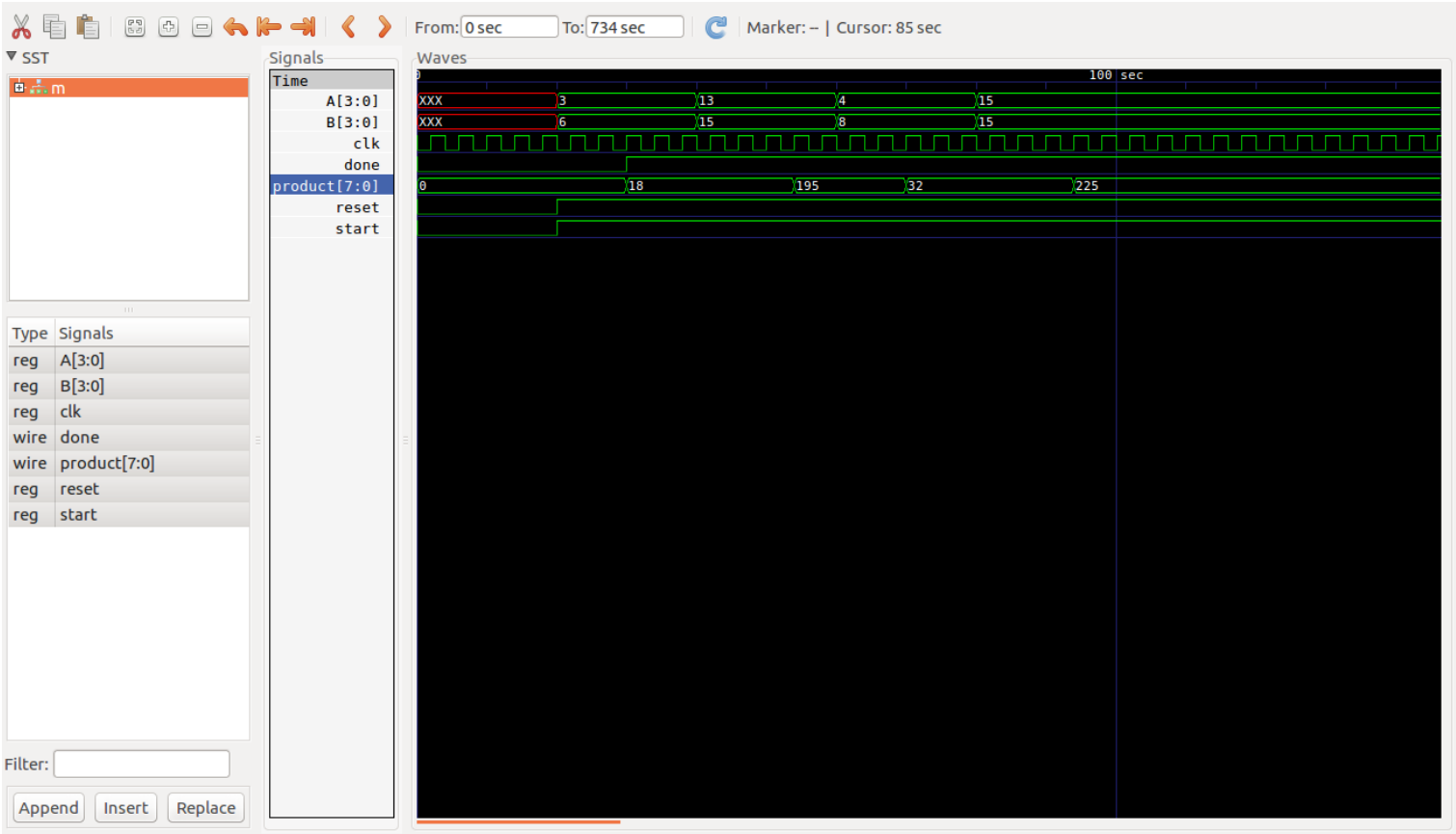
2018122004



Initially, the inputs are not loaded.
Once, start is high and reset is high(active low), at posedge of clk, the inputs are loaded.
Done is Zero initially, Once the multiplication is done, Done = 1

Here, there are three stages of pipeline which uses arrays of registers.
There are 2 states.
State 1 is initially 0
State 1 becomes one after first pipeline(storing in reg array) is done.

State 2 is initially 0
State 2 becomes one after second pipeline(storing in reg array) is done.

State 1 is made zero when state 2 starts so that the next inputs can get in the state 1.