

Synthesis and Implementation

Shivani Chepuri
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Adder (full_1bit):

Slice Logic:

LUT - 53200(available) 1(used) <0.01% utilization

Registers - 106400(av) 0(used) 0.00% utilization (both after synth and impl)

IOB – 5(used) 200(av) 2.50% utilization;

Primitives: Ibuf-3 Obuf-2 LUT3 – 2

Timing: Not using a clk(setup,hold,pw times are NA)

LUT utilization: 1% I/O utilization: 2.5%

Total reg = 0

DSPs = 0

Power: Total on-chip power 1.023W

Junction Temperature: 36.8 oC

Thermal Margin: 48.2oC (4.0 W)

Dynamic Power: 0.903

Total Device Static Power: 0.120

On-chip signals: 5

Multiplier:

Slice Logic:

LUT - 53200(available) 30(used) 0.05% utilization

Registers - 106400(av) 42(used) 0.04% utilization (both after synth and impl)

IOB – 9(used) 200(av) 4.50% utilization;

DSPs = 0

Timing:

Worst Negative Slack: 2.852 ns

Worst Hold Slack: 0.014

Total End Points: 72

Power: Total on-chip power 0.103W

Junction Temperature: 26.2 oC

Thermal Margin: 58.8oC (4.9 W)

Dynamic Power: 0.051

Total Device Static Power: 0.052

GCD:

Slice Logic:

LUT - 53200(available) 168(used) 0.32% utilization

Registers - 106400(av) 131(used) 0.12% utilization (both after synth and impl)

IOB – 100(used) 200(av) 50% utilization;

Timing:

Worst Negative Slack: 0.942 ns

Worst Hold Slack: 0.204 ns

Total End Points: 193

DSPs = 0

Power: Total on-chip power 1.03W

Junction Temperature: 28.6 oC

Dynamic Power: 0.04

Thermal Margin: 58.2oC (4.9 W)

Total Device Static Power: 0.99

Divider:

Slice Logic:

LUT - 53200(available) 31(used) 0.06% utilization

Registers - 106400(av) 24(used) 0.03% utilization (both after synth and impl)

IOB – 19(used) 200(av) 9.50% utilization;

Timing:

Worst Negative Slack: 1.831

Worst Hold Slack: 0.85

Total End Points: 39

DSPs = 0

Power: Total on-chip power 0.108W

Junction Temperature: 36.3 oC

Dynamic Power: 0.007

Thermal Margin: 39.2oC (4.0 W)

Total Device Static Power: 0.101