EHD_Report for Lab_0

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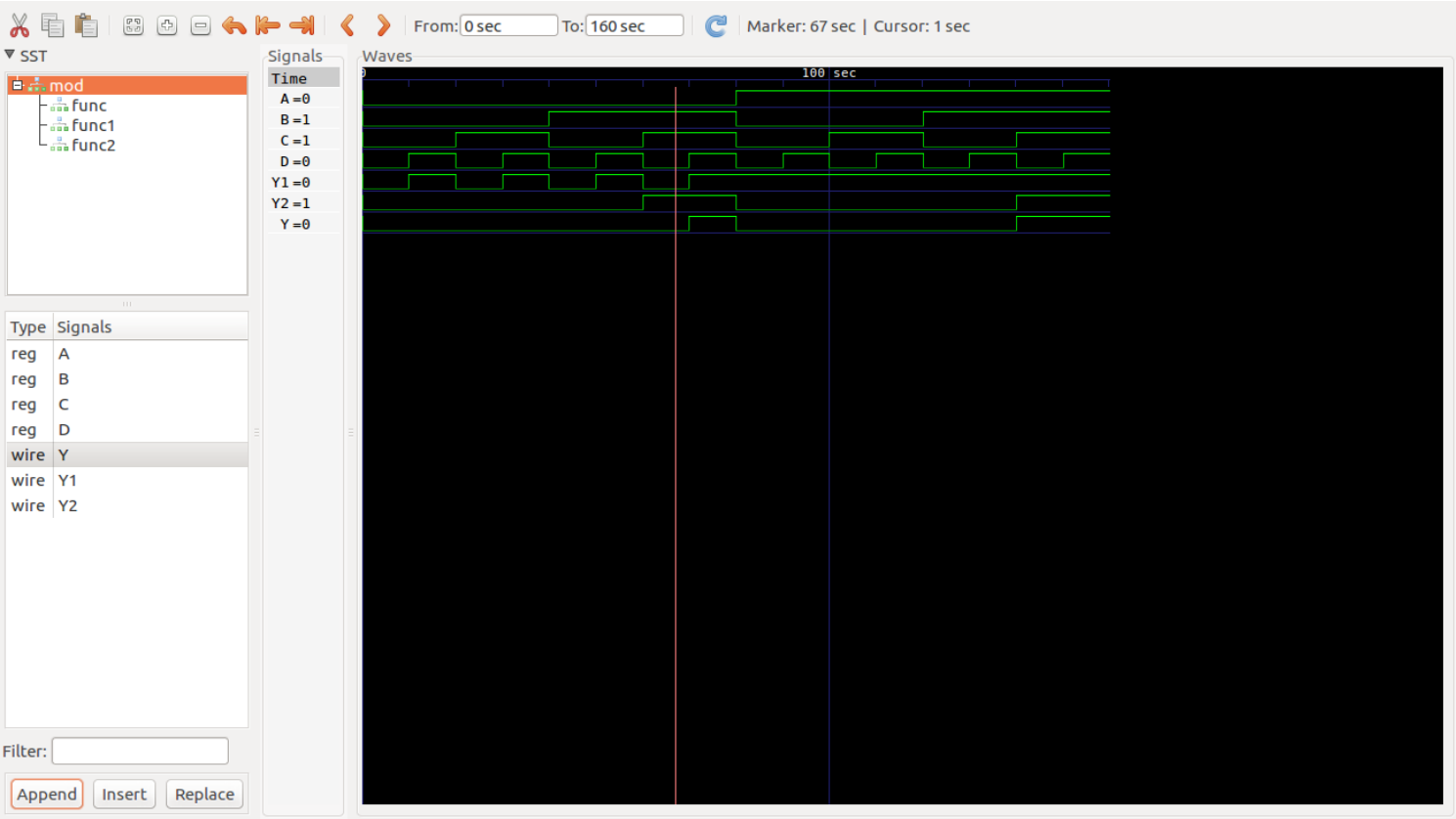
Roll: 2018122004
UG2 – ECD



The above image is the output wave form of the verilog file test.v which uses muxfile.v to instantiate 3 2:1 muxes and evaluates the Boolean Function BC(A+D), the reduced form of the given boolean equation.

A,B,C,D are the inputs; Y1,Y2 are intermediate outputs of mux1 and mux2 respectively.

Y = BC(A+D) is being plotted for the respective A,B,C,D inputs at each instant of time.