Framework of Cache Architecture

Key Contribution:

- Designing Parameterized cache simulator with complete hierarchy of cache memory in single core processor and then extending to multi core processors.
- Input is two files: Configuration File and Trace File and Output will be Hit Rate according to that configuration FIle.
- Compare between outputs generated if different configurations are tested with same trace file.
- Configuration File has following parameters:
  - Cache Size
  - Block Size
  - Associativity

Assumption:

- Associativity : 2,4,8,16
- Block Size(in word) : 1,2,4,8,16
- Cache Size (max values)
  - L1 - 64KB
  - L2 - 256 KB
  - L3 - 4MB
- Byte Addressable Memory - Each address has 8 bit of data
- Physical memory address is 32 bit wide.
- No of Ways = No of BRAMs
- No of sets = No of lines in each BRAM

Methodology: (in Verilog)

- Building cache using BRAM present on FPGAs.
- As we cannot parameterize the size of BRAM, we have designed BRAM of max size.
  - Depth of BRAM: Depends on max no of sets.
  - Width of BRAM: Valid bit + Tag Bit + Data (Depends on max tag width and max block size)
- Max Set:

  $= MaxCacheSize/(MinBlockSize * MinAssociativity)$

  $= (2^6 * 2^{10})/(2^2 * 2)$

  $= 2^{13}$

- Max Tag:
  - To calculate max tag, we take min set and min block offset bits.

TAG	SET	BLOCK OFFSET
29	1	2

- Max Data Block:
  - To calculate max data block, we take max block size (16 words)

    $= 16 * 4 * 8 \; bits$

    $= 512 \; bits$

- Depth of Block Ram: $0 \; to \; 2^{13} - 1$
- Width of Block Ram: $512 + 29 + 1 = 542 \; bits$

Way 0	Valid Bit [1]	Tag Bits [29]	Data Bits [512]
Set 0			
Set 1			
.			
.			
.			
Set 8191			