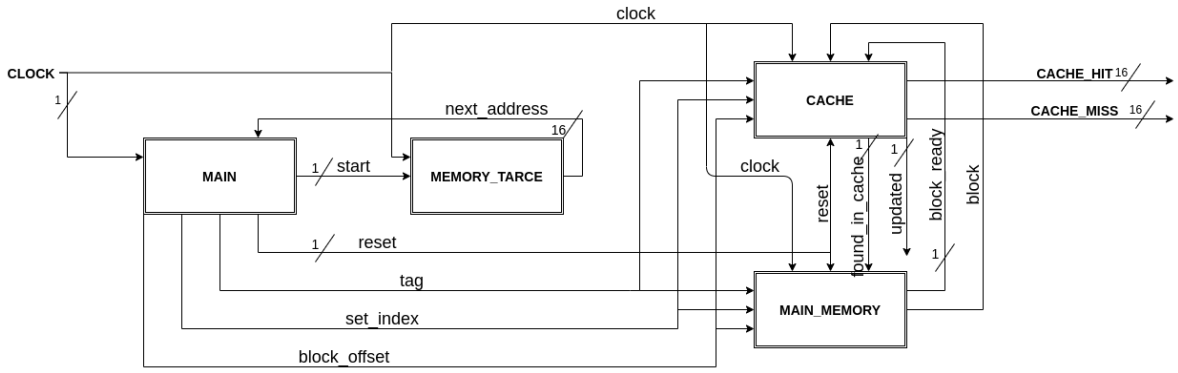
Comparison of Different Cache Architecture

Block diagram of cache architecture



Brief configuration of Cache Architectures

1. Cache_BlockRAM
    - Cache model is designed using BlockRams present on FPGA
    - Direct mapped cache with block size 4 word and cache size 32KB

2. Cache_Regbank
    - Cache model is designed using registers as reg bank
    - Direct mapped cache with block size 4 word and cache size 32KB

3. Cache_BlockRAM_Regbank
    - Cache model is designed using BlockRams and registers.
        - BlockRams is L1 cache which is direct mapped (block size 4 word and cache size 32KB)
        - Reg bank cache is like L0 cache which is fully associative (currently 16 line each of 169 bit wide)
        - So, first data will be checked in this flow

          L0 - yes - cache_hit (with x latency)

          no - go to L1

          L1 - yes - cache_hit (with y latency (y>x))

          So, this cache line is then stored in L0

          no - cache_miss go to memory (with z latency (z>y>x))

          So, this memory block is then stored in L1

Resource Utilization Summary

RESOURCE	CACHE BLOCKRAM	CACHE REGBANK	CACHE BLOCKRAM_REGBANK	AVAILABLE
LUT	1512	2399	1700	53200
LUTRAM	182	1107	147	17400
FF	2407	2359	3071	106400
BRAM	38	32	38	140
IO	1	1	1	200

Power Report Summary

POWER COMPONENTS	CACHE BLOCKRAM	CACHE REGBANK	CACHE BLOCKRAM_REGBANK
Clocks (W)	0.011	0.012	0.012
Signals (W)	0.001	0.012	0.006
Logic (W)	0.001	0.002	0.002
BRAM (W)	0.040	0.022	0.034
I/O (W)	<0.001	<0.001	<0.001
Static (W)	0.105	0.105	0.105
Total (W)	**0.158**	**0.153**	**0.158**

Hit/Miss Latency Summary

	CACHE BLOCKRAM	CACHE REGBANK	CACHE BLOCKRAM_REGBANK
Hit latency (Clock Cycles)	4	1	FIRST HIT - 4 REST - 1
Miss latency (Clock Cycles)	20	20	20