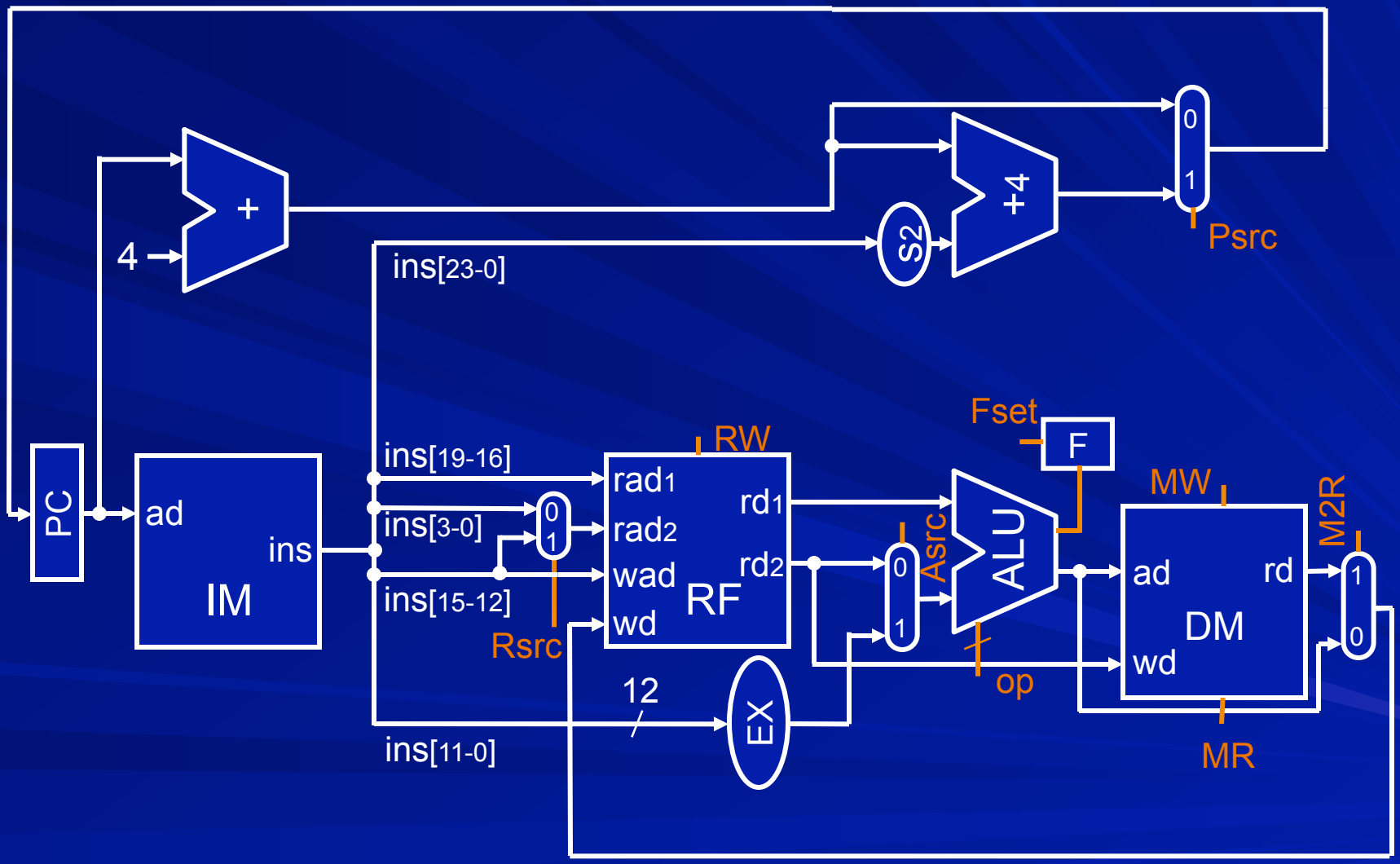
COL216
Computer Architecture

Processor design -
Simple design continued
7th March, 2016

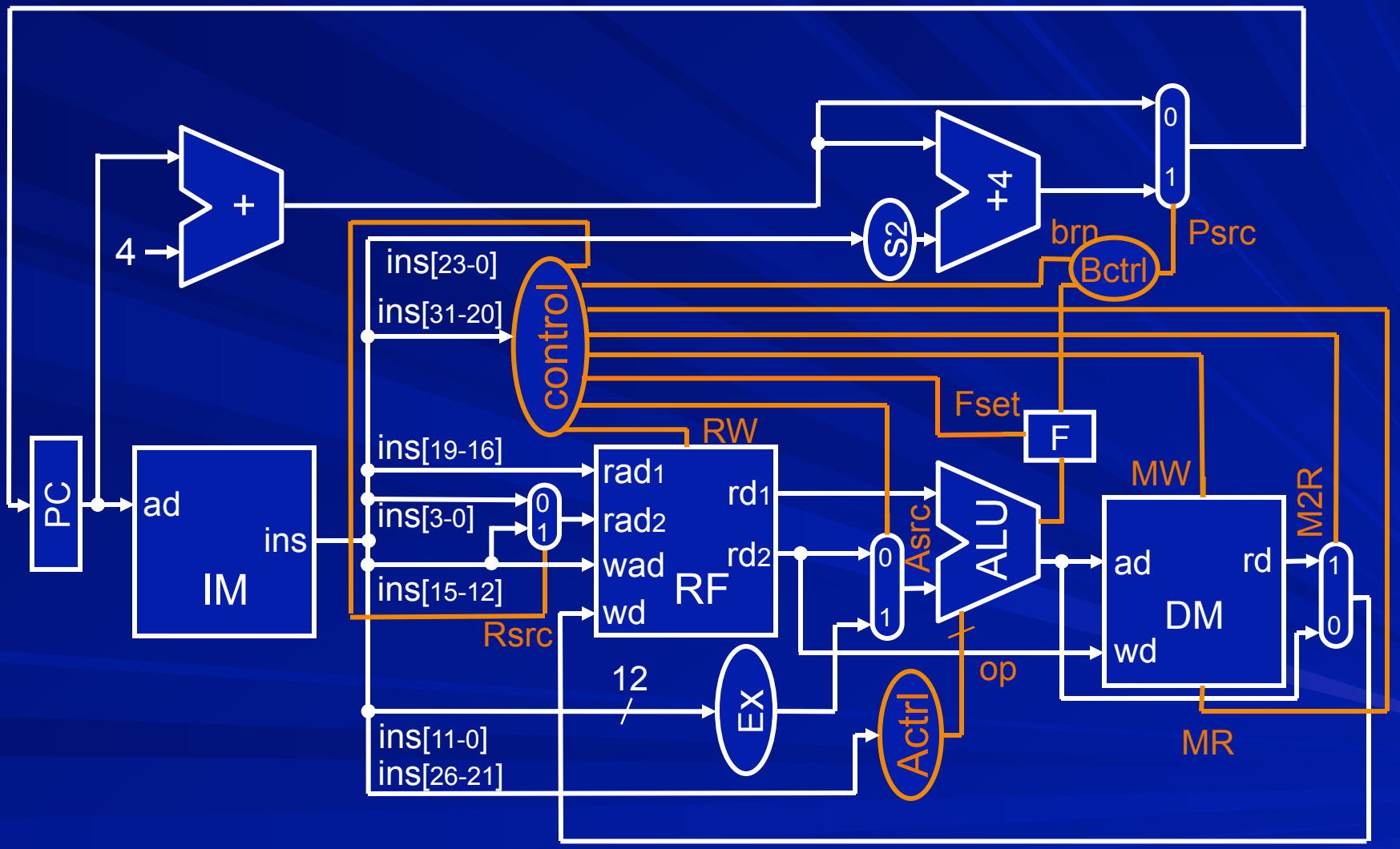
Outline of this lecture

- Define control inputs for various instructions
- Build truth tables for controllers

Control Signals (from last lecture)



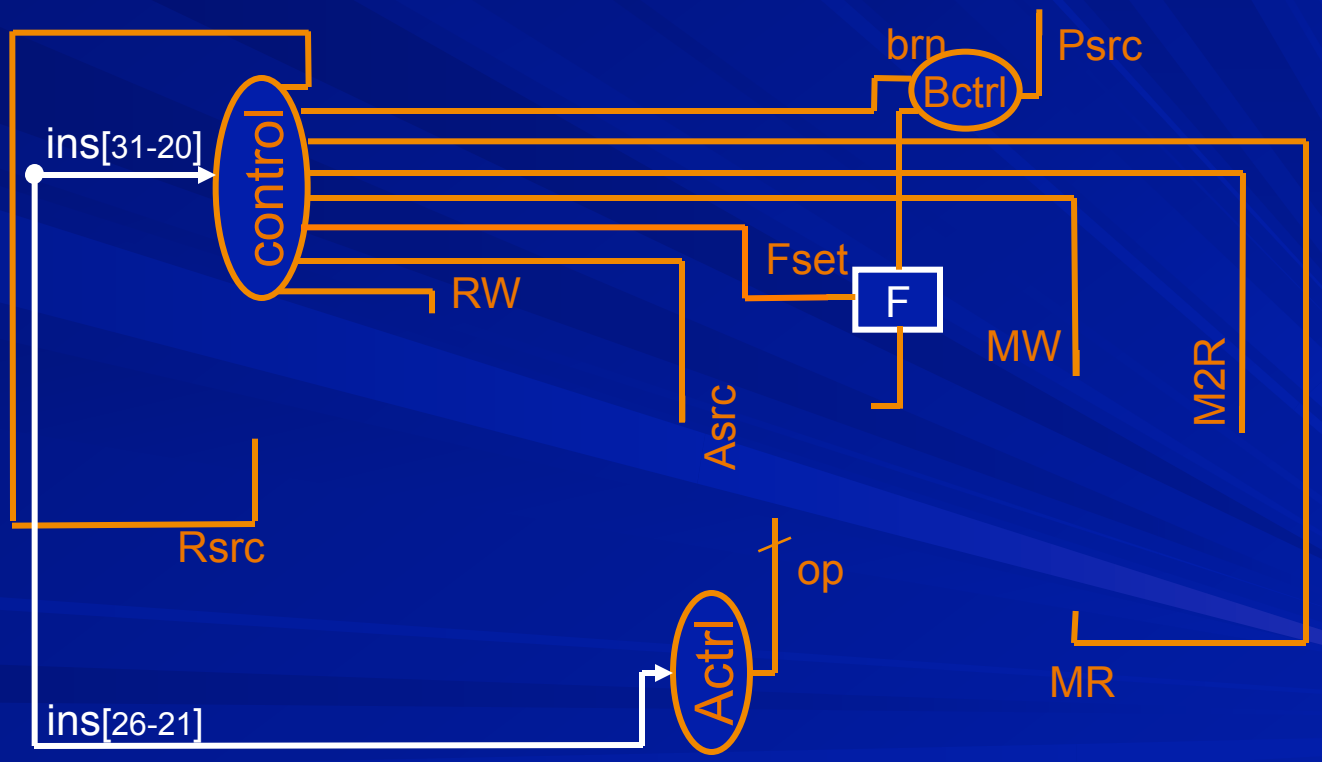
Datapath + Control (from last lecture)



Controller has 3 parts

1. Actrl looks at ‘opc’ field (for DP instructions) and ‘U’ field (for DT instructions) to generate control signals for ALU
2. Bctrl generates control signal Psrc for PC input multiplexer. Psrc = 1 if and only if the instruction is a branch instruction and flags satisfy the condition specified by ‘cond’ field
3. Main controller generates control signals (Rsrc, Asrc, M2R) for other multiplexers and control signals (RW, MR, MW, Fset) for state elements (RF, DM, F)

Controller without showing datapath

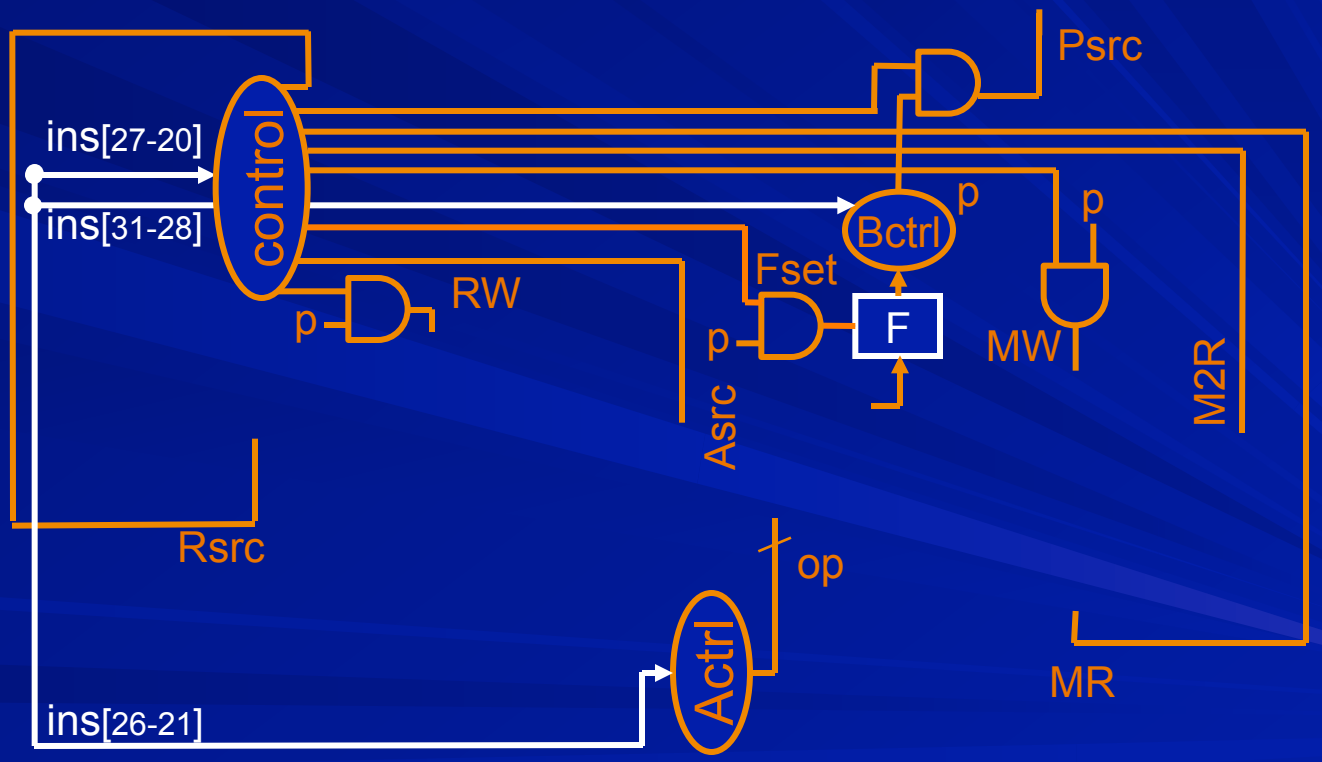


Extending the design for predication

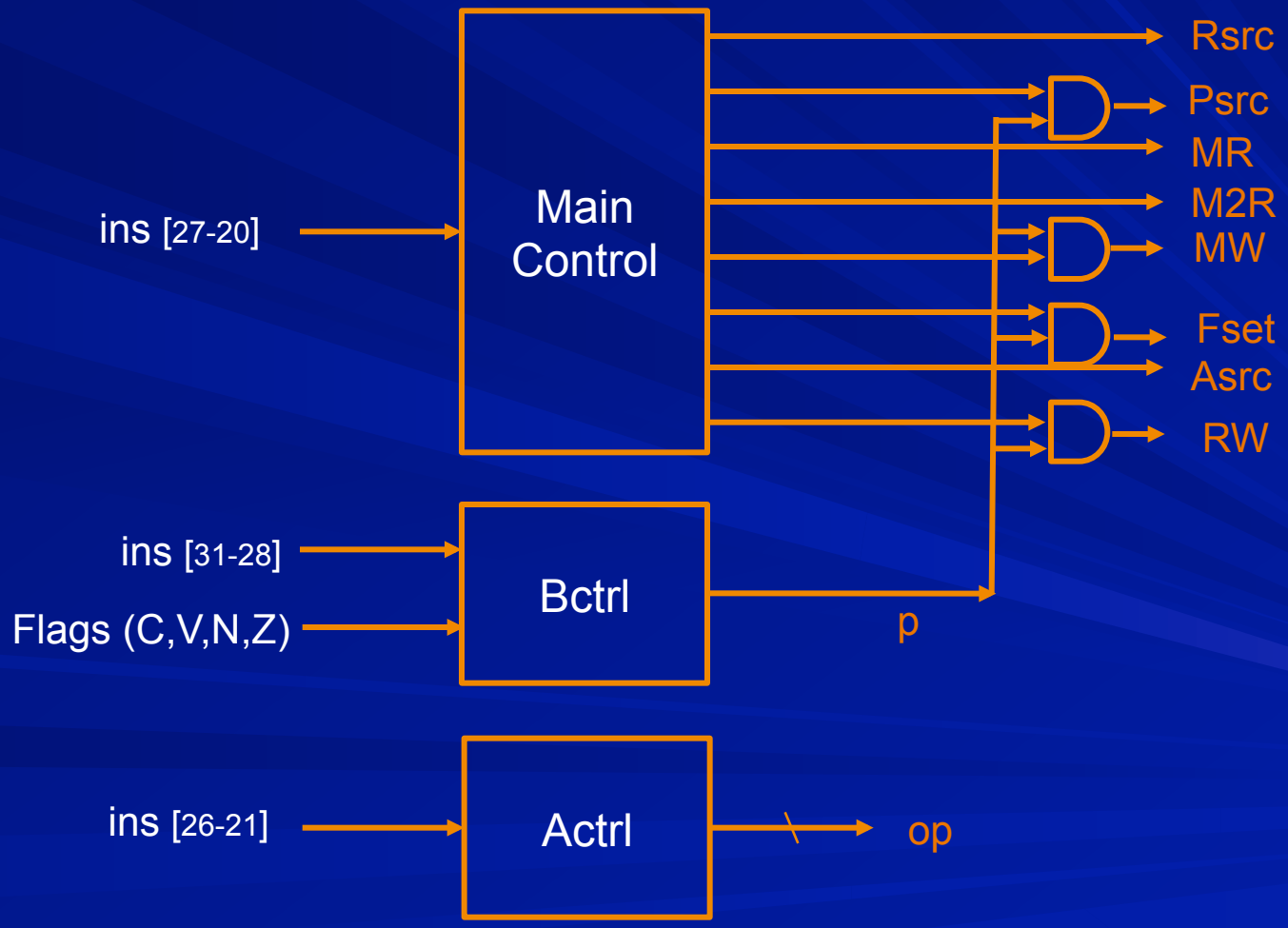
- Currently, Bctrl is designed to take care of conditional branches only. Its logic is as follows
- A slight modification of Bctrl takes care of predication in other instructions as well
- Now Bctrl produce a signal p which is 1 if and only if the condition specified by the ‘cond’ field is satisfied by the flags
- Psrc is conjunction (AND) of p and a signal from the main controller that it is a branch instruction
- Similarly, RW, MW and Fset are conjunction of p with appropriate signals from the main controller

Controller for predication

The main controller now needs to look at the bits ins [27-20] only

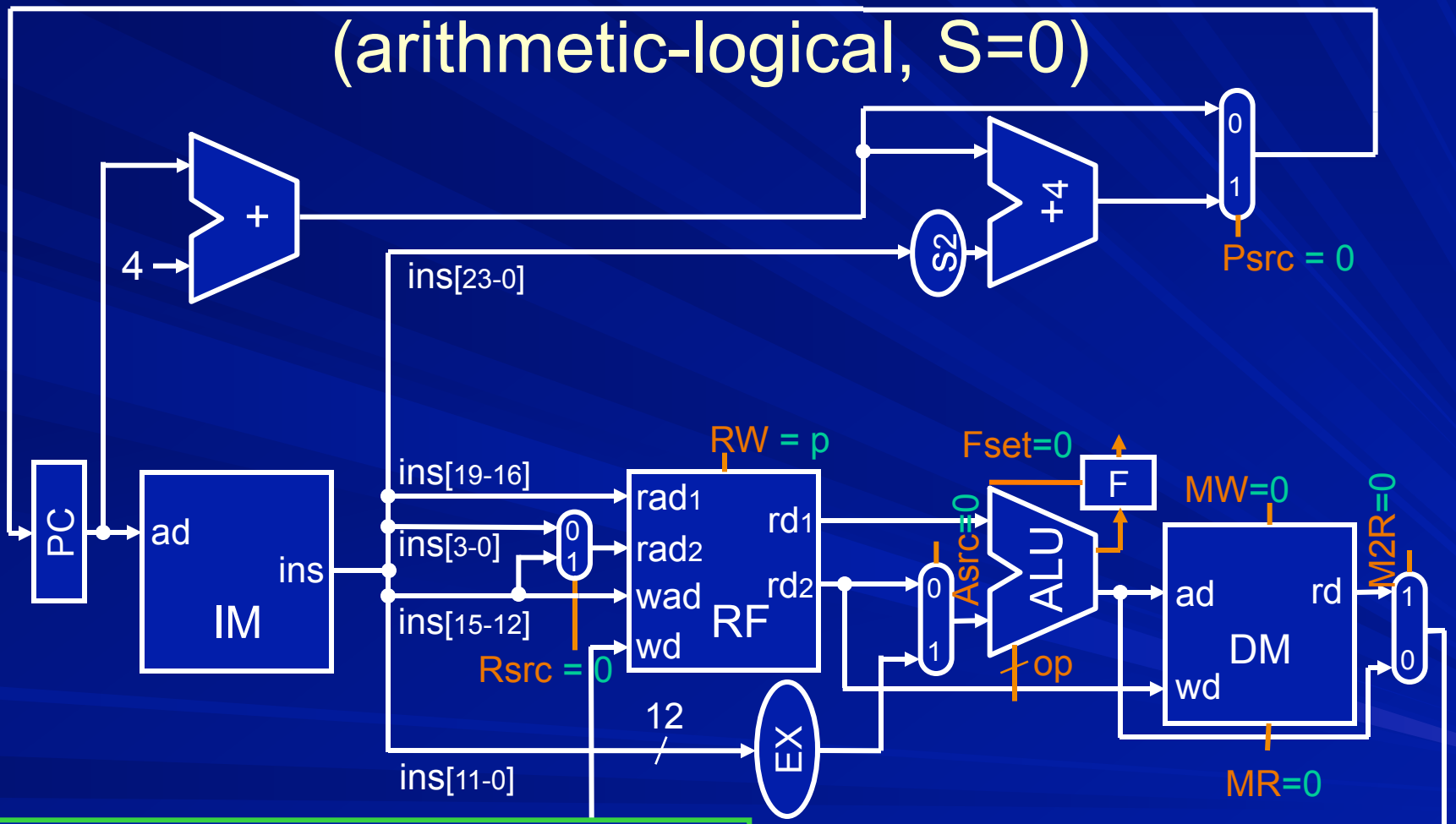


Controller structure



Control Inputs for DP instructions

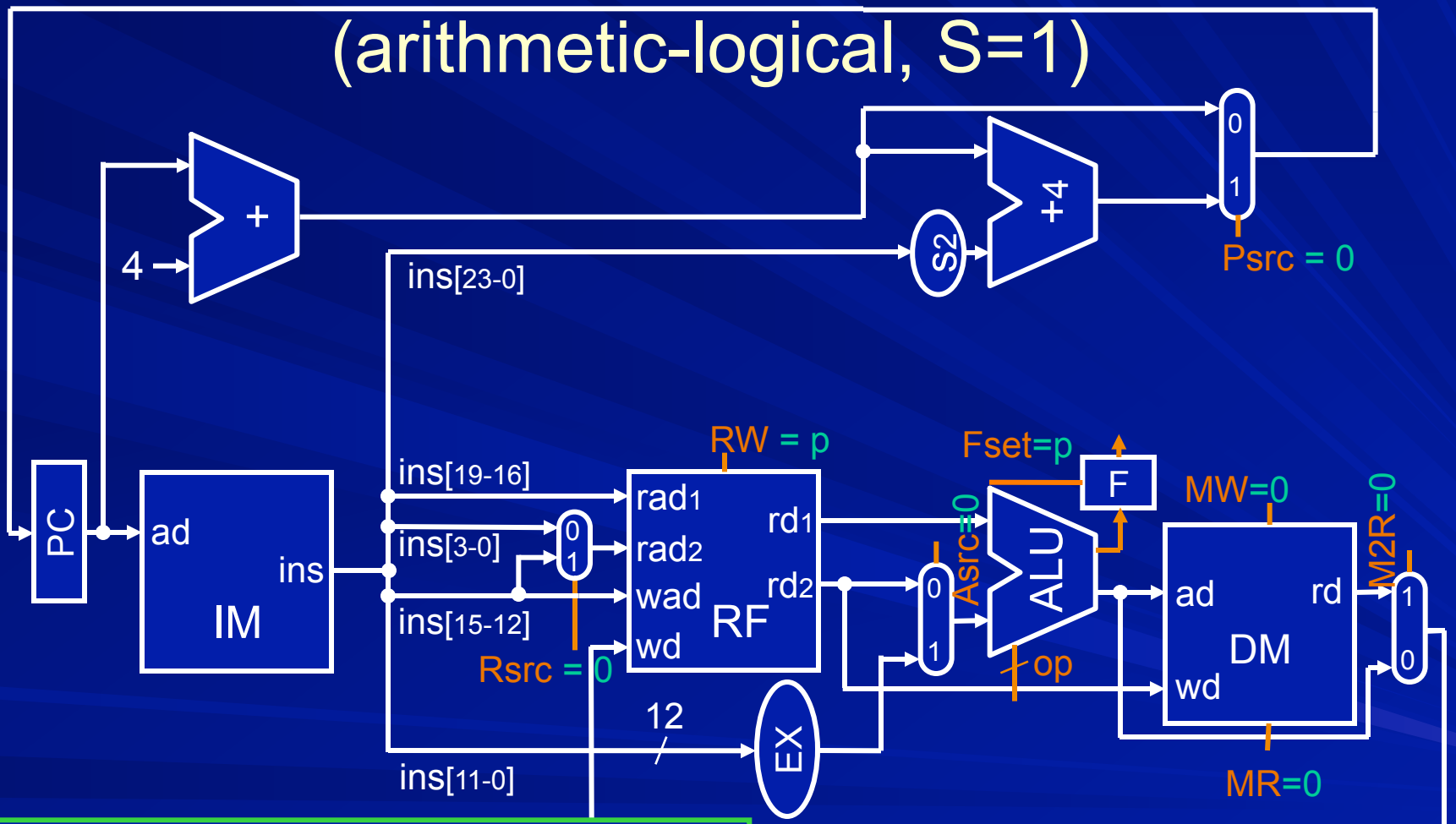
(arithmetic-logical, S=0)



Rsrc	RW	Asrc	MW	MR	M2R	Psrc	Fset
0	p	0	0	0	0	0	0

Control Inputs for DP instructions

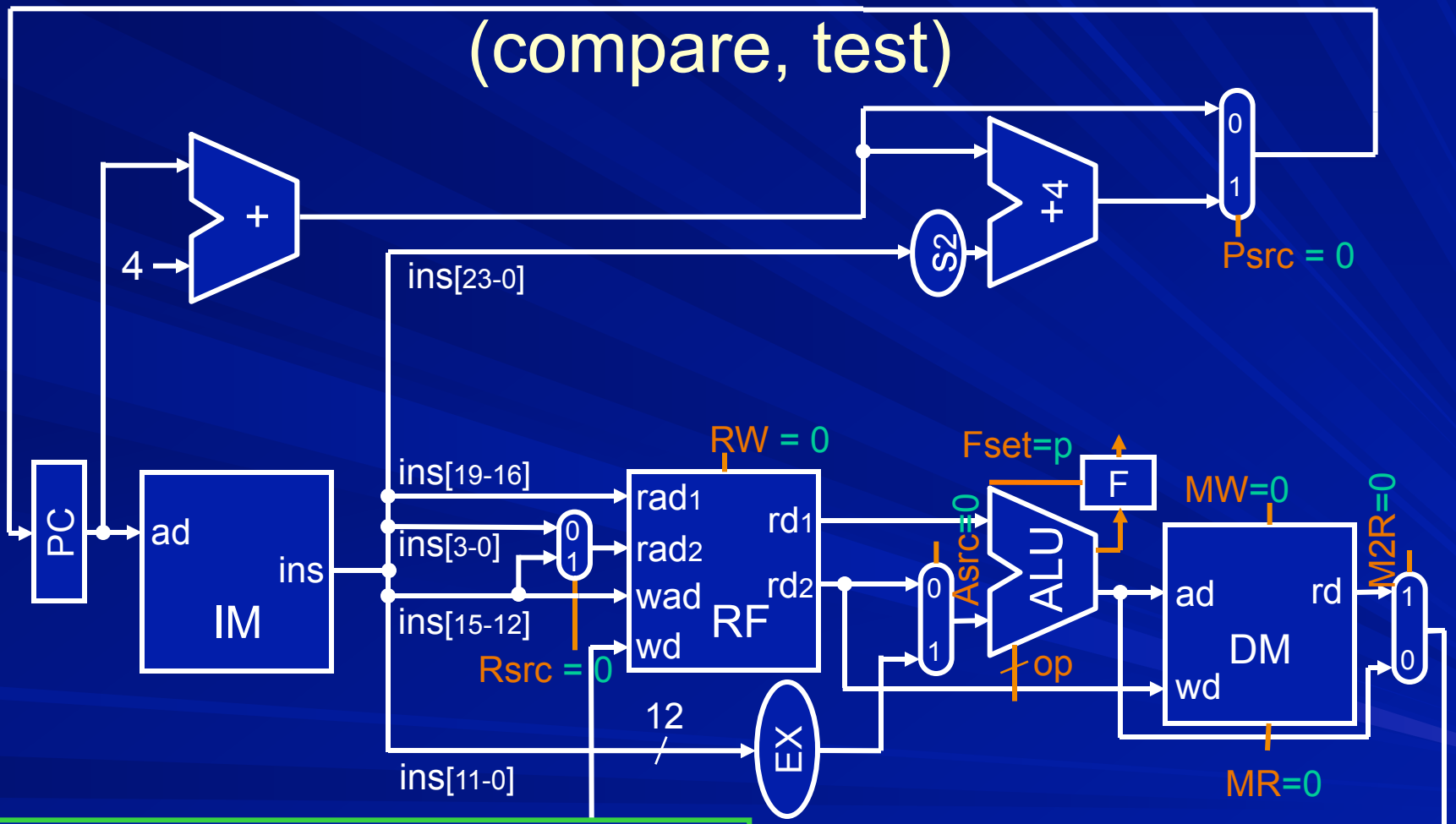
(arithmetic-logical, S=1)



Rsrc	RW	Asrc	MW	MR	M2R	Psrc	Fset
0	p	0	0	0	0	0	p

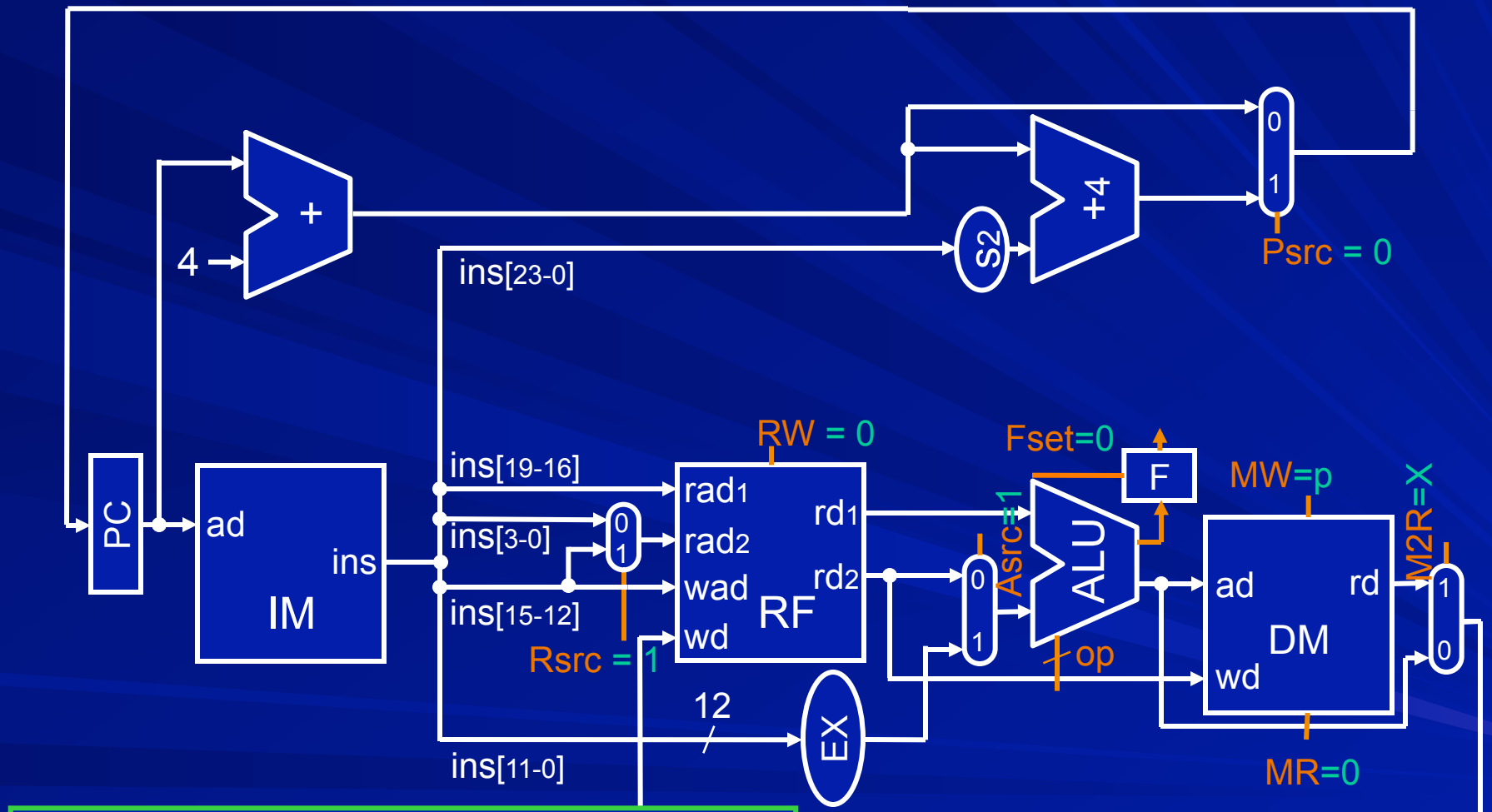
Control Inputs for DP instructions

(compare, test)



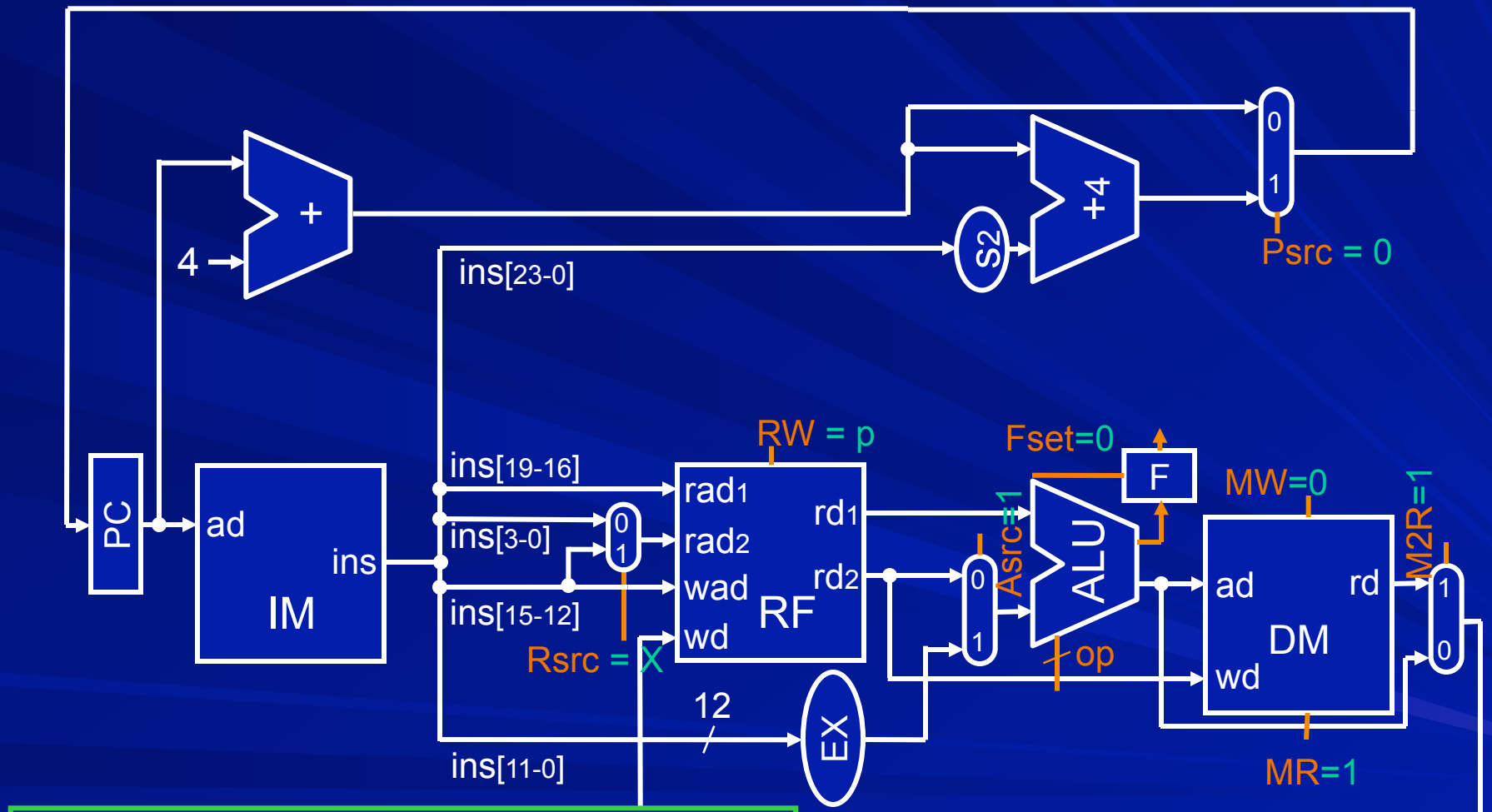
Rsrc	RW	Asrc	MW	MR	M2R	Psrc	Fset
0	0	0	0	0	X	0	p

Control Inputs for str instruction



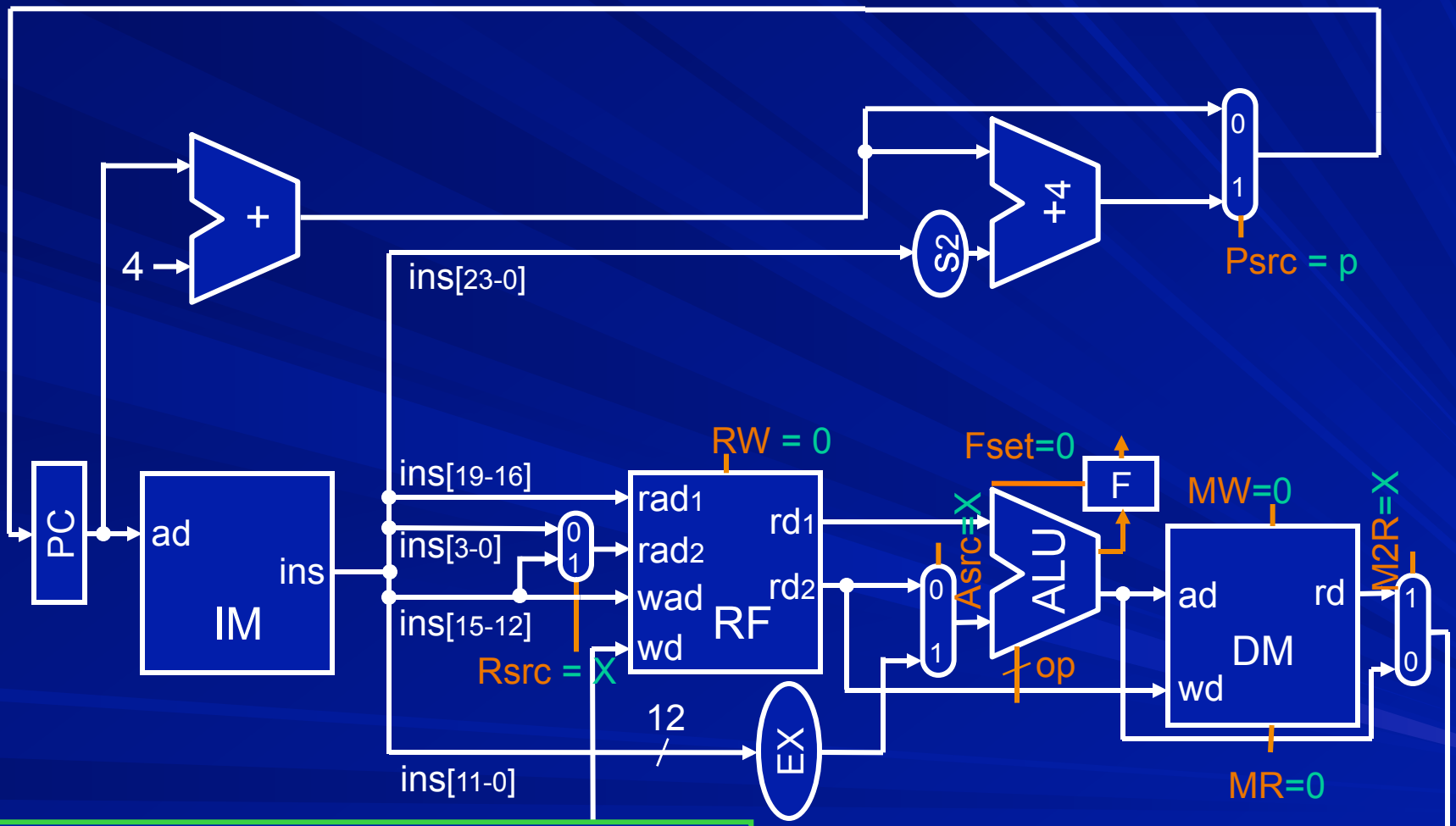
Rsrc	RW	Asrc	MW	MR	M2R	Psrc	Fset
1	0	1	p	0	X	0	0

Control Inputs for ldr instruction



Rsrc	RW	Asrc	MW	MR	M2R	Psrc	Fset
X	p	1	0	1	1	0	0

Control Inputs for b instruction



Rsrc	RW	Asrc	MW	MR	M2R	Psrc	Fset
X	0	X	0	0	X	p	0

Truth table for main controller

instruction	ins [27-20]					Rsrc	RW	Asrc	MW	MR	M2R	Psrc	Fset
		I	opc		S								
arith,logic[1]	0 0	X	0 X X X		0	0	p	0	0	0	0	0	0
arith,logic[1]	0 0	X	0 X X X		1	0	p	0	0	0	0	0	p
arith,logic[2]	0 0	X	X 1 X X		0	0	p	0	0	0	0	0	0
arith,logic[2]	0 0	X	X 1 X X		1	0	p	0	0	0	0	0	p
cmp,test	0 0	X	1 0 X X		X	0	0	0	0	0	X	0	p
		I	P	U	B	W	L						
sdr	0 1	X	X	X	X	X	0	1	0	1	p	0	X	0	0
ldr	0 1	X	X	X	X	X	1	1	p	1	0	1	1	0	0
						L							
b	1 0	X	X	X	X	X	X	X	0	X	0	0	X	p	0