COL216 Computer Architecture
Lab Assignment 3

This and subsequent lab assignments involve designing hardware for processors and their subsystems. The designs are to be expressed in VHDL and then simulated and synthesized for Xilinx FPGA devices.

For this assignment, implement the following subset of ARM instructions.

Branch:	<b | bl> {*cond*} <destination>
Add-sub:	<add | sub | rsb | adc | sbc | rsc> {*cond*} {s} Rn, Rd <Op2>
Logical:	<and | orr | eor | bic> {*cond*} {s} Rn, Rd <Op2>
Test:	<cmp | cmn | teq | tst> {*cond*} Rn <Op2>
Move:	<mov | mvn> {*cond*} {s} Rd <Op2>
Multiply:	<mul> {*cond*} {s} Rd, Rm, Rs
Load/store:	<ldr | str> {*cond*} {b} Rd, # <Imm12>

cond:	<EQ|NE|CS|MI|PL|LS|VS|VC|HI|GE|LT|GT|LE|AL>
destination:	24 bit signed word-offset
Op2:	Rm{, <LSL | LSR | ASR | ROR> #Imm5} or, <#Imm32>
Imm5:	5 bit unsigned immediate
Imm12:	12 bit signed immediate
Imm32:	32 bit immediate encoded as 8 bit immediate with 4 bit shift amount

1. Design and simulate the ALU.
2. Design and simulate datapath using ALU designed in step 1.
3. Design and simulate controller
4. Put the datapath and controller together and simulate with some test programs.

Date of announcement: 26th February, 2016

Dates of submission:
Step 1 and 2 11th March, 2016
Step 3 and 4 17th March, 2016