COL216
Computer Architecture

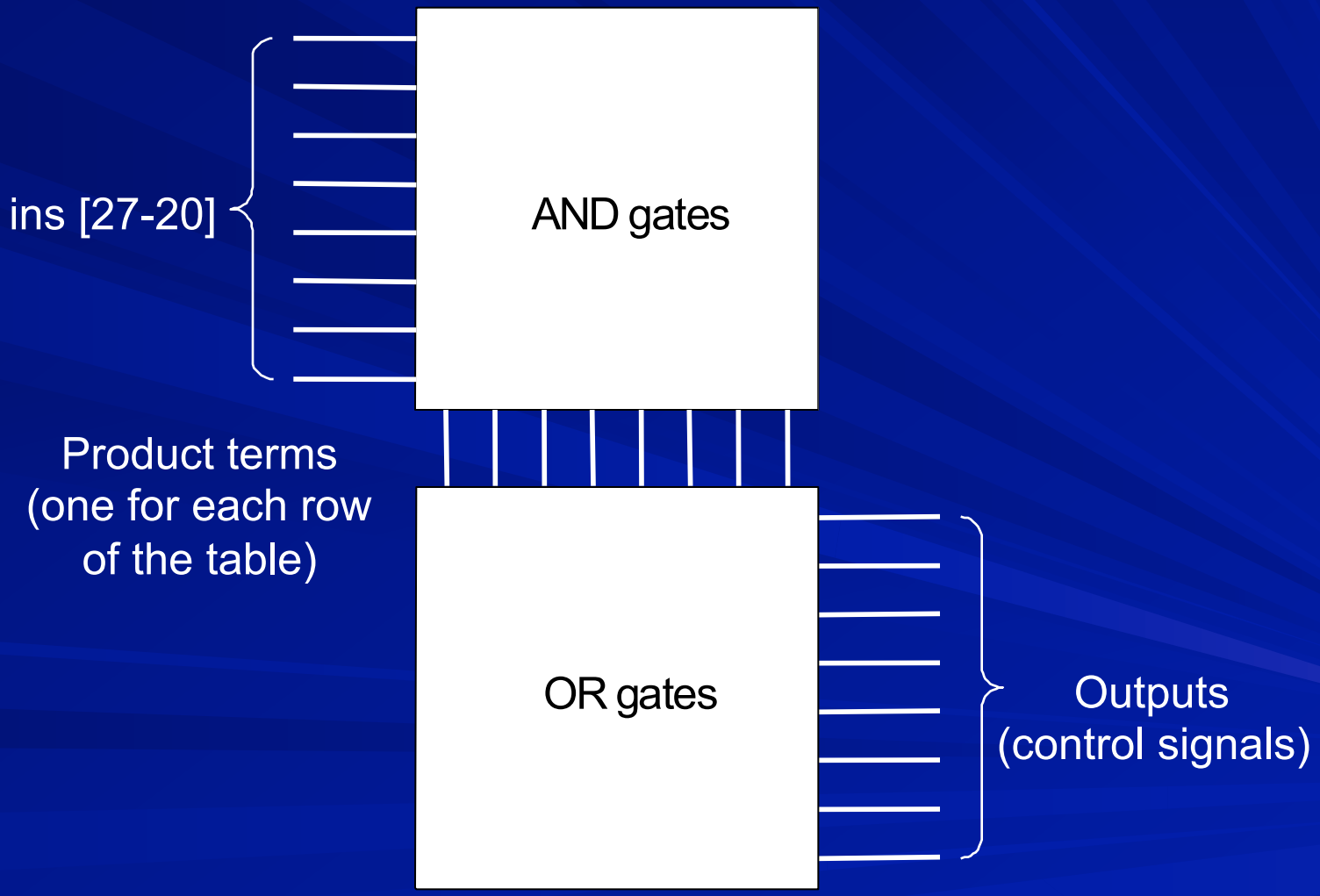
Addendum to Lecture 15

8th March, 2016

Truth table for main controller

instruction	ins [27-20]					Rsrc	RW	Asrc	MW	MR	M2R	Psrc	Fset
		I	opc		S								
arith,logic[1]	0 0	X	0 X X X		0	0	p	0	0	0	0	0	0
arith,logic[1]	0 0	X	0 X X X		1	0	p	0	0	0	0	0	p
arith,logic[2]	0 0	X	X 1 X X		0	0	p	0	0	0	0	0	0
arith,logic[2]	0 0	X	X 1 X X		1	0	p	0	0	0	0	0	p
cmp,test	0 0	X	1 0 X X		X	0	0	0	0	0	X	0	p
		I	P	U	B	W	L						
sdr	0 1	X	X	X	X	X	0	1	0	1	p	0	X	0	0
ldr	0 1	X	X	X	X	X	1	1	p	1	0	1	1	0	0
						L							
b	1 0	X	X	X	X	X	X	X	0	X	0	0	X	p	0

Implementing using PLA



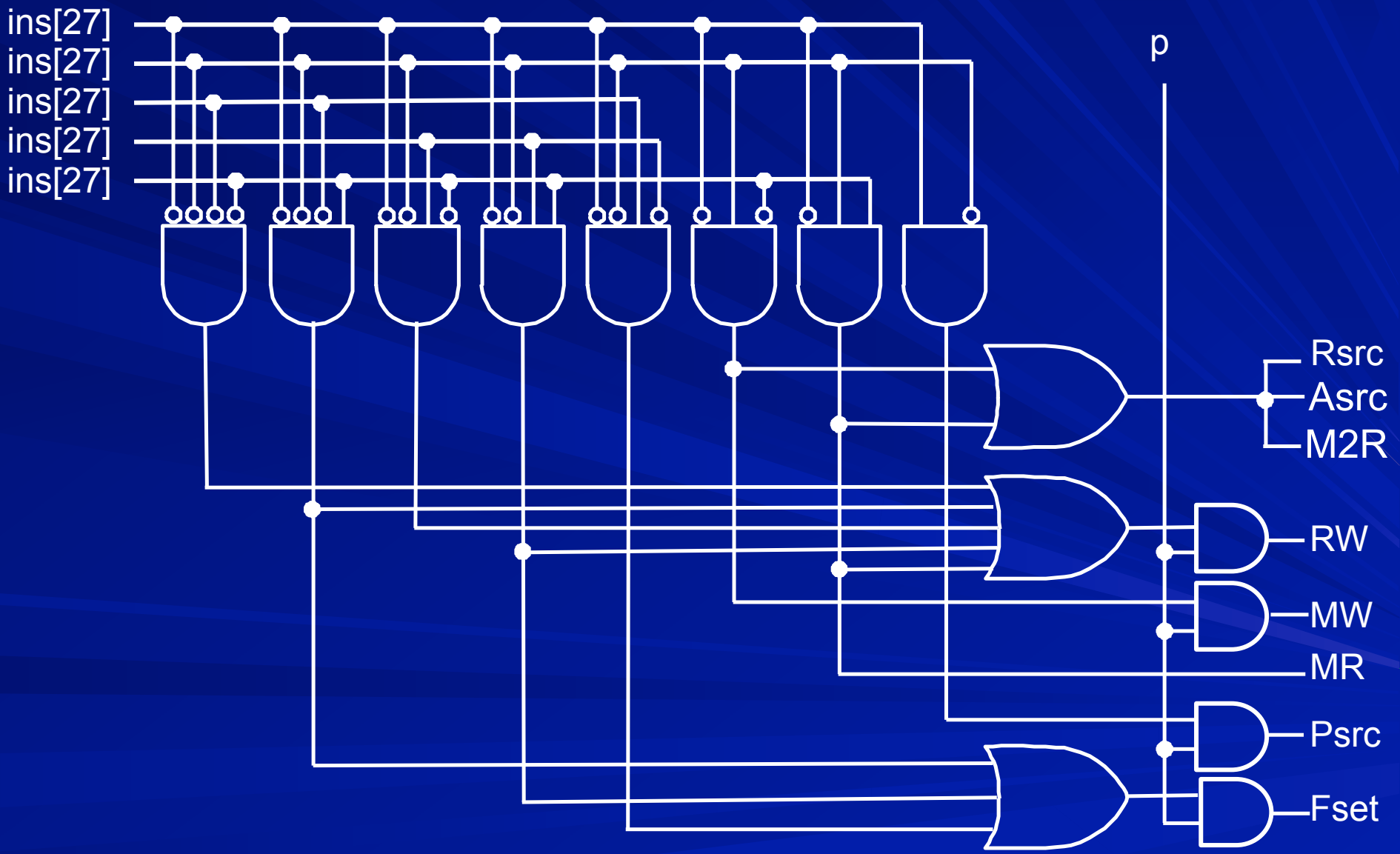
Reducing inputs and outputs

- ins [21], ins [22] and ins [26] are don’t cares in the table and can be omitted
- signals Asrc and M2R are no different from Rsrc and can be dropped
- reduced table is shown next

Reduced table for main controller

ins [27,26,24,23,20]	Rsrc	RW	MW	MR	Psrc	Fset
0 0 0 X 0	0	p	0	0	0	0
0 0 0 X 1	0	p	0	0	0	p
0 0 X 1 0	0	p	0	0	0	0
0 0 X 1 1	0	p	0	0	0	p
0 0 1 0 X	0	0	0	0	0	p
0 1 X X 0	1	0	p	0	0	0
0 1 X X 1	1	p	0	1	0	0
1 0 X X X	X	0	0	0	p	0

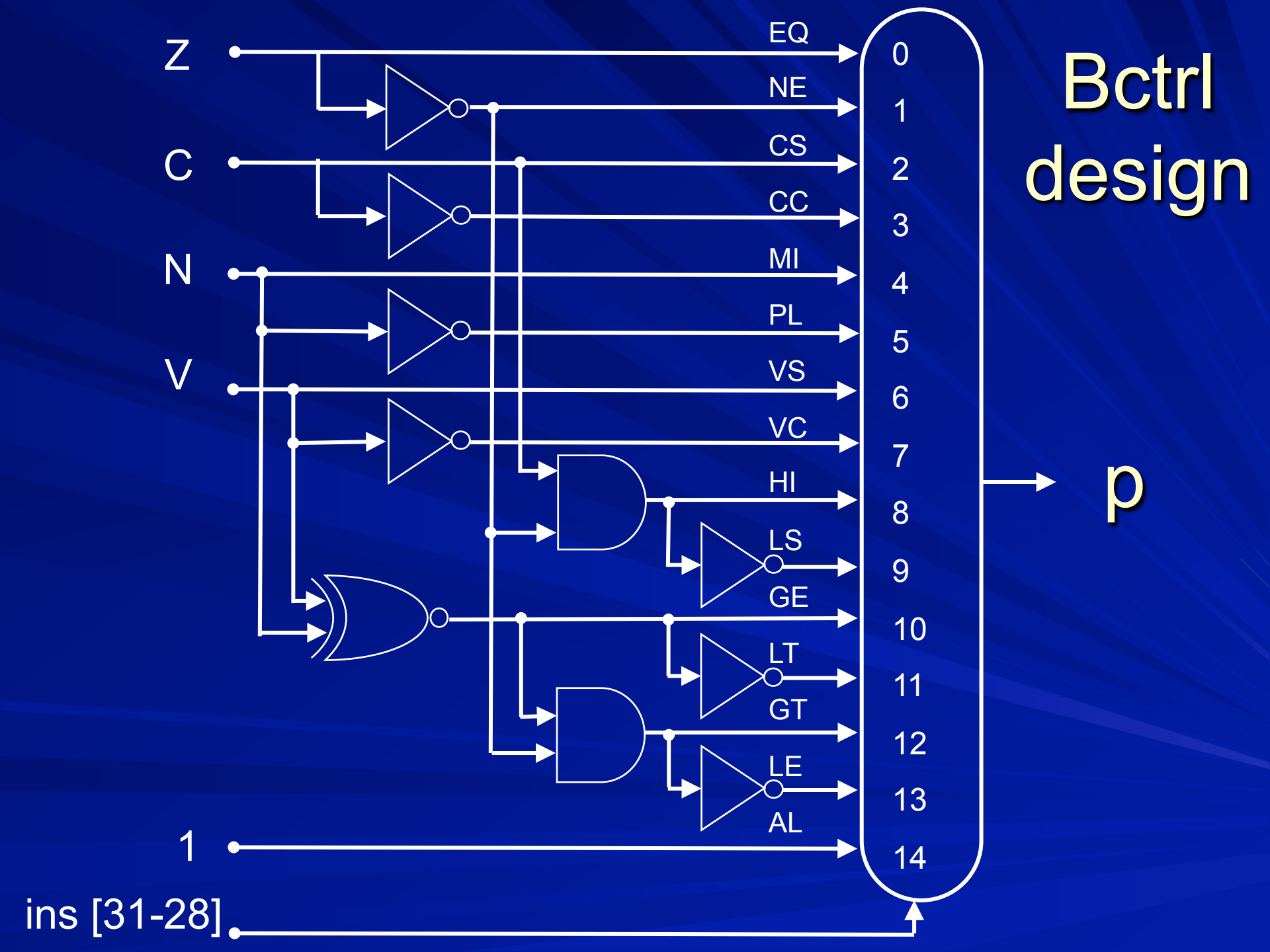
AND-OR PLA for main controller



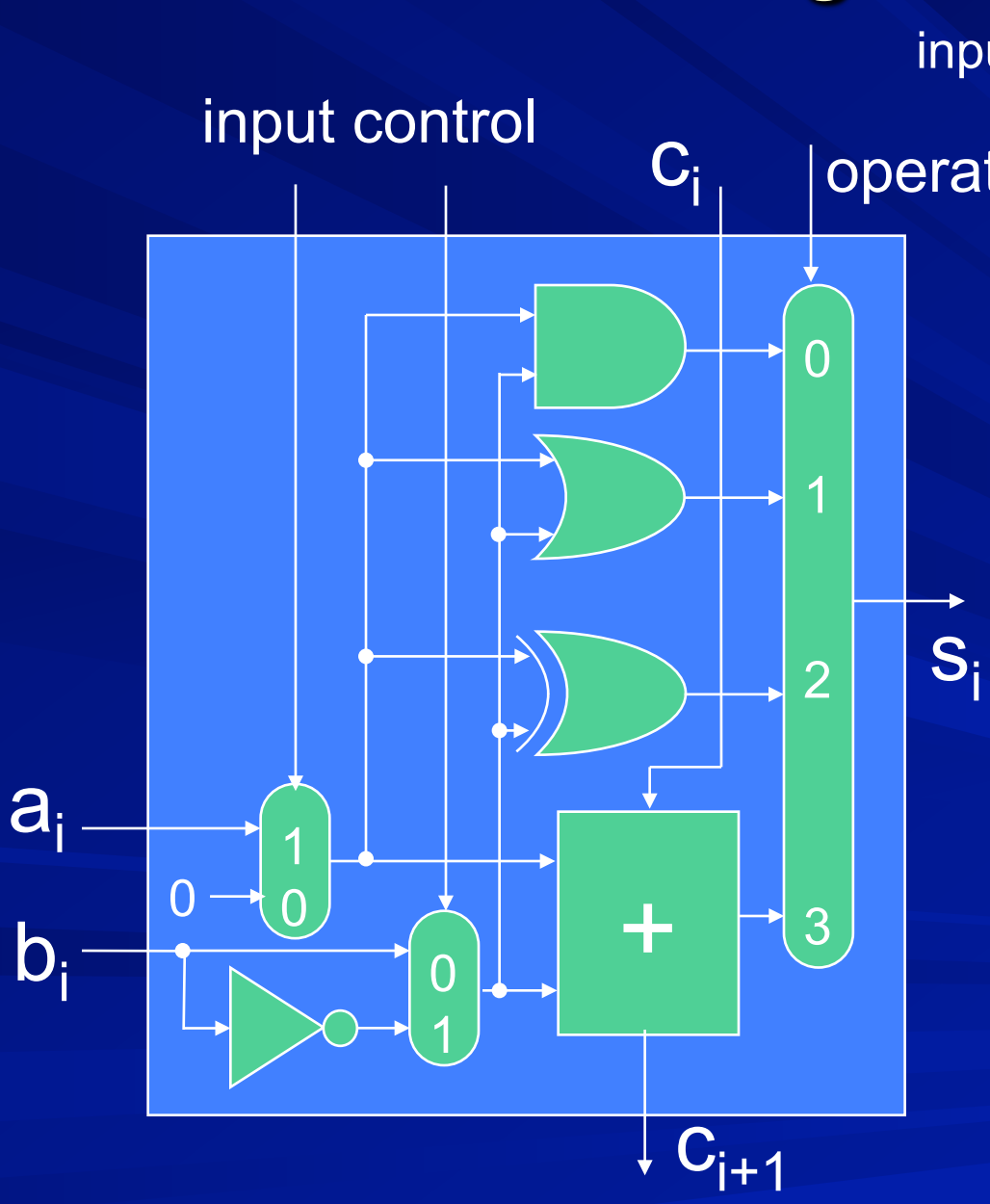
Conditions checked by Bctrl

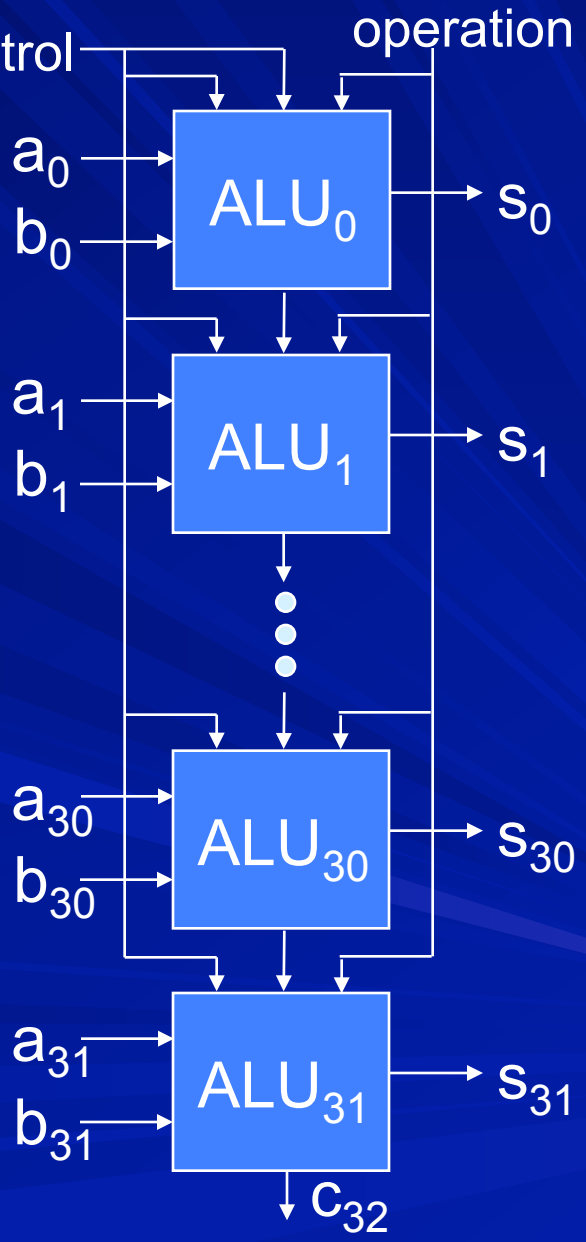
cond	ins [31-28]	Flags
EQ	0 0 0 0	Z set
NE	0 0 0 1	Z clear
CS	0 0 1 0	C set
CC	0 0 1 1	C clear
MI	0 1 0 0	N set
PL	0 1 0 1	N clear
VS	0 1 1 0	V set
VC	0 1 1 1	V clear
HI	1 0 0 0	C set and Z clear
LS	1 0 0 1	C clear or Z set
GE	1 0 1 0	N = V
LT	1 0 1 1	N ≠ V
GT	1 1 0 0	Z clear and (N = V)
LE	1 1 0 1	Z set or (N ≠ V)
AL	1 1 1 0	ignored

Bctrl design



ALU designed earlier





Instructions doable by earlier ALU

- add, sub
- and, eor, orr, bic
- cmp, cmn
- tst, teq
- mov, mvn

Additional DP instructions to be done

- adc, sbc
- rsb, rsc

For reverse subtraction, we can either include multiplexers to switch between Op1 and Op2, or include option to invert Op1.

The initial carry can be constant ‘0’, constant ‘1’ or C Flag.

ALU operations for DP instructions

Instr	ins [24-21]	Operation
and	0 0 0 0	Op1 AND Op2
eor	0 0 0 1	Op1 EOR Op2
sub	0 0 1 0	Op1 + NOT Op2 + 1
rsb	0 0 1 1	NOT Op1 + Op2 + 1
add	0 1 0 0	Op1 + Op2
adc	0 1 0 1	Op1 + Op2 + C
sbc	0 1 1 0	Op1 + NOT Op2 + C
rsc	0 1 1 1	NOT Op1 + Op2 + C
tst	1 0 0 0	Op1 AND Op2
teq	1 0 0 1	Op1 EOR Op2
cmp	1 0 1 0	Op1 + NOT Op2 + 1
cmn	1 0 1 1	Op1 + Op2
orr	1 1 0 0	Op1 OR Op2
mov	1 1 0 1	Op2
bic	1 1 1 0	Op1 AND NOT Op2
mvn	1 1 1 1	NOT Op2

ALU operations for DT instructions

Instr	ins [23] : U bit	Operation
ldr	1	Op1 + Op2
ldr	0	Op1 + NOT Op2 + 1
str	1	Op1 + Op2
str	0	Op1 + NOT Op2 + 1