MARRI LAXMAN REDDY
INSTITUTE OF TECHNOLOGY & MANAGEMENT
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Dundigal (Vill .& Mandal), Medchal District, Hyderabad - 500043, Telangana.

Department of Electronics & Communication Engineering

Unit –III

LECTURE NOTES

ON

ANALOG AND DIGITAL ELECTRONICS

II B. Tech I semester (JNTUH-R18)

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Department of Electronics & Communication Engineering

COURSE: ANALOG AND DIGITAL ELECTRONICS

MAININDEX A.Y:2019-20

Department of Electronics & Communication Engineering

Unit–III

COURSE OBJECTIVE & OUTCOMES

Course Objectives:

- To introduce components such as diodes, BJTs and FETs.
- To know the applications of components.
- To give understanding of various types of amplifier circuits
- To learn basic techniques for the design of digital circuits and fundamental concepts used in
- the design of digital systems.
- To understand the concepts of combinational logic circuits and sequential circuits.

Course Outcomes: Upon completion of the Course, the students will be able to:

- Know the characteristics of various components.
- Understand the utilization of components.
- Design and analyze small signal amplifier circuits.
- Learn Postulates of Boolean algebra and to minimize combinational functions
- Design and analyze combinational and sequential circuits

UNIT-II

SYLLUBUS

FETs And DIGITAL CIRCUITS

FETs and Digital Circuits: FETs: JFET, V-I characteristics, MOSFET, low frequency CS and CD amplifiers, CS and CD amplifiers.

Digital Circuits: Digital (binary) operations of a system, OR gate, AND gate, NOT, EXCLUSIVE ORgate, De Morgan Laws, NAND and NOR DTL gates, modified DTL gates, HTL and TTL gates, output stages, RTL and DCTL, CMOS, Comparison of logic families.

UNIT-III

FIELD EFFECT TRANSISTORS& DIGITAL CIRCUITS

INTRODUCTION:

Field effect devices are those in which current is controlled by the action of an electron field, rather than carrier injection.

Field-effect transistors are so named because a weak electrical signal coming in through one electrode creates an electrical field through the rest of the transistor.

The FET was known as a –unipolar‖ transistor because the function depends only on minority carriers.

The term refers to the fact that current is transported by carriers of one polarity (majority), whereas in the conventional bipolar transistor carriers of both polarities (majority and minority) are involved.

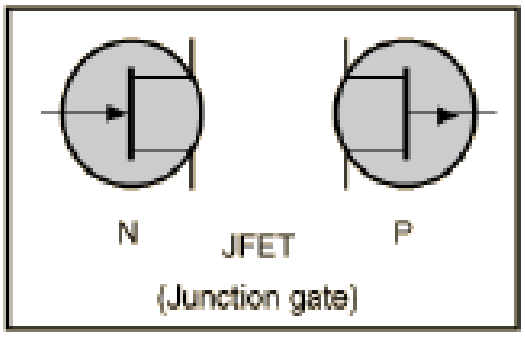
The family of FET devices may be divided into :

• JunctionFET

• Depletion Mode MOSFET

Enhancement Mode MOSFET

3.1 Junction FETs (JFETs):



JFETs consists of a piece of high-resistivity semiconductor material (usually Si) which constitutes a channel for the majority carrier flow.

Conducting semiconductor channel between two ohmic contacts – source & drain.

JFET is a high-input resistance device, while the BJT is comparatively low.

If the channel is doped with a donor impurity, n-type material is formed and the channel current will consist of electrons.

If the channel is doped with an acceptor impurity, p-type material will be formed and the channel current will consist of holes.

N-channel devices have greater conductivity than p-channel types, since electrons have higher mobility than do holes; thus n-channel JFETs are approximately twice as efficient conductors compared to their p-channel counterparts.

The magnitude of this current is controlled by a voltage applied to a gate, which is a reverse-biased.

The fundamental difference between JFET and BJT devices: when the JFET junction is reverse-biased the gate current is practically zero, whereas the base current of the BJT is always some value greater than zero.

Basic structure of JFETs

• In addition to the channel, a JFET contains two ohmic contacts: the source and thedrain.

• The JFET will conduct current equally well in either direction and the source and drain leads are usually interchangeable. N-channelJFET

• This transistor is made by forming a channel of N-type material in a P-typesubstrate.

• Three wires are then connected to thedevice.

• One at each end of thechannel.

• One connected to thesubstrate.

In a sense, the device is a bit like a PN-junction diode, except that there are two wires connected to the N-type side

• The gate is connected to thesource.

• Since the pn junction is reverse-biased, little current will flow in the gateconnection.

• The potential gradient established will form a depletion layer, where almost all the electrons present in the n-type channel will be swept away. The most depleted portion is in the high field between the G and the D, and the least-depleted area is between the G and theS.

• Because the flow of current along the channel from the (+ve) drain to the (-ve) source is really a flow of free electrons from S to D in the n-type Si, the magnitude of this current will fall as more Si becomes depleted of freeelectrons.

• There is a limit to the drain current (ID) which increased VDS can drive through thechannel.

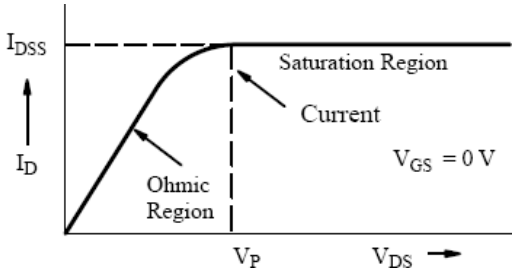
• This limiting current is known as IDSS (*Drain-to-Source current with the gate shorted to the source*).

• The output characteristics of an n-channel JFET with the gate short-circuited to thesource.

• The initial rise in ID is related to the buildup of the depletion layer as VDSincreases.

• The curve approaches the level of the limiting current IDSS when ID begins to be pinchedoff.

• Thephysicalmeaning ofthistermleadsto onedefinitionofpinch-off voltage,V_P,which isthe value of V_{DS} at which the maximum I_{DSS}flows.



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• With a steady gate-source voltage of 1 V there is always 1 V across the wall of the channel at the sourceend.

• A drain-source voltage of 1 V means that there will be 2 V across the wall at the drain end. (The drain is _up' 1V from the source potential and the gate is 1V _down', hence the total difference is2V.)

• The higher voltage difference at the drain end means that the electron channel is squeezed down a bit more at thisend.

• When the drain-source voltage is increased to 10V the voltage across the channel walls at the drain end increases to 11V, but remains just 1V at the sourceend.

• The field across the walls near the drain end is now a lot larger than at the sourceend.

• As a result the channel near the drain is squeezed down quite alot.

• Increasing the source-drain voltage to 20V squeezes down this end of the channelstill more.

• As we increase this voltage we increase the electric field which drives electrons along the open part of thechannel.

• However, also squeezes down the channel near the drainend.

• This reduction in the open channel width makes it harder for electrons topass.

• As a result the drain-source current tends to remain constant when we increase the drain source voltage.

• Increasing V_{DS} increases the widths of depletion layers, which penetrate more into channel and hence result in more channel narrowing toward thedrain.

• The resistance of the n-channel, R_{AB} therefore increases withV_{DS}.

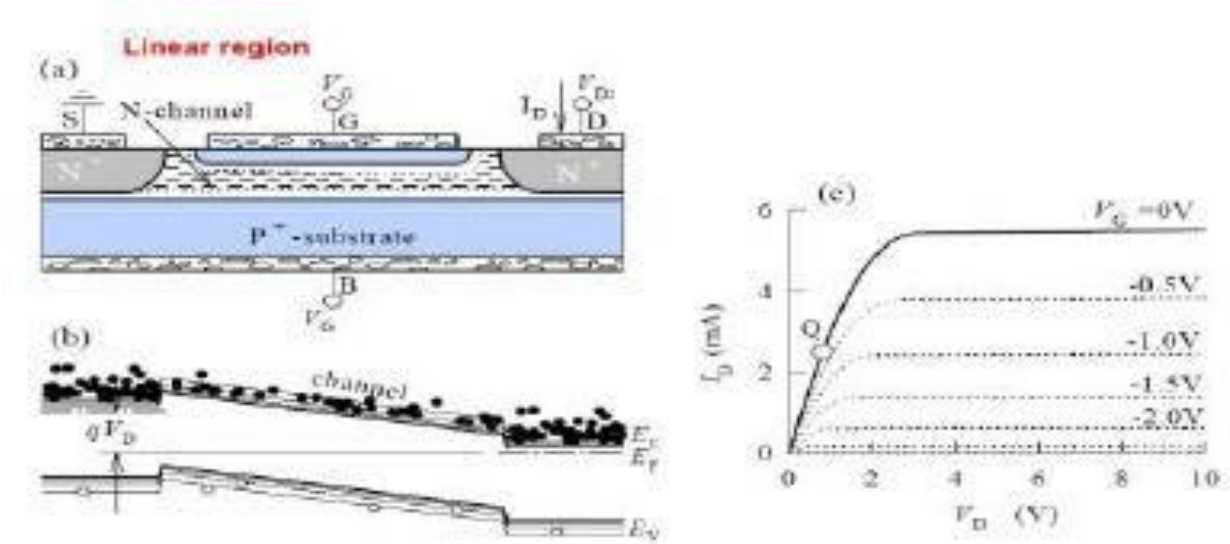
• The drain current: $I_{DS} = V_{DS}/R_{AB}$

• I_D versus V_{DS} exhibits a sub linear behavior, see figure for V_{DS} <5V.

• The pinch-off voltage, V_P is the magnitude of reverse bias needed across the p^+n junction to make them just touch at the drainend.

• Since actual bias voltage across p^+n junction at drain end is V_{GD}, the pinch-off occur whenever: $V_{GD} = -V_P$.

3.2 JFET: I-V characteristics:



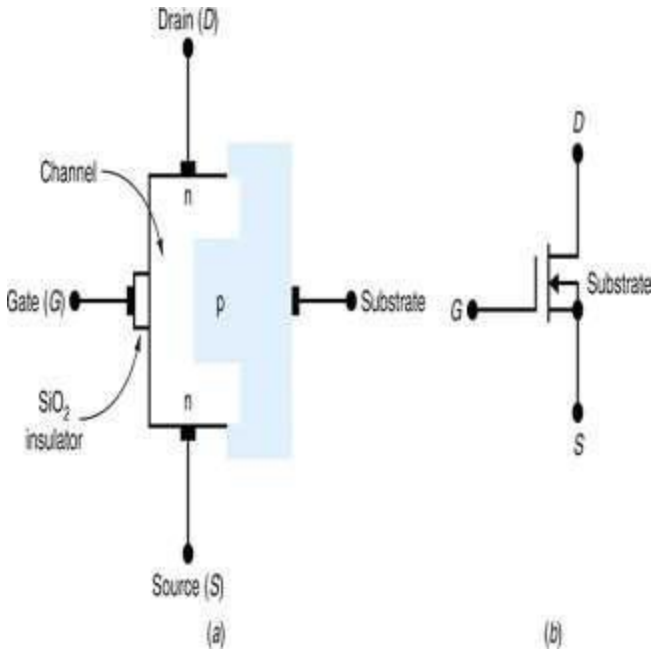
3.3 MOSFETs and Their Characteristics

The metal-oxide semiconductor field effect transistor has a gate, source, and drain just like the JFET.

The drain current in a MOSFET is controlled by the gate-source voltage VGS.
There are two basic types of MOSFETS: the enhancement-type and the depletion-type.

The enhancement-type MOSFET is usually referred to as an E-MOSFET, and the depletion type, aD-MOSFET.

The MOSFET is also referred to as an IGFET because the gate is insulated from the channel



DEPLETION-TYPE MOSFET

MOSFETs are further broken down into depletion type and enhancement type. The terms depletion and enhancement define their basic mode of operation, while the label MOSFET stands for metal-oxide-semiconductor-field-effect transistor.

Basic Construction

The basic construction of the n-channel depletion-type MOSFET is provided in Fig. A slab of p-type material is formed from a silicon base and is referred to as the substrate. It is the foundation upon which the device will be constructed. In some cases the substrate is internally

connected to the source terminal. However, many discrete devices provide an additional terminal labeled SS, resulting in a four-terminal device, such as that appearing in Fig. 1

The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO_2) layer. SiO_2 is a particular type of insulator referred to as a dielectric that sets up opposing (as revealed by the prefix di-) electric fields within the dielectric when exposed to an externally applied field.

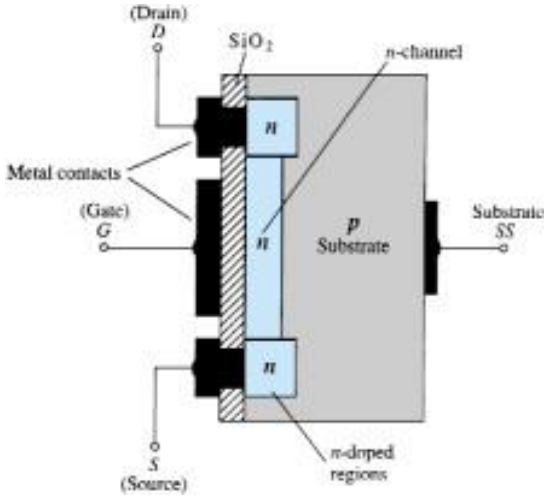


Fig. 1 n – channel depletion type MOSFET

There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

It is the insulating layer of SiO2 in the MOSFET construction that accounts for the very desirable high input impedance of thedevice.

Basic Operation andCharacteristics

In Fig. 2 the gate-to-source voltage is set to zero volts by the direct connection from one terminal to the other, and a voltage VDS is applied across the drain-to-source terminals. The result is an attraction for the positive potential at the drain by the free electrons of the n-channel and a current similar to that established through the channel of the JFET. In fact, the resulting current with V_{GS} = 0 V continues to be labeled IDSS, as shown in Fig. 3.

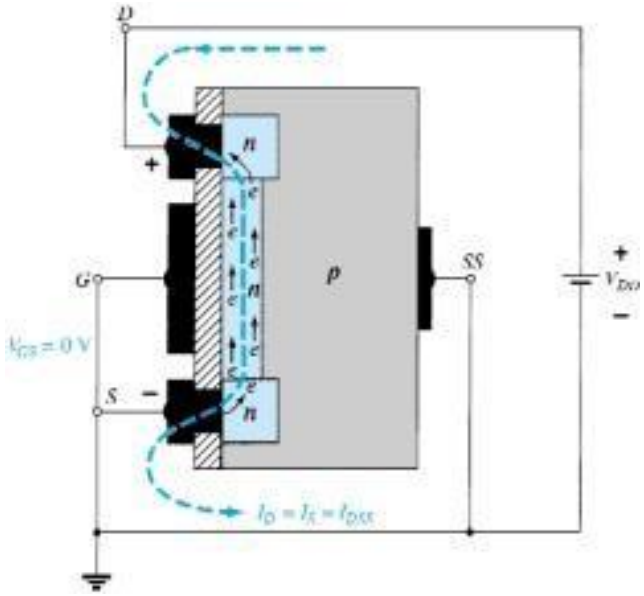


Fig 2. n – channel depletion type MOSFET with V_{GS} = 0 V

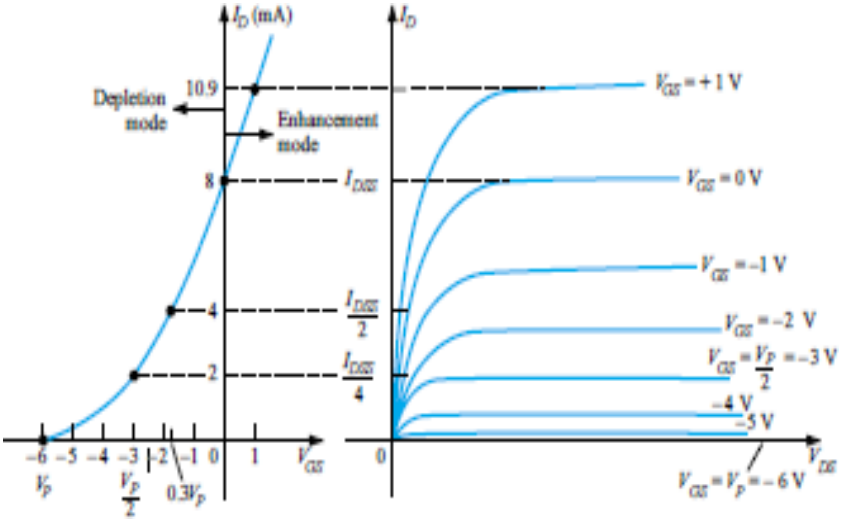


Fig 3. Drain and transfer characteristics

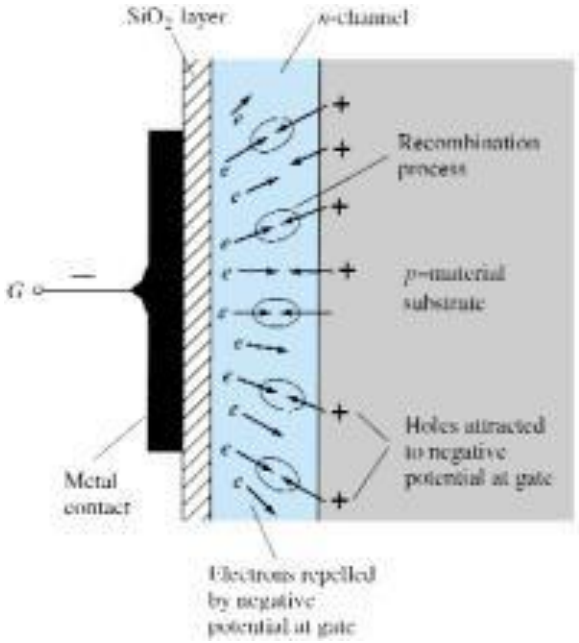


Fig.4 Reduction in free carriers in channel due to –ve potential

In Fig. 4, VGS has been set at a negative voltage such as -1 V. The negative potential at the gate will tend to pressure electrons toward the p-type substrate (like charges repel) and attract holes from the p-type substrate (opposite charges attract) as shown in Fig. 4. Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, the higher the rate of recombination.

For positive values of V_{GS}, the positive gate will draw additional electrons (free carriers) from the p-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig. 3 reveals that the drain current will increase at a rapidrate.

3.4 ENHANCEMENT-TYPE MOSFET

Basic Construction

The basic construction of the n-channel enhancement-type MOSFET is provided in Fig.1. A slab of p-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, while in other cases a fourth lead is made available for external control of its potential level.

The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material. In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and sourceterminals.

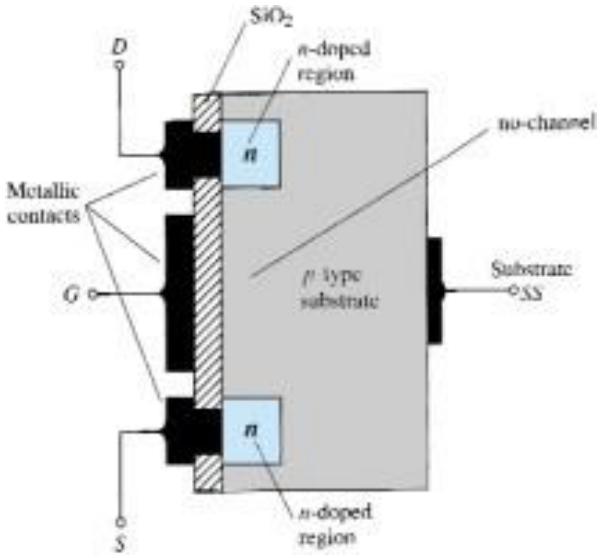


Fig 1. N channel enhancement type MOSFET

Basic Operation and Characteristics

If V_{GS} is set at 0 V and a voltage applied between the drain and source of the device of Fig. 1, the absence of an n-channel (with its generous number of free carriers) will result in a current of effectively zero amperes—quite different from the depletion- type MOSFET and JFET where I_D - I_{DSS}. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and source (due to the n-doped regions) if a path fails to exist between the two. With VDS some positive voltage, VGS at 0 V, and terminal SS directly connected to the source, there are in fact two reverse-biased p-n junctions between the n-doped regions and the p-substrate to oppose any significant flow between drain and source.

In Fig. 2 both VDS and VGS have been set at some positive voltage greater than 0 V, establishing the drain and gate at a positive potential with respect to the source. The positive potential at the gate will pressure the holes (since like charges repel) in the p-substrate along the edge of the SiO2 layer to leave the area and enter deeper regions of the p-substrate, as shown in the figure.

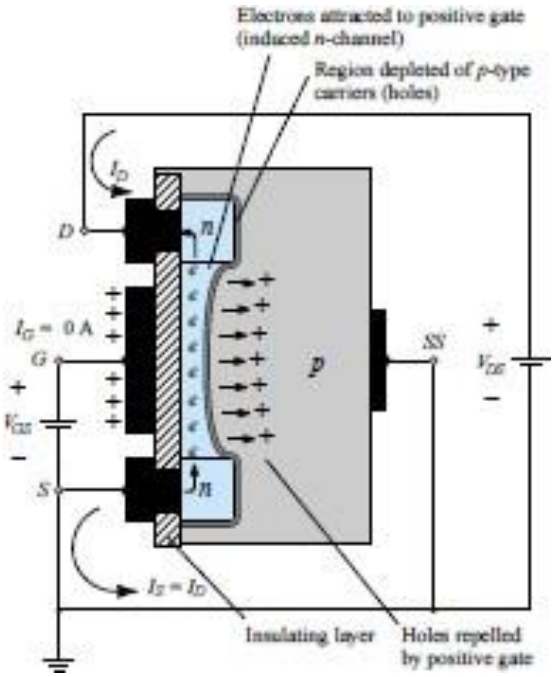


Fig 2. Channel formation

As *VGS* is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold *VGS* constant and increase the level of *VDS*, the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET. The leveling off of $I_D$is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 3. Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. 3, we find that

$$V_{DG} = V_{DS} - V_{GS}$$

The drain characteristics of Fig. 5.34 reveal that for the device of Fig 3 with VGS = 8 V, saturation occurred at a level of VDS = 6 V. In fact, the saturation level for VDS is related to the level of applied VGS by

$$V_{DSsat} = V_{GS} - V_T$$

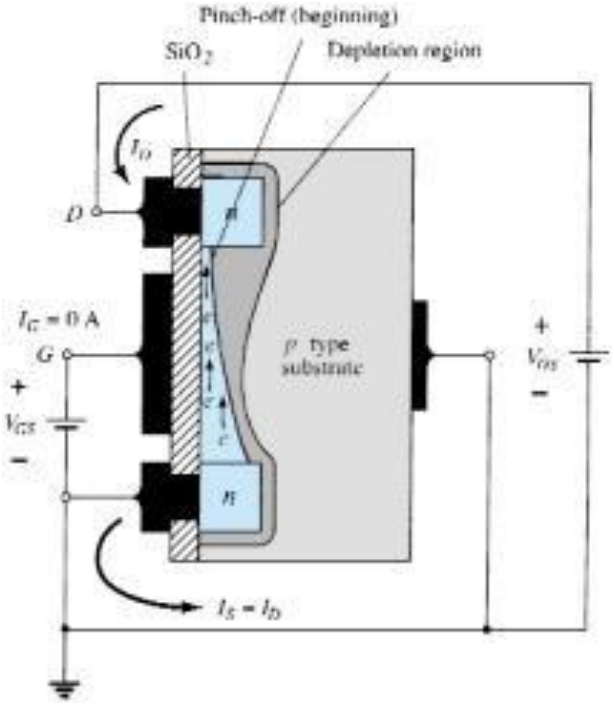


Fig 3. Change in channel and depletion region with increasing V_{DS}

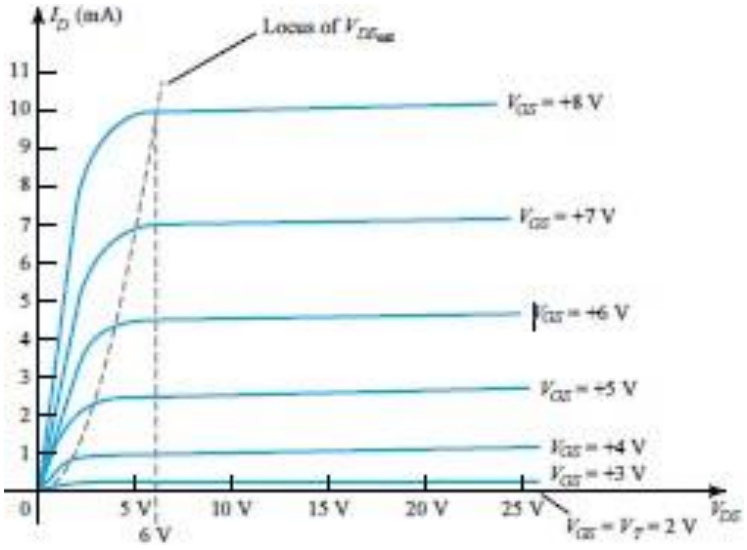


Fig 4. Drain characteristics

For levels of VGS > VT, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2$$

Again, it is the squared term that results in the nonlinear (curved) relationship between ID and VGS. The k term is a constant that is a function of the construction of the device. The value of k can be determined from the following equation where ID(on) and VGS(on) are the values for each at a particular point on the characteristics of the device.

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

3.5 LOGIC GATES:

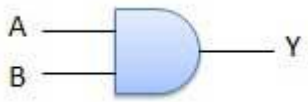
Logic gates are the basic building blocks of any digital system. It is an electronic circuit having one or more than one input and only one output. The relationship between the input and the output is based on a **certain logic**. Based on this, logic gates are named as AND gate, OR gate, NOT gate etc.

AND Gate

A circuit which performs an AND operation is shown in figure. It has n input (n >= 2) and one output.

Y = A AND B AND C ..... N
Y = A.B.C ..... N
Y = ABC ..... N

Logic diagram



Truth Table

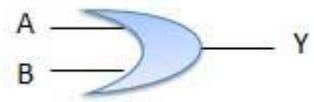
Inputs		Output
A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate

A circuit which performs an OR operation is shown in figure. It has n input (n >= 2) and one output.

Y = A OR B OR C ..... N
Y = A + B + C ..... N

Logic diagram



Truth Table

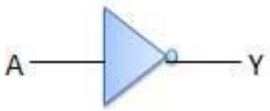
Inputs		Output
A	B	A + B
0	0	0
0	1	1
1	0	1
1	1	1

NOT Gate

NOT gate is also known as **Inverter**. It has one input A and one output Y.

Y = NOT A
Y = $\overline{A}$

Logic diagram



Truth Table

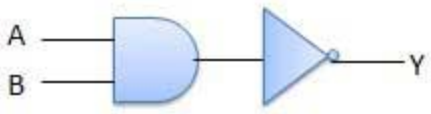
Inputs	Output
A	B
0	1
1	0

NAND Gate

A NOT-AND operation is known as NAND operation. It has n input (n >= 2) and one output.

Y = A NOT AND B NOT AND C ..... N
Y = A NAND B NAND C ..... N

Logic diagram



Truth Table

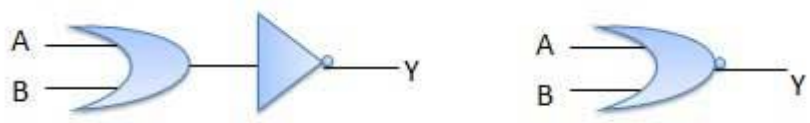
Inputs		Output
A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate

A NOT-OR operation is known as NOR operation. It has n input (n >= 2) and one output.

Y = A NOT OR B NOT OR C ..... N
Y = A NOR B NOR C ..... N

Logic diagram



Truth Table

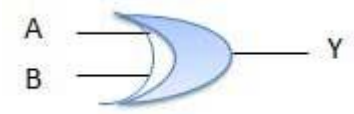
Inputs		Output
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

XOR Gate

XOR or Ex-OR gate is a special type of gate. It can be used in the half adder, full adder and subtractor. The exclusive-OR gate is abbreviated as EX-OR gate or sometime as X-OR gate. It has n input (n >= 2) and one output.

Y = A XOR B XOR C ..... N
Y = $A \oplus B \oplus C$ ..... N
Y = $\overline{A}B + A\overline{B}$

Logic diagram



Truth Table

Inputs		Output
A	B	A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

XNOR Gate

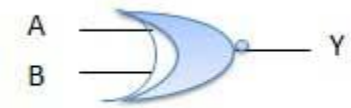
XNOR gate is a special type of gate. It can be used in the half adder, full adder and subtractor. The exclusive-NOR gate is abbreviated as EX-NOR gate or sometime as X-NOR gate. It has n input (n >= 2) and one output.

Y = A XOR B XOR C ..... N

Y = A ⊙ B ⊙ C ..... N

$Y = \overline{A}B + A\overline{B}$

Logic diagram



Truth Table

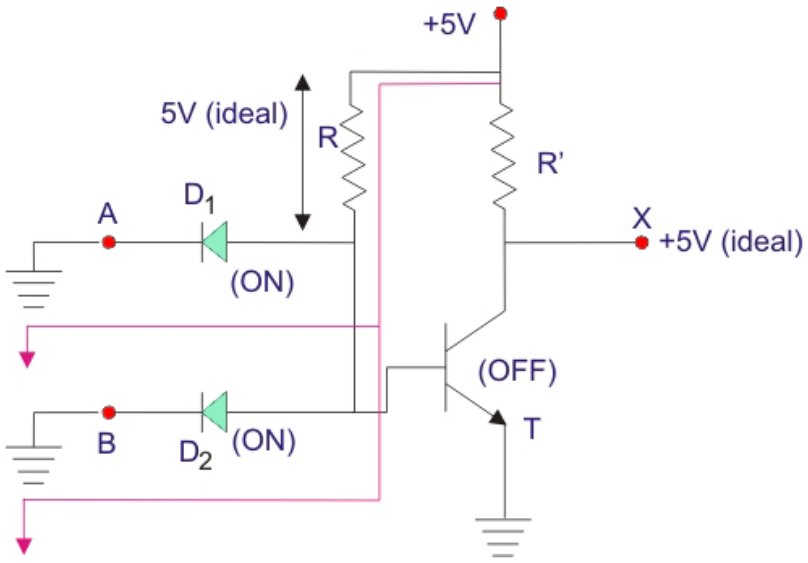
Inputs		Output
A	B	A ⊙ B
0	0	1
0	1	0
1	0	0
1	1	1

3.6 NAND and NOR DTL Circuits:

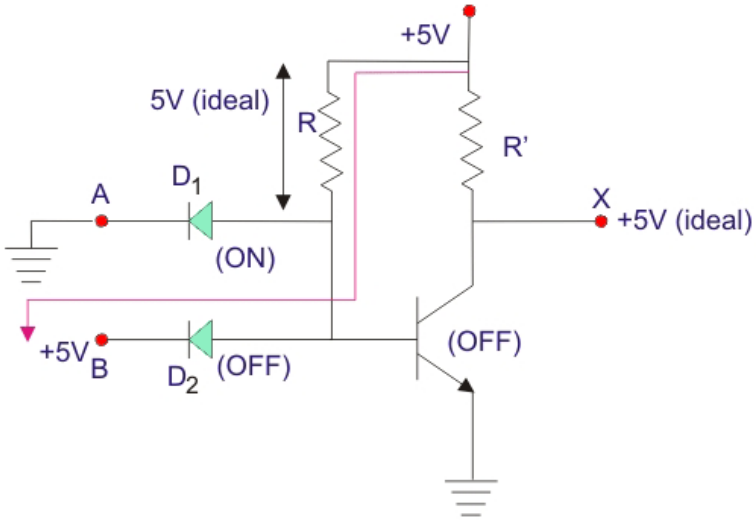
NAND DTL CIRCUIT:

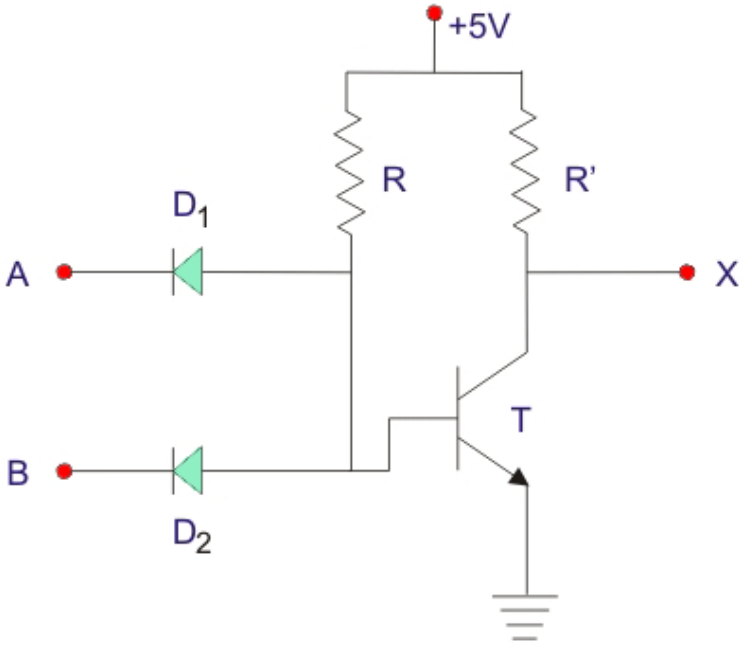
For simplicity we will show here only two inputs NAND gate circuit by using diodes and transistors. This NAND gate is called **DTL NAND gate** or **Diode Transistor Logical NAND Gate**. When both input A and B are given with 0 V, both of the diodes are in forward biased condition that is in ON condition. Supply voltage will get path to the ground through diode D_1 and D_2. Entire supply voltage +5 V will ideally drop across resistor R and hence base terminal of transistor T will not get enough

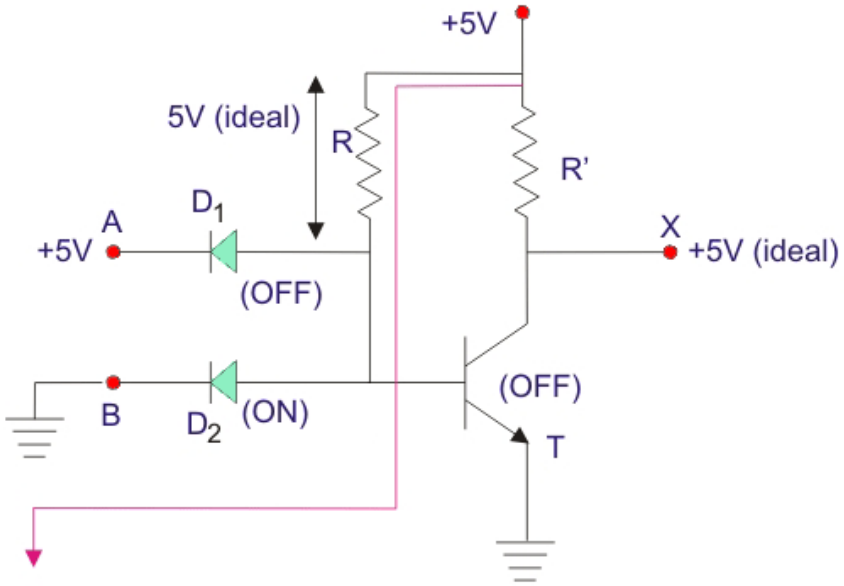
potential to turn ON the transistor and hence the transistor will be in OFF condition. As a result supply voltage +5 V will appear at output terminal X and hence output X will become high or logical 1.



Now if either of diode D_1 and D_2, is applied with 0 V, the same thing happens as in these cases also the supply voltage gets a path to the ground either of the forward biased diode. In that cases also the output will be logical high or 1.

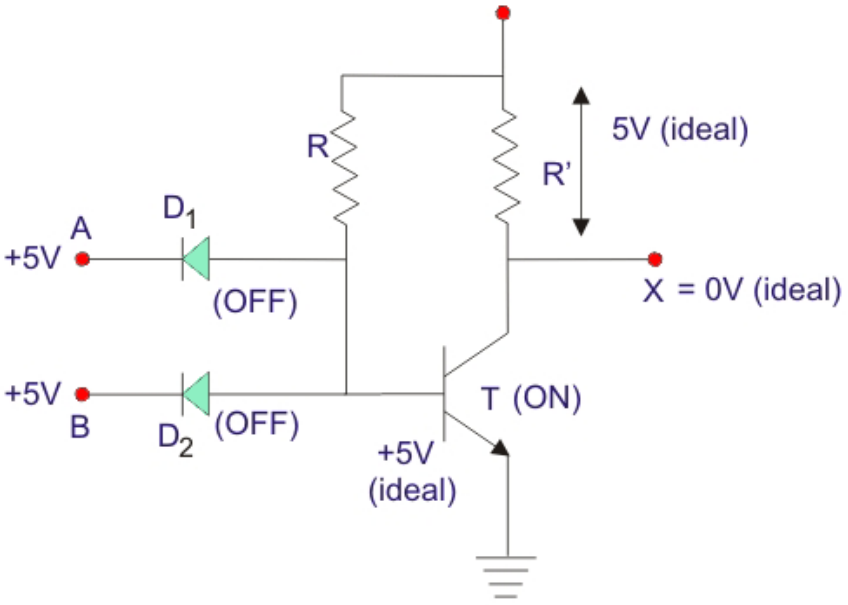




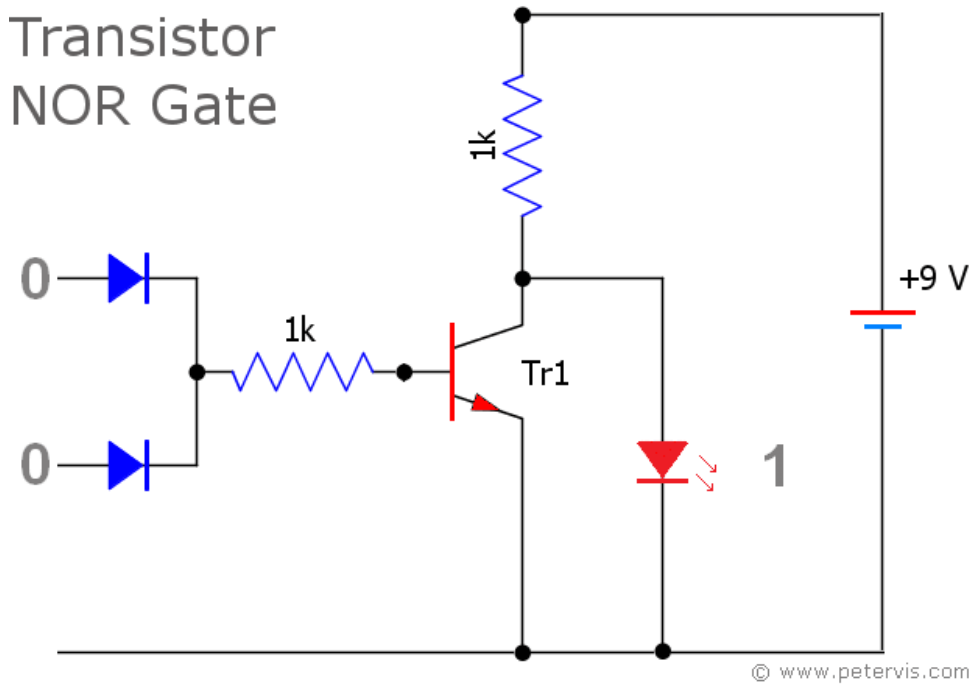


When both of the inputs are given with +5 V that is logical 1, both of the diodes are in OFF condition and hence supply voltage will appear at the base terminal of the transistor T which makes it switched ON and supply voltage gets a path to the ground through this transistors. Ideally entire supply voltage +5 V will drop across resistor R' and output terminal X will get ideally zero volts and hence the output is considered

as logical 0. Hence, the output is only 0 when and only when both inputs are +5 V or logical 1.



NOR DTL CIRCUIT:



This is a Diode-Transistor Logic (DTL) NOR Gate circuit using a general-purpose bipolar junction transistor (BC547), and general-purpose diodes (1N4148). This page shows how to make this circuit, and the implementation is on a breadboard using discrete components.

The working logic is very simple. The emitter-collector junctions of the transistor connect in parallel to the *light emitting diode* (LED). When the transistor conducts (ON), it bypasses the current because almost all the current passes through the emitter-collector junctions, and therefore the LED goes OFF.

The transistor will conduct when either one or both of the inputs receive a logic 1 signal. When both inputs are logic 0, the transistor stops conducting (OFF) and all the current passes through the LED instead, hence the LED lights up.

This is a very simple NOR gate circuit construction using a pair of diodes and a transistor. The implementation is on a solderless breadboard using discrete components. This diagram shows how to make a simple DTL circuit that has the same function as a NOR gate. The design is very similar to the transistor gates shown in this multi-part article.

Make sure you connect the transistor right way round. You may wish to follow the links in the parts list to see how they are connected. To learn how to use the light emitting diode, please refer to the LED Resistor Calculator article.

We apply the power to the circuit through the red wire, which is positive, and the blue wire, which is negative. A PP3 9 V dry cell powers this circuit.

The green wires are for the signal input, and the black wire is for the common ground. The input signal is with respect to ground. For practical purposes, you could use a 1.5 V AA sized battery for the signal inputs, where the black wire connects to the negative of the battery and the green wire to the positive.

3.7 High Threshold Logic, HTL Logic Family

Figure 3.19 shows the circuit configuration of logic gate called *high-threshold logic (HTL) gate*. The circuit shown in Fig. 3.19 can be employed in environments where noise-interference level is high. This circuit is actually a modified version of the DTL gate with a supply voltage of +15 V, which is very high compared to the TTL supply voltage of +5 V. For the HTL gate, a 6.9-V Zener diode is used as the coupling element between transistors T_1 and T_2. T_1 and T_2 perform the NOT operation. Since the coupling Zener diode has a typical breakdown value of 6.9 V, noise of amplitude greater than 7 V alone will be able to produce a switching transition of the gate. These high-amplitude noise voltages are rare and hence the circuit will safely operate in noise-environments.

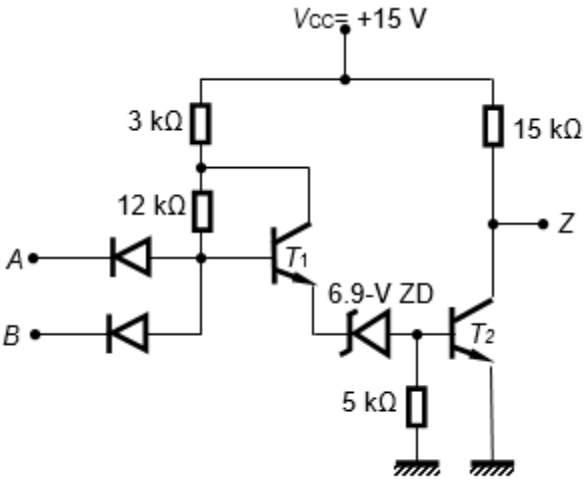


Fig. 3.19 High-threshold logic (HTL) gate

At present, HTL logic gates are replaced with NMOS and CMOS gates, which have, higher noise margins and much more packing density than HTL gates. Hence these gates are almost obsolete.

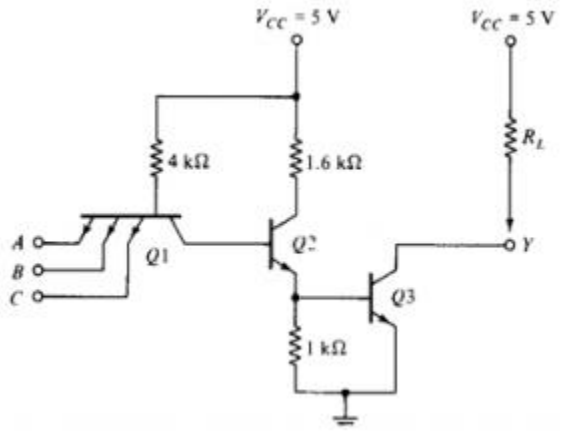
3.8 Introduction to TTLs:

It is a logic family consisting completely of transistors. It employs transistor with multiple emitters. Commercially it starts with the 74 series like the 7404, 74S86 etc. It was build in 1961 by James L Bui and commercially used in logic design in 1963

Classification of TTL:

TTLs are classified based on the output.

1. Open Collector Output: The main feature is that its output is 0 when low and floating when high. Usually an external Vcc may be applied.



Transistor Q1 actually behaves as cluster of diodes placed back to back. With any of the input at logic low, corresponding emitter base junction is forward biased and the voltage drop across the base of Q1 is around 0.9V, not enough for the transistors Q2 and Q3 to conduct. Thus output is either floating or Vcc, i.e. High level.

Similarly when all inputs are high, all base emitter junctions of Q1 are reverse biased and transistor Q2 and Q3 get enough base current and are in saturation mode. Clearly output is at logic low. (For a transistor to go to saturation, collector current should be greater than β times the base current).

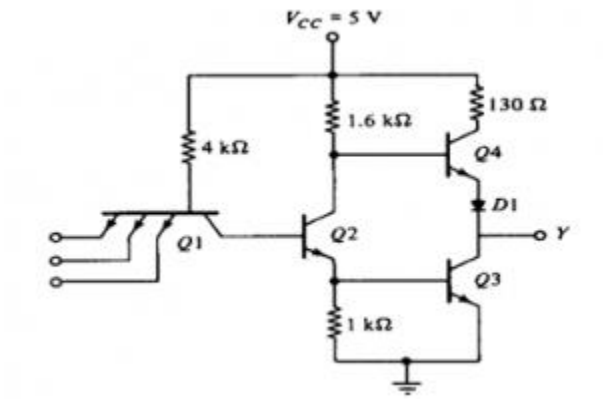
Applications of open-collector output:

It is used in 3 major applications:

1. In driving lamps or relays
2. In performing wired logic
3. In construction of a common bus system

2. Totem Pole Output:

Totem Pole means addition of an active pull up circuit in the output of the Gate which results in reduction of propagation delay.

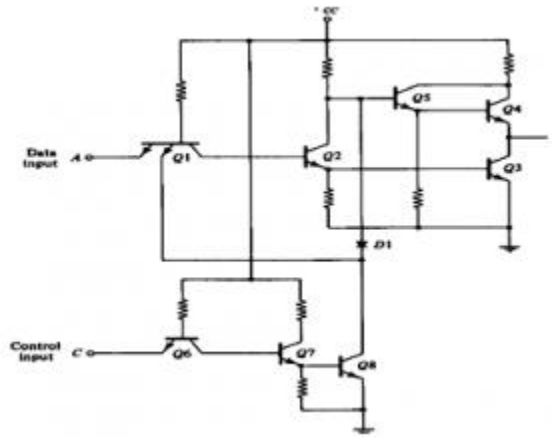


Logic operation is same as the open collector output. Use of transistors Q4 and diode is to provide quick charging and discharging of parasitic capacitance across Q3. Resistor is used to keep the output current to a safe value.

3. Three state Gate:

It provides 3 state output.

1. Low level state when lower transistor is ON and upper transistor is OFF.
2. High level state when lower transistor is OFF and upper transistor is ON.
3. Third state when both transistors are OFF. It allows a direct wire connection of many outputs.



Features of TTL Family:

1. Logic low level is at 0 or 0.2V.
2. Logic high level is at 5V.
3. Typical fan out of 10. It means it can support at most 10 gates at its output.

4. A basic TTL device draws a power of almost 10mW, which reduces with use of schottky devices.
5. Average propagation delay is about 9ns.
6. The noise margin is about 0.4V.

Series of TTL IC:

TTL ICs mostly start with the 7 series. It has basically 6 subfamilies given as:

1. Low Power device with propagation delay of 35 ns and power dissipation of 1mW.
2. Low power Schottkydevice with delay of 9ns
3. Advanced Schottky device with delay of 1.5ns.
4. Advanced low power Schottkydevice with delay of 4 ns and power dissipation of 1mW.

In any TTL device nomenclature, first two names indicate the name of the subfamily the device belongs to. The first two digits indicate the temperature range of operation. The next two alphabets indicate the subfamily the device belongs to. The last two digits indicate the logic function performed by the chip.

Examples are: 74LS02- 2 neither input NOR gate.

74LS10- Triple 3 input NAND gate.

TTL Applications:

1. Used in controller application for providing 0 to 5Vs
2. Used as switching device in driving lamps and relays
3. Used in processors of mini computers like DEC VAX
4. Used in printers and video display terminals

Typical TTL circuits

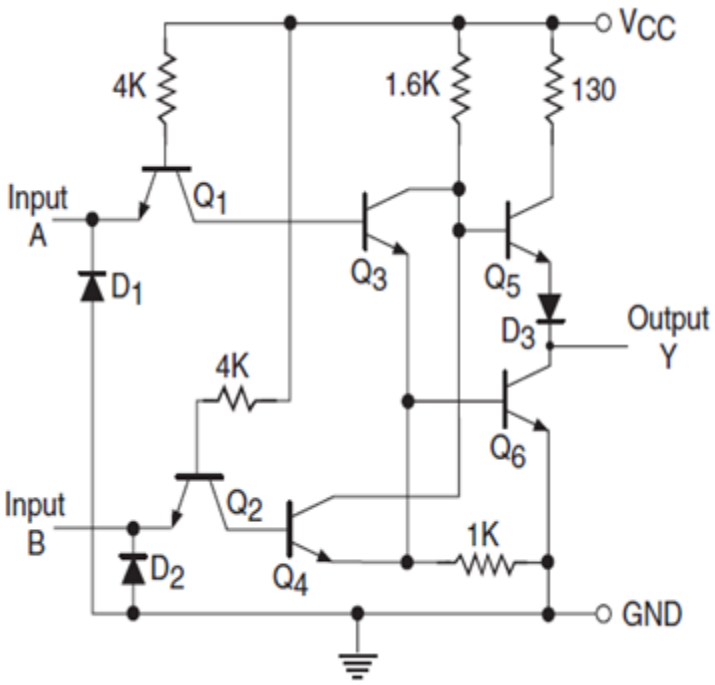
Logic Gates are used in daily life in applications like in clothes dryer, computer printer, door bell etc.

The 3 basic Logic gates implemented using TTL logic are given below:-

1. NOR Gate

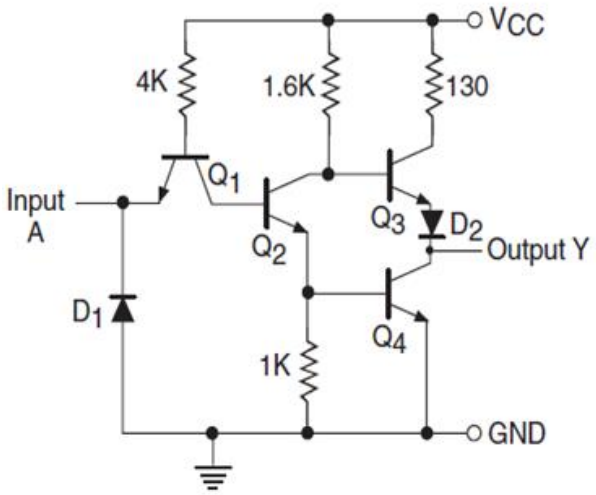
Suppose input A is at logic high, corresponding transistor's emitter base junction is reverse biased and base

collector junction is forward biased. Transistor Q3 gets base current from supply voltage Vcc and goes to saturation. As a result of low collector voltage from Q3, transistor Q5 goes to cut off and on the other hand if another input is low, Q4 is cut off and correspondingly Q5 is cut off and output is connected directly to ground through transistor Q3. In a similar way, when both inputs are logic low, the output will be at logic high.



2. NOT Gate

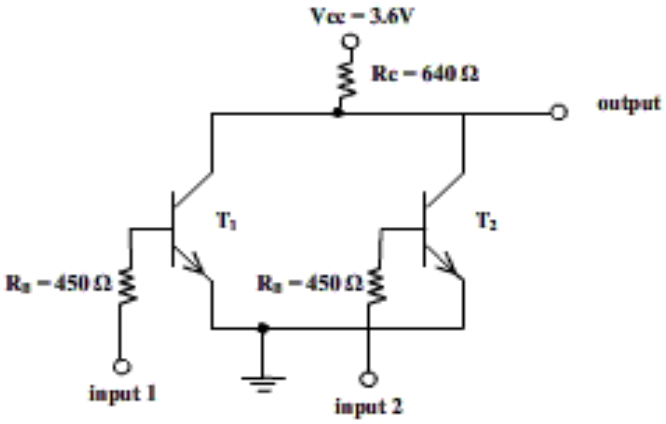
When input is low, corresponding base emitter junction is forward biased, and base collector junction is reverse biased. As a result transistor Q2 is cut off and also transistor Q4 is cut off. Transistor Q3 goes to saturation and diode D2 starts conducting and output is connected to Vcc and goes to logic high. Similarly, when input is at logic high, output is at logic low.



3.9 RTL & DCTL GATES:

The resistor-transistor logic, also termed as RTL, was most popular kind of logic before the invention of IC fabrication technologies.

As its name suggests, RTL circuits mainly consists of resistors and transistors that comprises RTL devices. The basic RTL device is a NOR gate, shown in figure aside.



Inputs to the NOR gate shown above are 'input1' & 'input2'. The inputs applied at these terminals represent either logic level HIGH (1) or LOW (0).

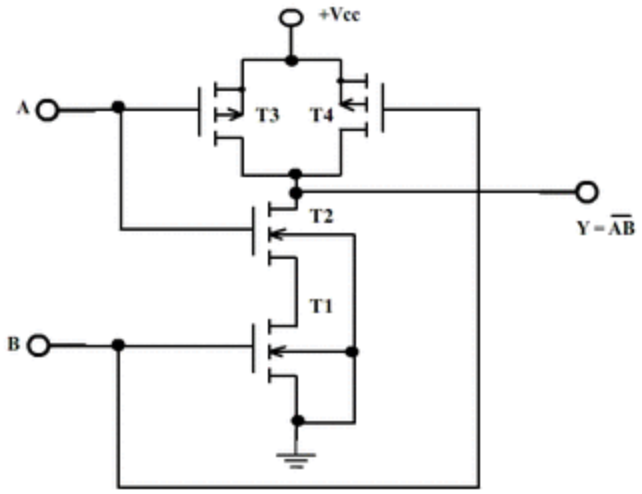
The logic level LOW is the voltage that drives corresponding transistor in cut-off region, while logic level HIGH drives it into saturation region.

If both the inputs are LOW, then both the transistors are in cut-off i.e. they are turned-off. Thus, voltage Vcc appears at *output* I.e. HIGH.
If either transistor or both of them are applied HIGH input, the voltage Vcc drops across Rc and output is LOW.

RTL family is characterized by poor noise margin, poor fan-out *capability*, low speed and high power dissipation. Due to these undesirable *characteristics*, this family is now obsolete.

3.10 CMOS Logic family:

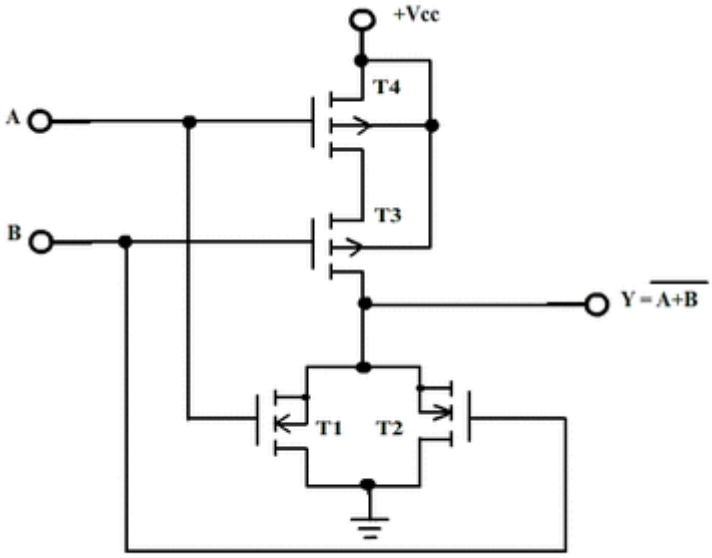
CMOS stands for complementary-MOS, in which both p-channel and n-channel enhancement MOSFET devices are fabricated on same chip. This causes density to be reduced and complex fabrication process. However, CMOS devices consume negligible power and hence are preferred over MOS devices in battery operated applications.



A CMOS NAND gate is shown in figure aside.
T1 and T2 are n-channel MOSFETs while T3 and T4 are p-channel MOSFETs.

When both inputs A & B are HIGH, then T1 & T2 are ON while T3 & T4 are OFF. Hence, output is connected to GND i.e. LOW.

If either input is LOW, then either T3 or T4 is ON, connecting output is +Vcc i.e. HIGH.



Similar is working of CMOS NOR gate shown in figure aside. Here, p-channel devices are in series and n-channel devices are in parallel.

TUTORIAL

1. A combinational circuit has 4 inputs(A,B,C,D) and three outputs(X,Y,Z)XYZ represents a binary number whose value equals the number of 1's at the input
   i Find the minterm expansion for the X,Y,Z
   ii. Find the maxterm expansion for the Y and Z
2. Simplify the following Boolean expressions using K-map and implement them using NOR gates:
   (a) F (A, B, C, D) = AB'C' + AC + A'CD'
   (b) F (W, X, Y, Z) = W'X'Y'Z' + WXY'Z' + W'X'YZ + WXYZ.
3. Design BCD to Gray code converter and realize using logic gates.
4. write standard SOP to given F (A, B, C, D) = AB'C' + AC + A'CD'
5. write standard POS to given F (A, B, C, D) = AB'C'D + ABC + A'CD'
6. . The pinch off voltage for a n – channel JFET is 4 V, when VGS = 1 V, the pinch – off occurs for VDS equal to
7. The 'Pinch – off' voltage of a JFET is 5.0 volts. Its 'cut – off' voltage is
8. A bulb in a staircases has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by and one of the switches irrespective of the state of the other switch. The logic of switching of the bulb resembles.
9. A Boolean function f of two variables X and Y is defined as follows: f(0, 0) = f(0, 1) = f(1, 1) = 1; f(1, 0) = 0 Assuming complements of X and Y are not available, a minimum cost solution for realizing using only 2-input NOR gates and 2-input OR gates (each having unit cost) would have a total cost Of
10. The Boolean function Y= AB + CD is to be realized using only 2 input NAND gates .The minimum number of gates required is

DESCRIPTIVE BANK

1. For the Common Source Amplifier, calculate the value of the voltage gain, given i) rd=100KΩ, RL=10KΩ, gm=300μ and RO=9.09KΩ. ii) If CDS=3pF, determine the output impedance at a signal frequency of 1 MHz.
2. Why we call FET as a Voltage Controlled Device
3. Define DC Drain resistance, AC Drain Resistance, Amplification Factor and derive them.
4. What are the values of ID and gm for VGS = -0.8V if IDSS and VP are given as 12.4mA and -6V respectively?
5. Mention small signal parameters of JFET.
6. Differentiate between BJT and JFET
7. Explain the different biasing techniques of JFET.
8. Describe the construction and working principle of Enhancement mode and depletion mode MOSFET and draw its characteristics.
9. State De Morgans's theorems
10. Prove that OR-AND network is equivalent to NOR-NOR network

OBJECTIVE BANK

1. A JFET is similar in operation to ……. valve

1. diode
2. pentode
3. triode
4. tetrode

ANSWER: 2

2.A JFET is also called …… transistor

1. unipolar
2. bipolar
3. unijunction
4. none of the above

ANSWER: 1

3. **The gate of a JFET is …… biased**

1. reverse
2. forward
3. reverse as well as forward
4. none of the above

ANSWER: 1

4. **In a p-channel JFET, the charge carriers are ……..**

1. electrons
2. holes
3. both electrons and holes
4. none of the above

ANSWER: 2

5. **If the reverse bias on the gate of a JFET is increased, then width of the conducting channel ……..**

1. is decreased
2. is increased
3. remains the same
4. none of the above

ANSWER: 1

6. **A MOSFET can be operated with ……..**

1. negative gate voltage only
2. positive gate voltage only
3. positive as well as negative gate voltage
4. none of the above

ANSWER: 3

7. If a signal passing through a gate is inhibited by sending a LOW into one of the inputs, and the output is HIGH, the gate is a(n):

1 AND

2 NAND

3. NOR

4 OR

ANSWER: B

8. **The inverter is ……**
   1. NOT gate
   2. OR gate
   3. AND gate
   4. None of the above

ANSWER: 1

9. **The NOR gate is OR gate followed by ……**
   1. AND gate
   2. NAND gate
   3. NOT gate
   4. None of the above

ANSWER: 3

10. **Digital circuit can be made by the repeated use of ……**
   1. OR gates
   2. NOT gates
   3. NAND gates
   4. None of the above

ANSWR: 3

DATE:

NAME OF THE STUDENT: **HTNO:** **Branch:**

SUBJECT: Electronic Devices & Circuits **TEST NO: 3** **MARKS: 10M**

SET NO: 1

(PART-A): Answer the Following Objective Questions: Each carries 0.5Mark

1). FET is a ---------- device.
2). MOSFET means ----------.
3). For low values of V_{DS}, JFET behaves like a ----------.
4). The drain characteristics are drawn between ---------- & ----------.
5). The symbol of n-channel MOSFET is ----------.
6). A depletion MOSFET differs from a JFET in the sense that it has no _____..
7). JFET operates in the _____ mode.

8). For an n-channel FET, the arrow on gate has ---------- the channel.
9). The formula for pinch-off voltage is given by ----------.
10). The power dissipation in FET is given by ----------.

(PART-B): Answer any one question

11) a). Explain the volt-ampere characteristics of JFET. **[3M]**
b). Define Transconductance and Drain resistance. **[2M]**

(OR)

12) a). For an n-channel silicon FET with a=3 x 10^{-4} and $N_D=10^{15}$ electrons/cm^3. Find the pinch-off voltage. **[3M]**

b). Draw the symbols of n-channel & p-channel JFET. **[2M]**

DATE:

NAME OF THE STUDENT: **HTNO:** **Branch:**
SUBJECT: Electronic Devices & Circuits **TEST NO: 3** **MARKS: 10M**

SET NO: 2

(PART-A): Answer the Following Objective Questions: Each carries 0.5Mark

1). BJT is a ---------- device.
2). JFET means ----------.
3). In JFET, drain current is maximum when VGS is ----------.
4). Drain resistance, rd is given by ----------.
5). The transfer characteristics are drawn between ---------- & ----------.
6). The symbol of p-channel MOSFET is ----------.
7). The types of MOSFET are ----------.
8). The main factor which differentiates a depletion MOSFET from an enhancement only MOSFET is the absence of _____.

9). For an p-channel FET, the arrow on gate has ---------- the channel
10). The applications of JFET are ----------.

(PART-B): Answer any one question

11) a). Explain the principle of MOSFET in enhancement mode with neat sketches. **[3M]**
b). Give the applications of JFET. **[2M]**

(OR)

12) a). An n-channel JFET has I_{DSS}=8mA and V_p=-5V. Determine the minimum value of V_{DS} for pinch-off region and the drain current I_{DS} **,** for V_{GS} =-2V in the pinch-off region. **[3M]**

b). Draw the symbols of n-channel & p-channel enhancement MOSFET. **[2M]**

DATE:

NAME OF THE STUDENT: **HTNO:** **Branch:**
SUBJECT: Electronic Devices & Circuits **TEST NO: 3** **MARKS: 10M**

SET NO: 3

(PART-A): Answer the Following Objective Questions: Each carries 0.5Mark

1). BJT is a ---------- controlled device.
2). FET means ----------.
3). Transconductance, gm is given by----------.
4). The symbol of n-channel JFET is ----------.
5). The formula for drain current is given by ----------.
6). The Shockley equation is given by ----------.
7). The types of JFET are ----------.
8). The configurations of JFET are ----------.
9). IGFET means ----------.
10). The controlled variable in JFET is ----------.

(PART-B): Answer any one question

11) a). Explain the principle of MOSFET in depletion mode with neat sketches. **[3M]**

b). Write a short notes on pinch-off voltage. **[2M]**

(OR)

12) a). A FET follows the relation $I_{DS} = I_{DSS}[1 - V_{GS}/ V_p]^2$ what are the values of I_D & g_m for $V_{GS} = -1V$ if I_{DSS} & V_p are 8.4mA and -3V respectively**. [3M]**

b). Draw the symbols of n-channel & p-channel depletion MOSFET. **[2M]**

DATE:

NAME OF THE STUDENT: **HTNO:** **Branch:**

SUBJECT: Electronic Devices & Circuits **TEST NO: 3** **MARKS: 10M**

SET NO: 4

(PART-A): Answer the Following Objective Questions: Each carries 0.5Mark

1). FET is a ---------- controlled device.
2). The channel of JFET exists between ---------- & ----------.
3). The amplification factor, μ is given by ----------.
4). When a reverse gate voltage of 12v is applied to JFET, the gate current is 1 nA. The resistance between gate and source is _____.

5). An FET has ---------- input impedance.
6). The drain to source voltage at which the drain current becomes nearly constant is called as -------- ---------- voltage.
7). The symbol of p-channel JFET is ----------.
8). The terminals of FET are ----------, ---------- & ----------.
9). FET is ---------- in size than BJT.
10). In---------- region, FET acts as voltage controlled resistor.

(PART-B): Answer any one question

11) a). Explain the construction of n-channel JFET. **[3M]**

b). Give the advantages of FET over conventional transistors. **[2M]**

(OR)

12) a). Determine the pinch-off voltage for an n-channel silicon JFET, if the thickness of its gate region is given by 3.2×10^{-4} cm and the donor density in n-type region is $1.2 \times 10^{5}/cm^{3}$ **[3M]**

b). Compare JFET and MOSFET. **[2M]**

ASSIGNMENT QUESTIONS

1. Explain with the help of neat diagram construction, working & VI characteristics of n channel MOSFET.
2. Short notes on the functional diagram of JFET?
3. Write standard SOP to given F (A, B, C, D) = AB'C' + AC + A'CD' and also draw logic diagram using Gates.
4. Write standard POS to given F (A, B, C, D) = AB'C'D + ABC + A'CD' and also draw logic diagram using Gates.
5. List the important features of MOSFET?

REAL TIME APPLICATIONS

Applications of FET

Low Noise Amplifier. Noise is an undesirable disturbance super-imposed on a useful signal.

Buffer Amplifier. ...

Cascode Amplifier. ...

Analog Switch. ...

Chopper. ...

Multiplexer. ...

Current Limiter. ...

Phase Shift Oscillators.

MOSFET and Its Applications

The **MOSFET** (Metal Oxide Semiconductor Field Effect Transistor) transistor is a semiconductor device which is widely used for switching and amplifying electronic signals in the electronic devices.
The **MOSFET** is a three terminal device such as source, gate, and drain.

NPTEL

NPTEL LECTURES

http://nptel.ac.in/courses/117105080/

SEMINAR TOPICS

1. Why FET is called a voltage operated device?
2. List the important features of FET?
3. Draw the functional diagram of JFET?
4. List the types of mosfet.

Applications of fet and mosfet

BLOOM'S TAXANOMY-1

TOPIC : **Field Effect Transistor**

ANALYSING:

- Why FET is called Voltage Controlled device?

EVALUATING:

- The 'Pinch – off' voltage of a JFET is 5.0 volts. Its 'cut – off' voltage is?

CREATING :

- Draw the circuit diagram of N-channel JFET.

BLOOM'S TAXONOMY-II

TOPIC: **Digital Circuits**

ANALYSING :

- Difference between Analog and Digital.

CREATING:

- Implement AND gate using universal Gates.

EVALUATING:

- Write the truth tables of logic gates.