Design of CMOS NAND Gate

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***Abstract*—There are several type of basic gatessuch as inverter, NAND gate, NOR gate which are widely used designing .In this paper 28 nm CMOS NAND gate is proposed .**

Keywords—NAND Gate

Introduction

As we know technological evolution lead to reducing of VLSI technology has to follow various prospective like decrease in power dissipation, higher signal to noise margin (SNM) , lower area higher speed and lower cost etc.[1] As the technology is scaled down from higher node to lower node, these various aspects change accordingly. So depending upon the application and fabrication availability we use a particular node. Static CMOS are very power efficient as they dissipate nearly zero power while in idle state. These are frequently used for modeling of various designs. Taking into consideration of the history of CMOS design, power was secondary consideration after speed and area for many chips[2],[3].

Reference Circuit Details

NAND gate is important because we can implement any type of boolean function using combination of NAND gate and this property is known as functional completeness. The function NAND ($a_1,a_2,a_3,.....a_n$) is logically equivalent to NOT (a_1 AND a_2 AND a_3……AND a_n).

There are 3 symbol for NAND gate shown below.

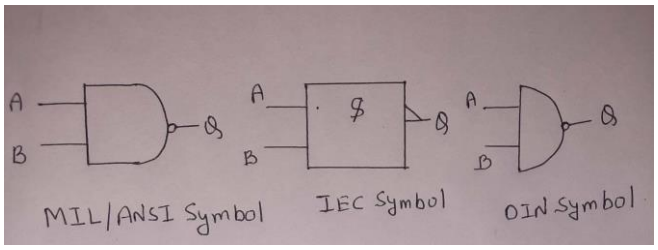

Fig1:Symbols for NAND gate

It consists of two series NMOS transistors between Z and ground and two parallel PMOS transistor between Z and $V_{DD.}$

Case 1.: **V_A** – Low: pMOS1 – ON; nMOS1 – OFF
V_B – High: pMOS2 – OFF; nMOS2 – ON
Case 2 : **V_A – High:** pMOS1 – OFF; nMOS1 – ON
V_B – Low: pMOS2 – ON; nMOS2 – OFF
Case3: **V_A** – High: pMOS1 – OFF; nMOS1 – ON
V_B – High: pMOS2 – OFF; nMOS2 – ON
Case4: **V_A** – Low & **V_B** – Low
Both the pMOS will be ON and both the nMOS will be OFF

1. Reference Circuits

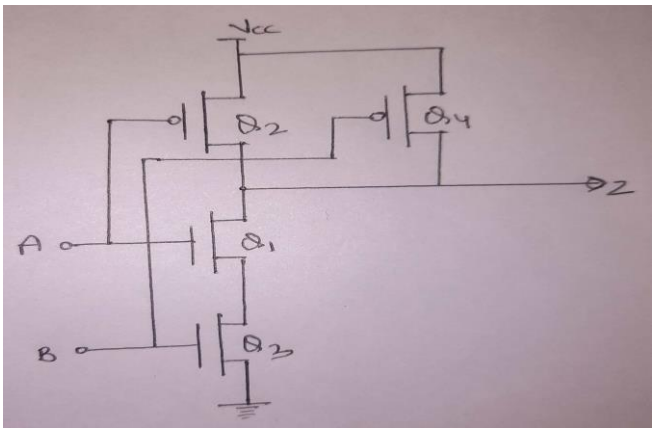

Fig2: Reference circuit diagram

3. Reference Circuit Waveform

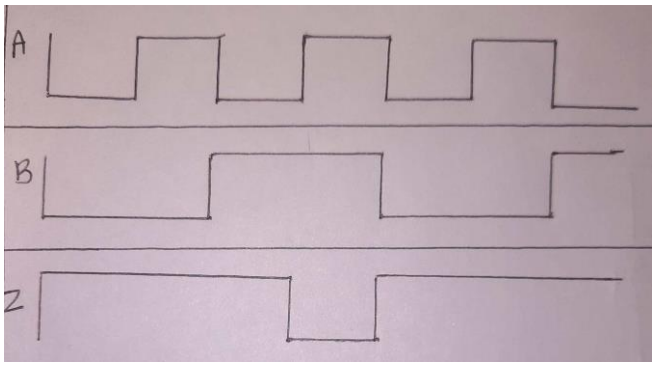

Fig3:Reference circuit Waveform

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