

## Assignment\_ Unit - 3

Programme: B.Tech

Branch: CSE

Semester: 3<sup>rd</sup>

Subject code: CSE 212

Subject Name: Digital electronics

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### PART-A

Q.1: Which of the following flip-flops is known as a "latch"?

Ans: (a) S-R flip-flop.

Q.2: In a D flip-flop, what is the output when the clock pulse

is High and the input D is 1?

Ans: (b) 1

Q.3: What happens when J and K inputs are High in a J-K

flip flop?

Ans: (c) The output toggles.

Q.4: Which of the following is NOT a type of sequential circuit?

Ans: (a) Multiplexer.

Q.5: In a 4-bit synchronous counter, how many flip-flops

are required?

Ans: (c) 4

Q.6: The number of flip-flops needed for a Mod-16 Counter is

Ans: (b) 4

Q.7: A master-slave flip-flop is used to:

Ans: (a) Eliminate race condition.

## Part - B - Short Answer Type Questions

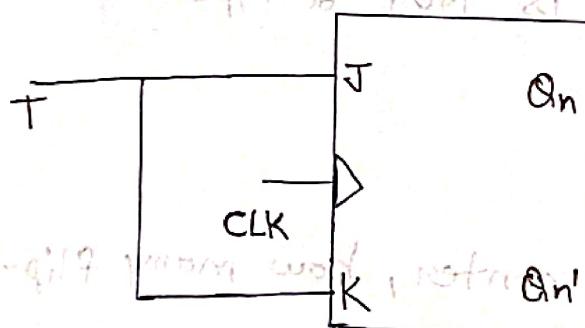
Q-8 - What is a T flip-flop, and how is it derived from a J-K flip-flop?

Ans - T Flip-Flop - A T flip-flop is a digital circuit that toggles its output ( $Q$ ) when the input ( $T$ ) is high and the clock signal is applied. If  $T$  is low, the output remains the same.

T flip-flop Derivation from J-K flip-flop -

A T flip-flop can be derived from a J-K flip-flop by connecting the J and K inputs together and applying the same input signal ( $T$ ) to both. This configuration makes the J-K flip-flop toggle its output when  $T$  is high.

Characteristic table of T-FF  
Excitation table of J-K FF



T	Q <sub>n</sub>	Q <sub>n+1</sub>	J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

K map

J	T	Q <sub>n</sub>	Q <sub>n+1</sub>
0	0	0	1
1	X	X	X

$$J = T$$

J	T	Q <sub>n</sub>	Q <sub>n+1</sub>
0	0	0	X
1	0	1	0

$$K = T$$

Q-9 - Write the D-flip flop truth table and its output state equation.

Ans - Truth Table of D-flip flop :-

Trigger	Inputs	Output		Next state		state
		present state	Q'			
CLK	D	Q	Q'	Q	Q'	
	0	0	1	0	1	No Change
	0	1	0	1	0	Reset
	1	0	1	0	1	No Change
	1	1	0	0	1	Set

Output State Equation of D-flip flop :-

$$Q'(\text{next state}) = D$$

This equation shows that the next state of flip-flop  $Q'$  is directly determined by the input  $D$  when the clock signal (CLK) rises.

Q-10 - Differentiate between synchronous and asynchronous counters.

Ans - Differentiation between synchronous and asynchronous counters :-

Synchronous Counter

- (i) Known as parallel counter.
- (ii) All flip-flops are triggered by the same clock signal simultaneously.
- (iii) Faster and more efficient.

## Asynchronous Counter

- (i) Known as Ripple counter and as serial Counter.
- (ii) Each flip-flop is triggered by the output of the previous flip-flop.
- (iii) Slower due to propagation delays between stages.

Q-11 - Differentiate between Latches and Flip flops

Ans - Latches

- (i) Level-sensitive
- (ii) Output changes as long as the enable signal is active
- (iii) Latches do not require a clock edge to change the output.
- (iv) Latches are more prone to race conditions due to their transparency

Flip Flop

- (i) Edge-sensitive
- (ii) Output changes only at the clock edge (rising or falling)
- (iii) Flip Flops require a clock edge to change the output.
- (iv) Flip Flops are less prone to race conditions due to their edge-sensitive nature.

Q-12 - What is the purpose of a Master-Slave flip-flop?

Ans - Purpose of a Master-Slave flip-flop:-

1. Eliminate race conditions - Prevents data from racing through the circuit.

2. Ensure synchronized data transfer - Critical in digital systems where data needs to be processed in a specific order.
3. Improve reliability - Reduces the risk of error and malfunctions.
4. Increase stability - Provides a stable output despite input changes.

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Q-13 - Define Set-up time and Hold-time.

Ans - Set up Time -

- The minimum time the input signal must be stable before the clock edge.
- Ensures the flip flop captures the correct data.

Hold - Time -

- The minimum time the input signal must remain stable after the clock edge.
- Ensures the flip-flop retains the captured data.

Both setup and hold times are critical in digital circuits to prevent metastability and ensure reliable data transfer.

Q-14 - Write the Truth Table and Boolean equation for D-flip flop.

Ans - Truth Table

Clock	Input	Output	
Function	D	Q	Q'
Low	X	0	1
High	0	0	1
High	1	1	0

Boolean Equation -

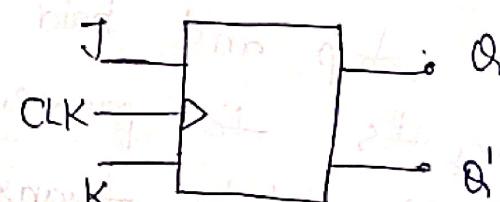
$$Q(t+1) = D$$

Part - C - Long Questions and Answers

Q-15 - Explain the J-K Flip flop with the circuit diagram and make its state table.

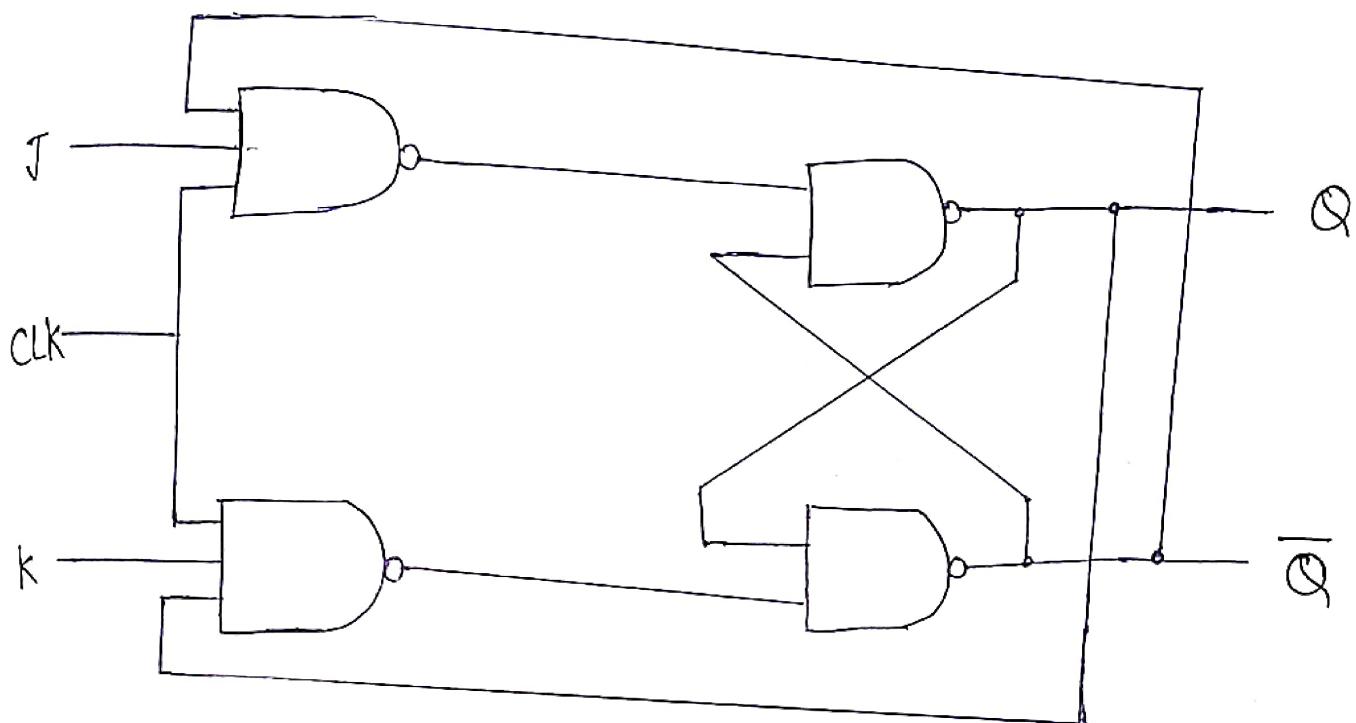
Ans - J-K Flip Flop - The J-K Flip Flop is a type of digital circuit that can store a bit of information. It has two inputs, J (set) and K (reset), and two outputs, Q and Q' (the complement of Q).

Symbol of J-K Flip Flop -



## Circuit Diagram -

The J-K flip flop can be implemented using logic gates, typically NAND or NOR gates.



## J-K Flip Flop State Table :-

CLK	J	K	Q	Q'	State
1	0	0	Q	Q'	No change in state
1	0	1	0	1	Reset Q to 0
1	1	0	1	0	Sets Q to 1
1	1	1	-	-	Toggles

## Explanation -

- Q is the current state of the flip flop
- Q' is the next state of the flip flop
- J and K are the inputs

Q-16 - Describe the shift registers. Draw the diagram of the PIP0 shift register.

Ans - Shift Registers - A shift register is a digital circuit that stores and shifts binary data in a sequence. It consists of a series of flip-flop connected in a chain, allowing data to be shifted from one flip-flop to the next.

### Types of Shift Registers -

1. Serial - In Parallel - Out (SIP0)
2. Serial - In Serial - Out (SISO)
3. Parallel - In Serial - Out (PISO)
4. Parallel - In Parallel - Out (PIPO)

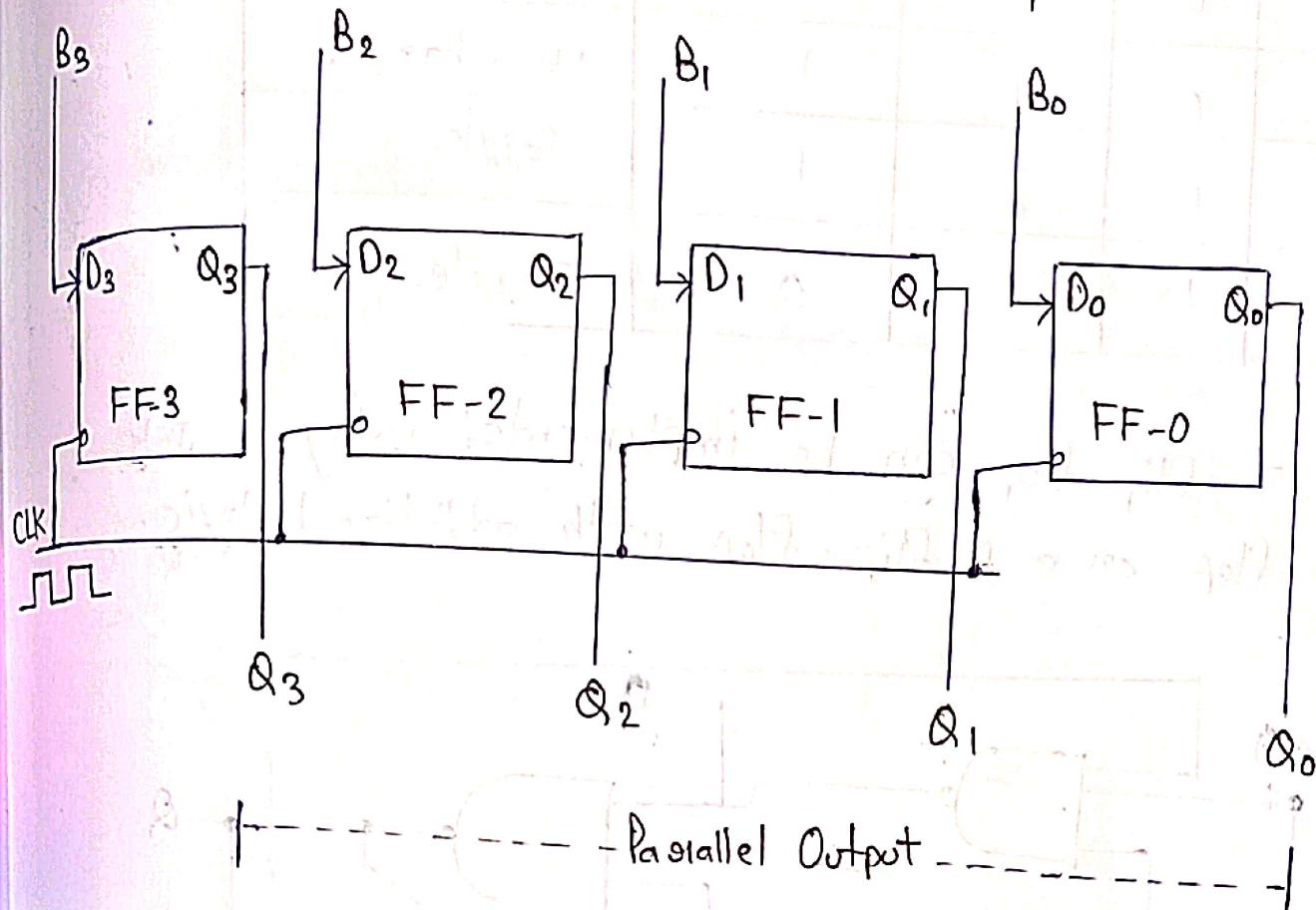
### PIPO Shift Register -

The PIPO shift register consists of multiple D-flip flops connected in parallel, allowing data to be input and output simultaneously.

- In PIPO Shift Register, the inputs and outputs come in a parallel way in the register.
- The inputs  $B_0, B_1, B_2$ , and  $B_3$  are directly passed to the data inputs  $D_0, D_1, D_2$ , and  $D_3$  of the respective flip flop.
- The bits of the binary input is loaded to the flip-

flop when the negative clock edge is applied. The clock pulse is required for loading all the bits. At the output side, the loaded bits appear.

----- Parallel Input -----



----- Parallel Output -----

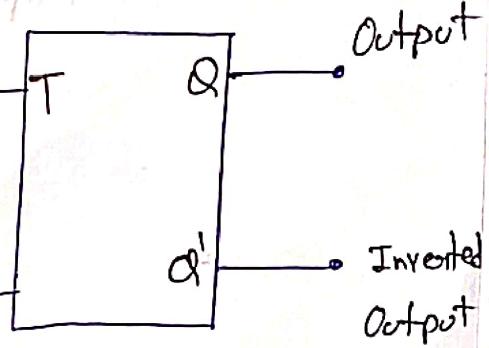
Q-17 - Explain T- flip flop and make its state table.

Ans - T- flip flop - The T - flip flop, also known as the Toggle flip - flop, is a type of digital circuit that can store a bit of information. It has one input, T (Toggle), and two outputs, Q and  $Q'$  (the complement of Q).

Symbol of T- flip flop -

Toggle or  
Trigger input

CLK

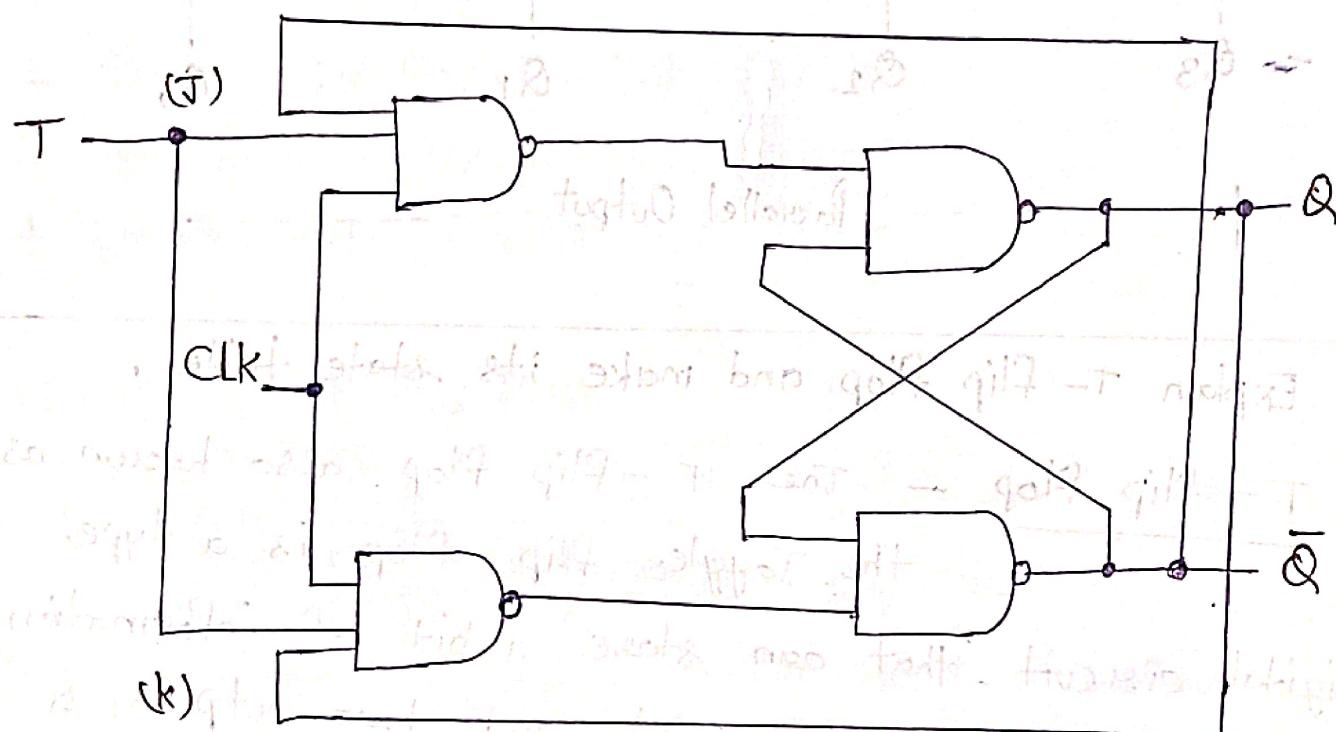


Inverted  
Output

# T - Flip flop State Table

CLK	T	(Present state) $Q(n)$	(Next state) $Q(n+1)$	state
1	0	0	0	No change
1	0	1	1	No change
1	1	0	1	Toggle
1	1	1	0	Toggle

- The T flip flop can be implemented using a J-K flip flop or a D flip-flop with additional logic.



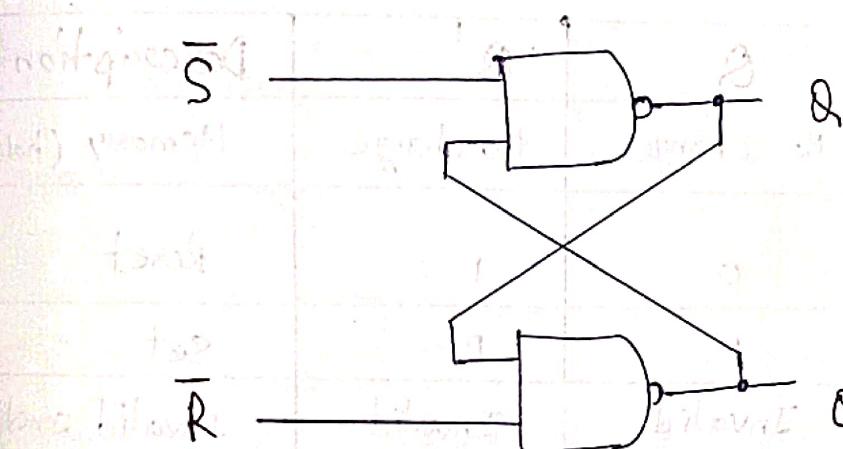
T - Flip flop using J-K Flip flop

Q-18 - Explain the S-R latch using NAND and NOR.

Ans - S-R Latch - An S-R latch is a type of digital circuit that can store a bit of information. It has two inputs, S (Set) and R (Reset), and two outputs, Q and Q' (the complement of Q).

S-R Latch using NAND Gates :- The S-R latch can be implemented

using two NAND gates,

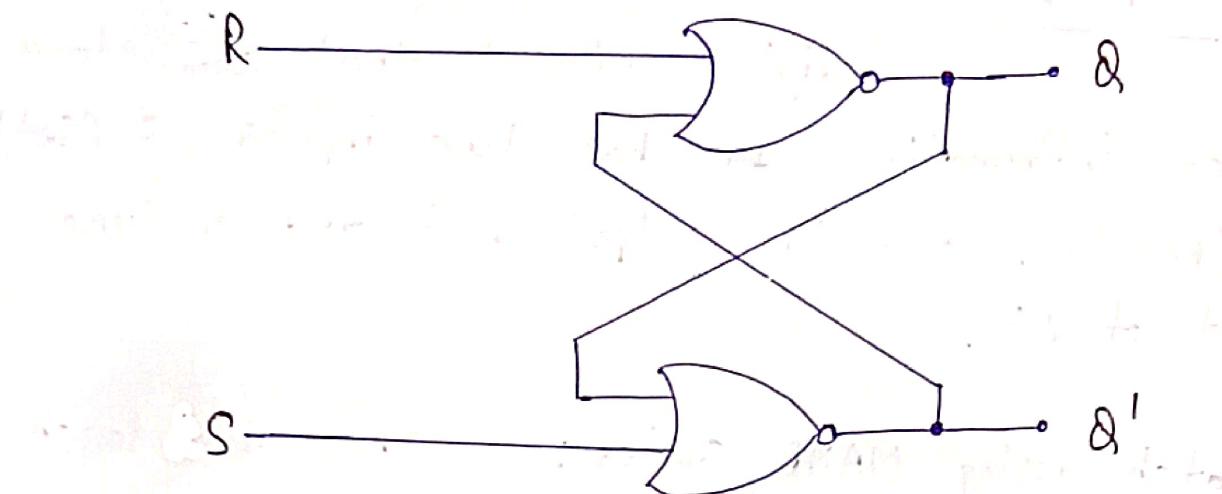


Truth Table

S'	R'	Q	Q'	Description
1	1	No change	No change	Memory (hold state)
1	0	0	1	Reset
0	1	1	0	Set
0	0	Invalid	Invalid	Invalid condition

S-R Latch using NOR Gate :- The S-R Latch can also be implemented using two NOR gates. The circuit is as follows:

## S-R Latch with NOR gates



Truth Table

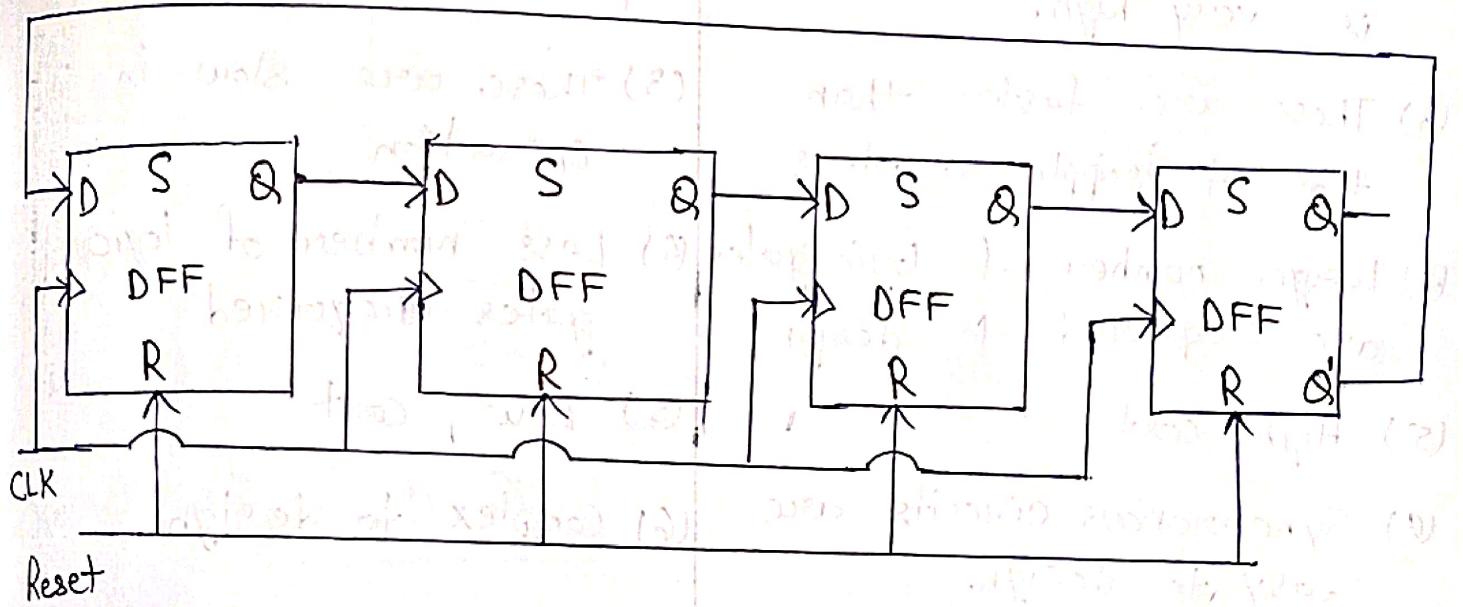
S	R	Q	Q'	Description
0	0	No change	No change	Memory (hold state)
0	1	0	1	Reset
1	0	1	0	Set
1	1	Invalid	Invalid	Invalid condition

Q-19 - Explain the Johnson Counter with its diagram.

Ans - Johnson Counter - A Johnson Counter, also known as a Twisted Ring Counter, is a type of sequential logic circuit used to generate a specific sequence of binary states. It's commonly built using D-flip flops and is known for its efficient use of states.

The Johnson counter can be implemented using n flip flops to count  $2^n$  distinct states.

Circuit Diagram - The Johnson Counter typically consists of D flip flops or J-K flip flops connected in a ring configuration. The output of each flip-flop is connected to the input of the next flip-flop, and the inverted output of the last flip-flop is fed back to the input of the first flip-flop.



4-bit Johnson Counter Sequence:

Clock Cycle	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	Binary Code
0	0	0	0	0	0000
1	0	0	0	1	0001
2	0	0	1	1	0011
3	0	1	1	1	0111
4	1	1	1	1	1111
5	1	1	1	0	1110
6	1	1	0	0	1100
7	1	0	0	0	1000
8	0	0	0	0	0000

Q-20 - Give the difference between Synchronous and Asynchronous counters.

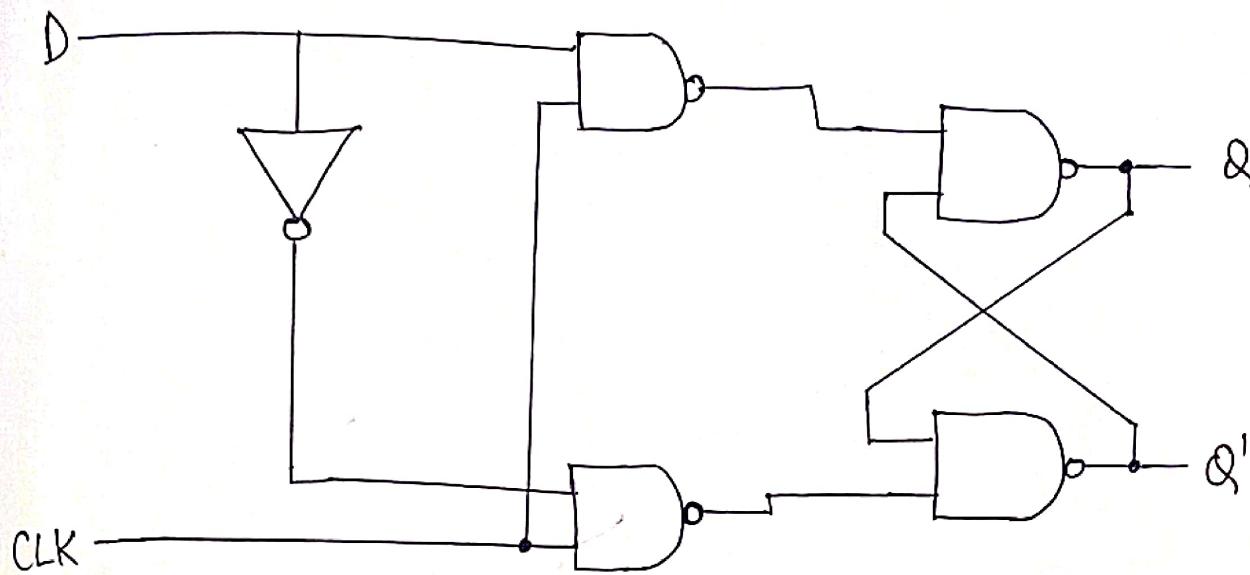
Ans - Difference -

Synchronous Counters	Asynchronous Counters
(1) The propagation delay is very low.	(1) Propagation delay is higher than that of synchronous counters.
(2) Its operational frequency is very high.	(2) The maximum frequency of operation is very low.
(3) These are faster than that of ripple counters.	(3) These are slow in operation.
(4) Large number of logic gates are required to design.	(4) Less number of logic gates required.
(5) High cost.	(5) Low cost.
(6) Synchronous circuits are easy to design.	(6) Complex to design.
(7) Standard logic packages available for synchronous	(7) For asynchronous counters, standard logic packages are not available.

Q-21 - Explain D- flip flop with diagram and make its state table.

Ans - D - flip flop - A D - flip flop is a type of digital circuit that stores a bit of information. It has one input, D (Data), two outputs,  $Q$  and  $Q'$ . The D flip-flop captures the input data on the rising edge of the clock signal (CLK).

D- Flip flop Diagram - The D flip-flop can be implemented using logic gates, typically NAND or NOR gates, or using a master-slave configuration.



Circuit Diagram of D flip flop using NAND gate

State Table of D- flip flop :-

Trigger	Inputs	Output				State
		present state	Next State	$Q$	$Q'$	
CLK	D	$Q$	$Q'$	$Q$	$Q'$	
	0	0	1	0	1	No change
[ <u> ]</u>	0	0	1	1	0	Reset
	1	0	1	0	1	No change
[ <u> ]</u>	1	1	0	0	1	Set