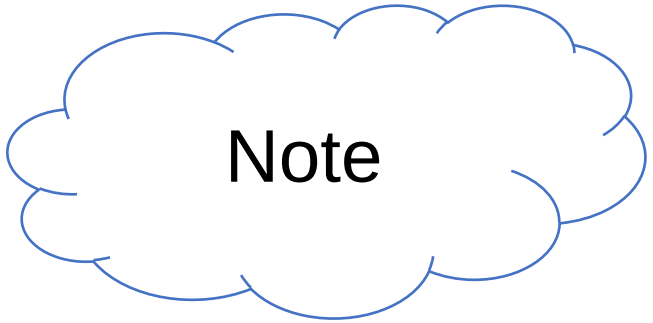

Lab11 Exercise

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Date：2025/05/15

Outline

- 00_TESTBED
- 01_RTL
- 02_SYN
- 03_GATE
- 04_MEM
- 05_APR
- 06_POST
- Avoid DRC violation after nanoRoute

00_TESTBED

- Put the pattern you use in 00_TESTBED
- Include all memory.v in filelist.f

```
TESTBED.v
../04_MEM/MEM_IMAGE.v
```

Modify this part like this if you use TA's code

01_RTL

- Use TA's RTL code
  - Prepare MEM_IMAGE.v in 04_MEM
  - Execute ./01_run_rtl
- Use your own RTL code
  - Remove the soft link named MVDM.v
  - Upload your code named MVDM.v
  - Prepare all memory.v in 04_MEM
  - Execute ./01_run_rtl

02_SYN

- Modify target_library and link_library in .synopsys_dc.setup
- Modify the synthesis cycle time in syn.tcl
- Execute 01_run_dc_shell

```
set company "iclab"
set desinger "Student"

set search_path         " ./ \
                        ../01_RTL                       \
                        ../04_MEM                       \
                        ~iclabTA01/UMC018_CBDK/CIC/SynopsysDC/db/    \
                        ~iclabTA01/UMC018_CBDK/CIC/Sdb/          \
                        /usr/cad/synopsys/synthesis/cur/libraries/syn/ \
                        /usr/cad/synopsys/synthesis/cur/dw "
set target_library      " fsa0m_a_generic_core_ss1p62v125c.db \
                          fsa0m_a_generic_core_ff1p98vm40c.db \
                          fsa0m_a_t33_generic_io_ss1p62v125c.db \
                          fsa0m_a_t33_generic_io_tt1p8v25c.db \
                          L1_WC.db \
                          L0_WC.db"
set link_library        " * $target_library dw_foundation.sldb standard.sldb L0_WC.db L1_WC.db"
set symbol_library      " *.sdb "
set synthetic_library   " dw_foundation.sldb "

set verilogout_no_tri true
set hdlin_enable_presto_for_vhdl "TRUE"
set sh_enable_line_editing true
history keep 100
alias h history
```

Modify this part like this if you use TA's code

03_GATE

- Execute ./01_run_gate

04_MEM

- Use TA's RTL code
  - Memory used has been generated in Memory/ftclib_200901.2.1/EXE
  - Memory name: L0 L1
  - Copy L0 L1 .v / .db / .lef / .lib to 04_MEM
- Use your own RTL code
  - Prepare all_your_memory.v / .db / .lef / .lib in 04_MEM

05_APR

- Put all Memory.lef in 05_APR/LEF
- Put all Memory_WC.lib & Memory_BC.lib in 05_APR/LIB
- Follow APR steps in APR_flow_2025S.pdf
  - You can execute ./01_setenv to set OA_HOME
  - You can source apr_setting.cmd after you activate Innovus

```
05_APR]$ ./01_setenv
```

```
#!/bin/csh
setenv OA_HOME /RAID2/cad/cadence/INNOVUS/INNOVUS_20.15.000/share/oa
```

```
[INFO] Loading Pegasus 21.21 fill procedures
innovus 1> source ./cmd/apr_setting.cmd
```

```
##############################################
############  APR UMC018 setting ############
##############################################
set init_design_uniquify 1
setDesignMode -process 180
suppressMessage TECHLIB 1318
suppressMessage ENCEXT-2799
```

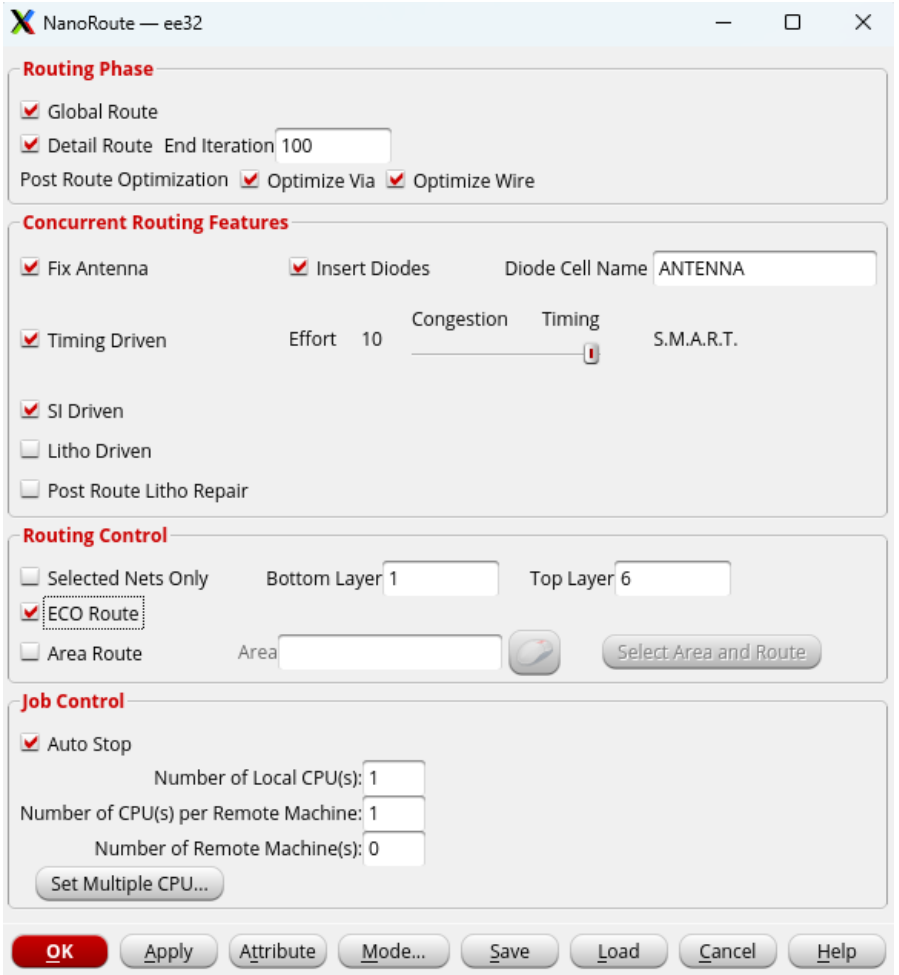
06_POST

- Execute ./01_run_post

Avoid DRC violation after nanoRoute

- End Iteration: more than once!
- Post Route Optimization
  - Turn on Optimize Via & Optimize Wire
- Routing Control
  - Turn on ECO Route

If you still have some DRC violation after nanoRoute with these settings, TA will suggest you should redo APR flow



Thanks