NYCU-EE IC LAB – SPRING 2025

Lab12 Exercise

Design: APRII for Static Timing Analysis

Data Preparation

1. Extract file from TA's directory:

   % tar xvf ~iclabTA01/Lab12_2025S.tar

2. The extracted LAB directory contains:

   a. **00_TESTBED**

   c. **05_APR**

   d. **06_POST**

   e. **09_SUBMIT**

Design Description

In this lab you will finish the **backend flow (APR)** for **Lab03 (TA provided netlist files)** and use the **IR drop** and **Power Analysis** tool for your layout.

Inputs and Outputs

The following are the definitions of input signals

Input Signals	Bit Width	Definition
clk	1	Clock.
rst_n	1	Asynchronous active-low reset.
in_valid	1	High when the input is valid.
delay	4	The delay for each input, output and logic. Value is ranged from 0 to 15.
source	4	The node ID of the source for each wire. Value is ranged from 0 to 15, except 1. (Output cannot be source)
destination	4	The node ID of the destination for each wire. Value is ranged from 1 to 15. (Input cannot be destination)

The following are the definitions of output signals

Output Signals	Bit Width	Definition
out_valid	1	High when out is valid.
worst_delay	8	The worst-case delay
path	4	The node ID of critical path. Should started from Input (ID: 0) and end at Output (ID: 1)

Layout Specifications

1. CHIP.sdc period is fixed to **11ns** and input/output delay is fixed to **5.5ns**
2. Floorplanning
   - Core size:
     - Defined by you
   - Core to IO boundary:
     - Each side must be larger than 100
3. Power Planning
   - Core Ring
     - Top & Bottom: metal layer must be **odd** and **width is fixed to 9**
     - Left & Right: metal layer must be **even** and **width is fixed to 9**
     - Each side must be **wire group**, **interleaving**, and at least **5 pairs**
   - Stripes
     - Horizontal: metal layer must be **odd** and **width at least 2**
     - Vertical: metal layer must be **even** and **width at least 2**
     - The maximum distance between two stripes or stripe and edge should be less than **200**
4. Timing Analysis
   - Timing Slack:
     - **No negative slacks** after setup/hold time analysis (Post-Route stage)
   - Design Rule Violation (DRV)
     - **The DRV of (fanout, cap, tran) should be all 0** after setup/hold time analysis
5. Design Verification Result
   - LVS: **No LVS violations** after "verify connectivity"
   - DRC: **No DRC violations** after "verify DRC"
   - Note: Remember to check DRC / LVS again after placing the fillers.

     Although in normal cases, if DRC and LVS are verified after nanoRoute, no more DRC / LVS will be produced during postRoute optimization and adding core filler. However, some special cases produce the further DRC and LVS.

     For example: inserting a filler that is isolated from all other cells and power lines, then open LVS occurs. Thus, be sure to verify all the specs above after performing all APR steps.
6. Post Layout Simulation:

   The post-simulation cannot include any timing violations without the **+notimingcheck** command.
7. Rail Analysis:
   - VCC Threshold set to **1.7**

- GND Threshold set to **0.1**
- No IR drop is allowed larger than **1mV**

Grading Policy

- **You should meet all the Layout Specification and File Specification above, pass post simulation without any timing violation, and within tolerable IR drop to pass the demo.**
- **1st demo grade: 100 points**
- **2nd demo grade: 70 points**

Note

1. Complete CHIP.io and CHIP_SHELL.v
2. Do all the flow as in APRI (Lab11) with Layout Specification above
3. Run Power Analysis (Setup & Run)
4. Run Rail Analysis
   - Set PG Library Mode
   - Generate PG Library
   - Setup & Run Rail Analysis
5. Observe the IR Drop to analyze whether IR drop is within **1mV**.
6. Please submit your files under **09_SUBMIT** and **a report to the E3 system**:
   - 1st_demo deadline: 2025/6/2 (Mon.) 12:00:00
   - 2nd_demo deadline: 2025/6/4 (Wed.) 12:00:00
   - The report should include screenshots and brief explanations. All necessary information is included in **"Lab12_report_example.docx"**. Your report needs to be named as **"Lab12_report_iclabXXX.pdf"**.
   - If uploaded files violate the naming rule, you will get **5 deduct point**.

   After that, you should check the following files under 09_SUBMIT/Lab12_iclabXXX/
   i. **CHIP_iclabXXX.inn**
   ii. **CHIP_iclabXXX.inn.dat (this one is a directory)**
   iii. **CHIP_SHELL_iclabXXX.v**
   iv. **CHIP_iclabXXX.io**

   If you miss any files on the list, you will fail this lab.

   Then use the command like the figure below to check the files are uploaded or not
7. **Self-Verify APR Result!!! Remember to restore and check the checklist.**