EECE 2160 - Embedded Design: Enabling Robotics

Fall 2016 – Homework #3
Due: November 12 (end of day)

Instructions:

- Please type your solutions into a document and convert it into a PDF file. Your solution document should contain your name, student ID, the course name, and homework number. Submit (on Blackboard) a single PDF file with all your work.
- You may discuss concepts with your classmates. This fosters group learning and improves the class' progress as a whole. However, make sure to submit your own independent and individual solutions.

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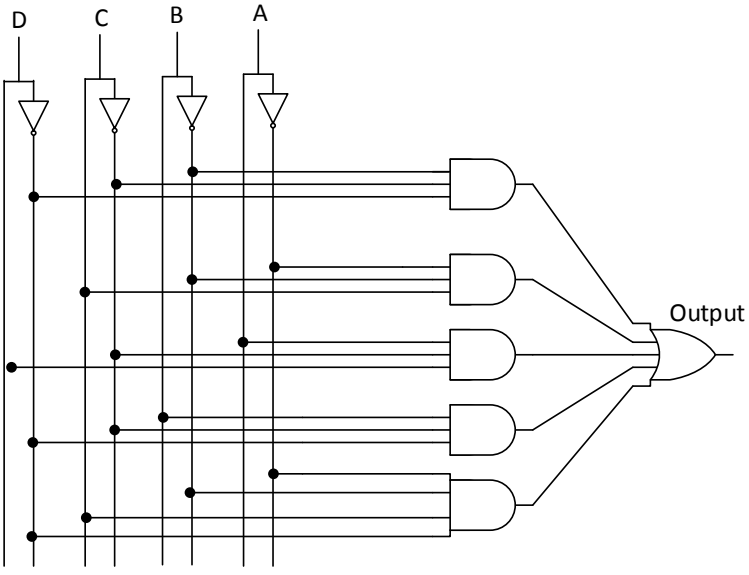
1. (15 points) Provide the CMOS circuit diagrams for the following combinational circuits and Boolean expressions:
   a. A 2-input XOR gate
   b. A 3-input NAND gate
   c. $F = (A \cdot (B + CD))'$

2. (20 points) Simplify the following Boolean expressions (without K-map):
   a. $xyz + x'y + xyz'$
   b. $(x + y)' \cdot (x' + y')$
   c. $A'C' + ABC + AC'$
   d. $(A + B)' \cdot (A' + B')'$

3. (25 points) Minimize the output of the following circuit using K-map and draw your final design just by using NAND gate. Show the procedure of minimization using K-map clearly (1-find the output, 2-draw K-map, 3-find the minimized form, 4-transform the output in NAND form, and 5-draw final minimized circuit using NAND gates).



4. (5 points) Minimize the following function using K-map.

$$f(A,B,C,D) = \sum(1,5,6,7,11,12,13,15)$$

Digital Design with Simulink

5. (25 points) Design a combinational circuit that compares 2 2-bit unsigned binary numbers, and produces 3 outputs indicating whether the first number is less than, greater than or equal to the second number. Use a Karnaugh Map to minimize your design for each output. Input this design in Simulink and make sure that it works.

6. (10 points) Design and test the following using Simulink:

   a.) A 3-to-8 decoder out of 2-to-4 decoders
   b.) A 4-to-1 multiplexor out of 2-to-1 multiplexors