Shizun Ge

Contact

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Skills

Software

C++
C
Go
Tcl
Python
Matlab
CUDA
Embedded Linux device driver
OpenCV
OpenGL

FPGA

Verilog
SystemVerilog
Static Timing Analysis
FPGA-based prototyping
Protocompiler
Certify
Synplify
Identify
VCS-MX
Verdi
Xilinx Vivado
Intel Quartus Prime

Recent coursework

IO Concepts and Protocols: PCI Express, Ethernet, and Fibre Channel • Jitter Essentials • Linux Device Drivers, Advanced • Linux Performance in the Cloud and Data Center • System Virtualization Fundamentals • SystemVerilog OOP Testbench • SystemVerilog Assertions and Formal Verification •

Career summary

- **Software** developer with work experience in object oriented programming, GPU programming and scripting.
- **FPGA RTL** developer with work experience in all aspects of FPGA implementation, including design partitioning, synthesis, place and route, timing analysis, IP integration, verification and bringup.

Experience

9/2018-Present **Software Engineer**
Google LLC, *Sunnyvale, CA*
- Developed a reference model for the next generation TPU using **C++**
- Designed and developed a co-simulation framework for FPGA products using **C++** and **SystemVerilog**
- Developed tools and test cases for hardware diagnostics in the platform infrastructure team, using **Go**, **C++** and **Python**

8/2013-9/2018 **R&D Engineer, Staff**
Synopsys, Inc., *Mountain View, CA*
- Designed and implemented software and hardware integration features using **C++**, **Verilog**, and **scripting**
- Led projects of distinguishing technology HSTDM of HAPS prototyping system, resulting in full adoption of HSTDM and success at customer sites
  - Designed and implemented time-division multiplexing (TDM) IP in **Verilog** based on Xilinx Select IO on **Xilinx Virtex7** and **Ultrascale** platform
  - Optimized the IP to achieve 2.4Gbps over a signle-ended channel between two FPGAs, which is the maximum bitrate supported by the hardware
  - Developed an IP insertion flow using **C++** and **C**
  - Developed various **Tcl scripts** helping internal and external customers develop, debug, bringup and monitor FPGA prototyping system
- Implemented a runtime software framework and IPs for SystemVerilog direct programming interface (DPI), using **C++** and **Verilog**
- Coordinated multiple teams cross geographical coordinations, including software team, firmware team, hardware team, and testing team, as well as external vendors and customers

10/2012-8/2013 **Software Engineer**
Minor Studios Interactive LLC, *Los Angeles, CA*
- Developed real time high-definition video processing program using **C++**, **CUDA**, **OpenCV**, and **OpenGL**

9/2011-9/2012 **Research Assistant**
Boston University, *Boston, MA*
- Developed error control codes algorithm to prevent side-channel attacks, modeling in **C** and **Matlab**, implementing in **Verilog** and **Cadence Encounter**

Education

5/2019 **Certificate** Embedded Systems
UCSC Silicon Valley Extension, *Santa Clara, CA*

9/2012 **Master of Science** in Computer Engineering
Boston University College of Engineering, *Boston, MA*

5/2010 **Bachelor of Engineering** in Electronic Engineering
The Chinese University of Hong Kong, *Hong Kong SAR*