**Technion**

*Electrical Engineering Department*

High Speed Digital System Lab

Image Manipulation Core for FPGA

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# Introduction

## Abstract

Many modern digital devices excute different image manipulations. These manipulations requires image rotation and zooming.

Image Processing algorithms are "heavy consumers" of resources and therefor we would to boost the procces using hardware acceleration.

## Applications

### Pilot Helmets

Modern Day Pilot Helmets contains a digital display module. Due to the helmets geometry, being elliptic and not straight, there's a need to "deform" the displayed image.  
Part of the "deformation" algorithm requires to rotate the image and zooming in/out of the image.  


Figure 1

### Intelligence Surveillance Devices

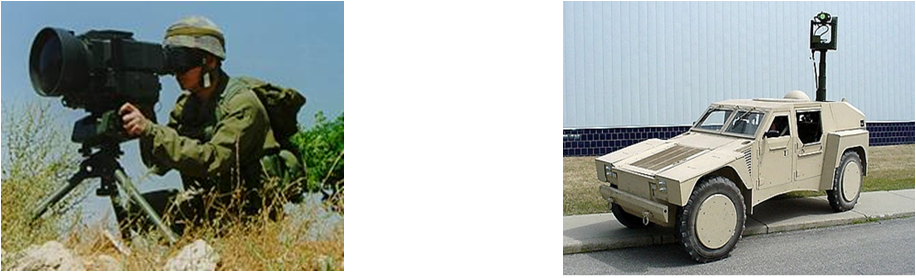
Security forces use different surveillance devices, and sometimes due to terrain conditions there is a need to rotate the image in order to make make the surveillance more comfortable.  


Figure 2

### Surgical Applications

Tiny cameras and Optical fibers are commonly used in various medical procedures. In order to improve the image and ease the procedure image rotation and zooming is necessary.

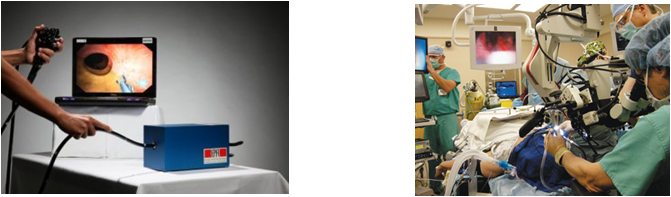


Figure 3

### Printer

New age printers have a built-in LCD display, using our feature the user will have the ability to edit (crop, zoom, rotate) the image before it is sent out to print simply and fast  


Figure 4

# Goals

Implement a FPGA core using VHDL. The core will execute the following objectives

* Full panoramic rotation: 0 to 360 degrees.
* Support of Zoom function.
* Support of crop image by user defined coordinates.

Building a GUI (Graphical User Interface) using Matlab. The GUI will transfer data packets (including the image, required zoom/rotation parameters/crop coordinates) to the FPGA.  
Finally, the GUI will display the output image for Debug purposes.

# Project requirements

* Input Image resolution must be 600x800 and monochromatic.
* Output image resolution will be 480x640.
* Zoom factor must be an integer, power of 2 (i.e. 4,16,32…)
* The rotation angle must be an integer.
* System clock- 133 MHz.
* Vesa (display) clock- 40 MHz.

# The algorithm

להוסיף רקע הסבר על מה זה תמונה במחשב (מטריצה) וכדו'  
  
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The Algorithm executes four operations, where "Crop Input Image"(4.1) is carried out separately before the other function which work simultaneously

## Crop Input Image

The user inputs (x\_start,y\_start) coordinates which describe the top left corner of the required cropped image, where (1,1) leaves the original picture intact.

The algorithm defines a new image which copies the original image matrix starting from  
(x\_start,y\_start) coordinates until the end of the matrix size.  
In case of colored picture, the matrix is three dimensional, the third dimension will be copied according to the same coordinates.

Figure 5 – Example Of Image Cropping

## Image Rotation

The rotation algorithm includes three main stages

* define a black picture with the required input dimensions
* Scanning the output image, pixel by pixel, and calculating the source coordinate of the pixel in original image.

Figure 6 - Example of 30 degree rotation

* Evaluating the grey/color level of the pixel using bi-linear interpolation.

### Calculation of source pixel address

Assume the pixel coordinate in the orginal image matrix is   
For a rotation over an angle ,  in the original image is mapped onto the point in the output image.

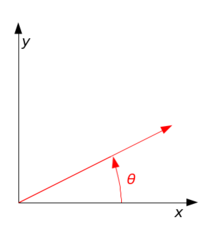


Figure 7 - A counterclockwise rotation of a vector through angle θ

The relation between the points is:



During the algorithm we scan the output image and we evaluate the grey level of the original non-rotated image and therefore we need to use the inverse transform:



Since a matrix cell address is a positive integer we have a problem calculating the source address using this method because cosine and sine functions give real values. Hence we will round up and down the values and evaluate the grey level using bilinear interpolation.

### Bilinear Interpolation

Once we round up the address values a problem rises, we cannot restore the original pixel address in the source image, and therefore we evaluate the grey/color level using bilinear interpolation.  
Bilinear Interpolation performs a weighted average between the four sourrounding neighbours of the required "real" address according to the following method:

* R1, R2 are the weighted averages between the top pair and the bottom pair , accordingly.
* Output is the weighted average between R1 and R2

Figure 8

The following formula describes the bilinear interpolation (weighted average):



## Zoom

### Mathematical background

The zoom function is achieved by using the mathematical operation of scaling the axis. For example- in one dimension: 

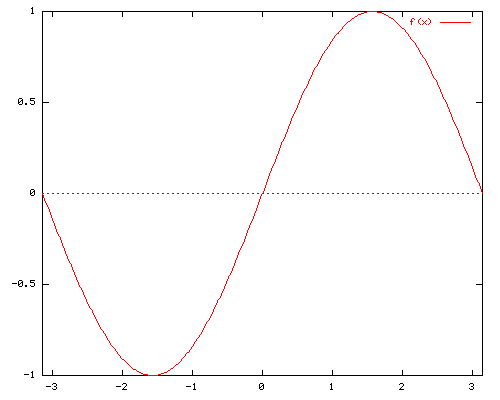


Figure 9

By scaling the X axis with the factor 'a', we receive the follow result:



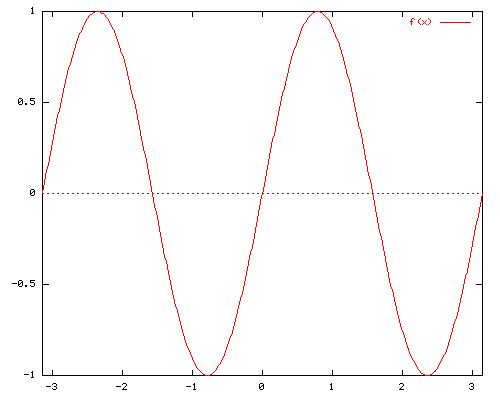


Figure 10



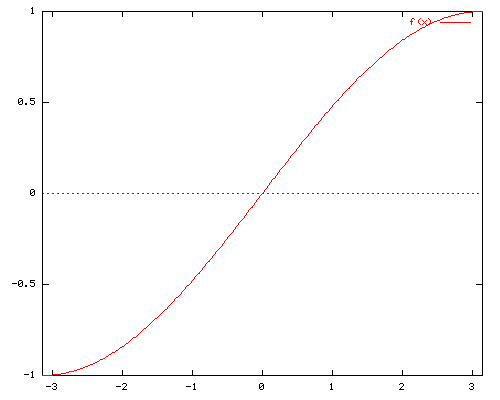


Figure 11

We induct the same principle in two dimensions- (x,y) axis.

### Implementation

In order to zoom in during the scan of the source image, the algorithm multiplies the number of appearances of a source pixel in the output image, according to the zoom factor.

In order to zoom out, in the output image we "skip" every specific amount of pixels in the source image- according the zoom factor. The following formula describes both actions:



## User defined output resolution

The algorithm assumes that the output resolution is smaller or equal to the source resolution. In case the output resolution is smaller, the algorithm shrinks the source image in order to fit it in the new frame. The implementation is identical to the zoom function, only with different factors. The following formula describes the action:



And the same for Y axis.

# General description

## Project's Top Blocks Scheme

## 

The following blocks were reused from a previous project:

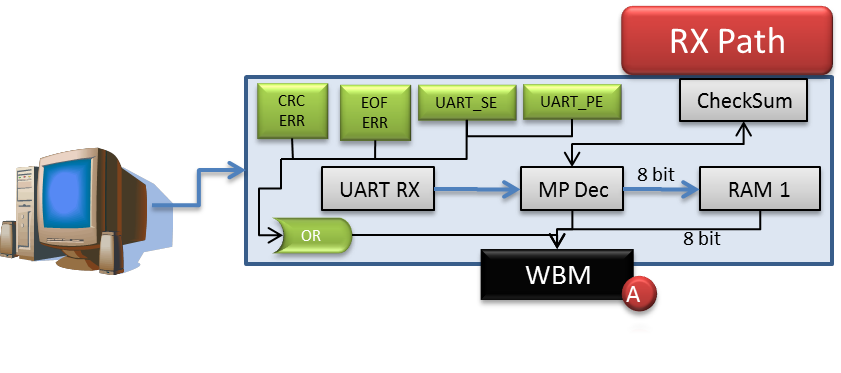
Rx Path, Tx Path, Memory Management, Wishbone Intercon, Display Controller.  
The blocks were adapted to fit our project's needs.

The previous project goal was to display a compressed image (using Run-Length coding), where our project is using a bitmap image so the following changes were made:

* Removing the Run-Length extractor
* Adapting of the Host – creating a GUI that will support our needs
* Creating a new block – Image Manipulation

## Block Descriptions

### Rx Path



This component is used for asynchronous serial data channel.

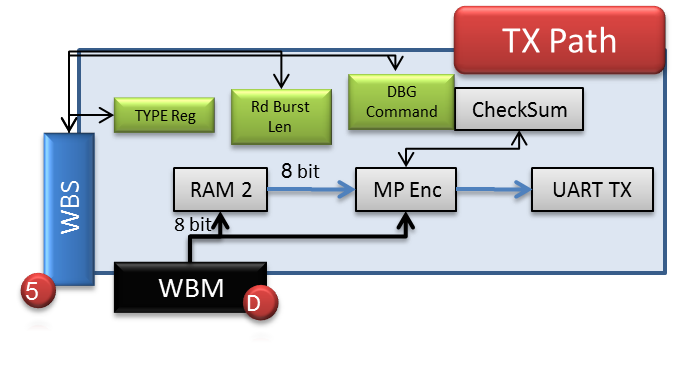
The receiver converts serial start bit, data, parity and stop bit to parallel data.

The data word length can be 5-8 bits, according to generic parameter. Parity bit can be odd or even or if decided can be inhibited, according to generic parameters.

All inputs and outputs are synchronized with the positive edge of the clock.

Any system clock and any baud rate are supported, according to generic parameter.

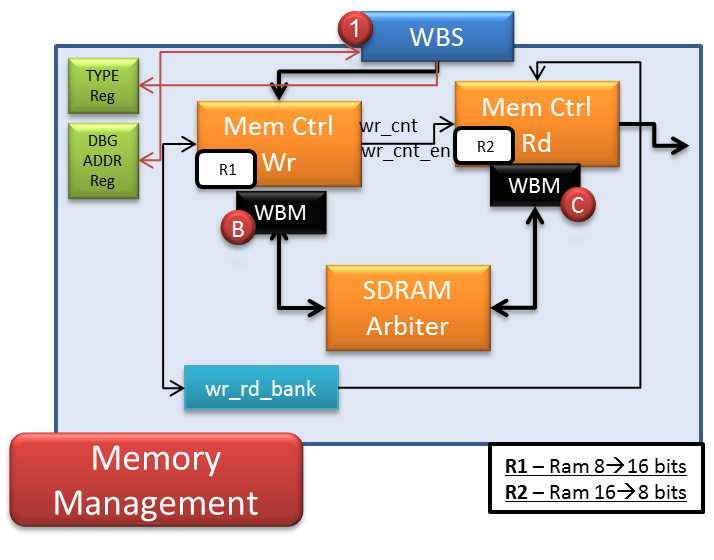
### Tx Path



The transmitter converts parallel data into serial form and automatically adds start bit, parity and stop bit.

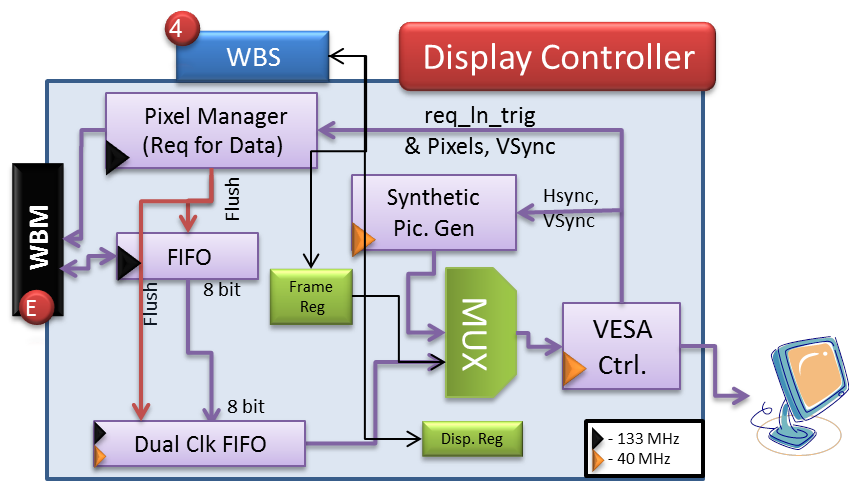
The main use of the component is for debug.

### Memory Management



The Memory Management block is in-charge of writing and reading data from the SDRAM.

### Display Controller



The Display Controller block transmits the data from the SDRAM / Synthetic Picture Generator, through the DAC on the DE2, to the VGA.

The FIFO's depth is 256X2X3 = 1536 (X8 bits), for 3 SDRAM read burst.

The Dual Clock FIFO's depth is 640X6 = 3,840 (X8 bits), for 6 lines.

### Wishbone Interconnector

The system has 3 wishbone interconnectors

* **Intercon Z** - Two Wishbone Masters are connected to this interconnection:

1. WBM (A) from RX Path, which responsible to write data (SDRAM / Registers) to Wishbone Slaves.
2. WBM (D) from TX Path, which responsible to read data (SDRAM / Registers) from Wishbone Slaves.

* **Intercon Y -** This interconnection receives the TYPE register, which is transmitted from the WBM (A). In case of debug mode, WBM (D) will be connected to the path. In case of normal mode, WBM (E) will be connected to the path.
* **Intercon X -** According to WBM (D) command (TGC\_I), routes the path toward reading from SDRAM in the Memory Block or from the registers, through INTERCON (Z)

### Image Manipulation

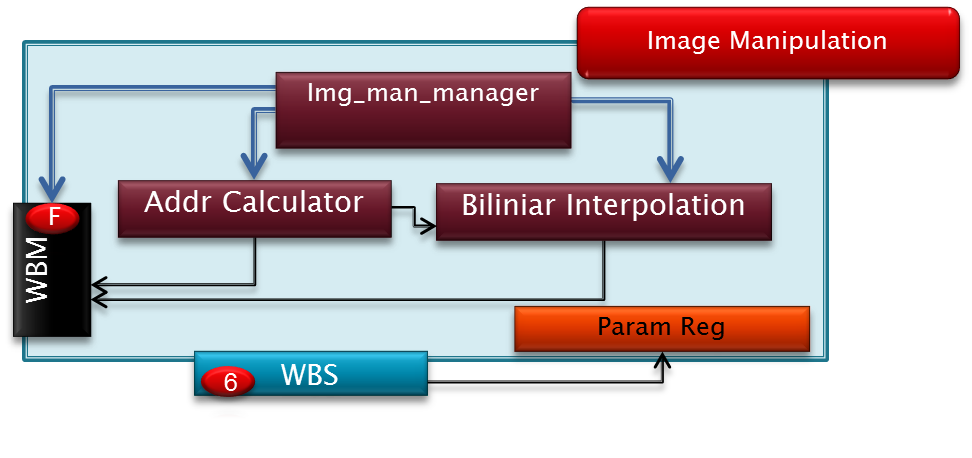


Image Manipulation block is in-charge of rotating, zooming and cropping the image. The blocks receives the data through the Wishbone Intercon, performs the required manipulation and writes it back to the SDRAM via the Wishbone Intercon.

The main components of the block are

* ImgMan Manager – controller for the image manipulation block
* Address Calculator – Calculates "matrix address" of 4 pixels that are required for the bilinear-interpolation and convert the "matrix address" into a "1D" SDRAM address.
* Bilinear Interpolator – Calculates a mean average between 4 pixels
* Parameters Register – holds the user parameters: angle, ROI indexes (Xstart, Ystart), Zoom.

## Data flow

**Host** transmits wrapped message of data packets, composed of bitmap image and user parameters to the **RX Path**. Message is decoded, transmitted to the **Memory Management** block, and stored into **Storage Device** (parameters into registers, image to the SDRAM). Data is read from the memory, sent to image manipulation block, and rewritten to the SDRAM. Then the manipulated image is transmitted to the **Display** through the **Display Controller**.

## Abbreviations

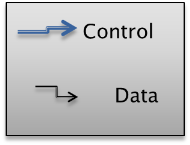
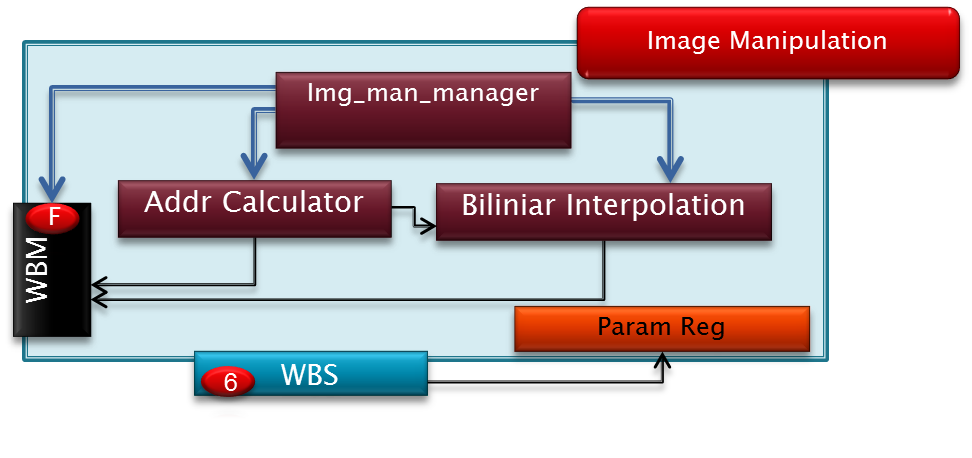
* SDRAM – Synchronous Dynamic Random Access Memory
* RAM – Random Access Memory
* TX – Transmission
* RX – Receive
* FIFO – First in First out
* PLL – Phased Locked Loop
* TB – Test bench
* SOF – Start of frame
* EOF – End of frame
* CRC - Cyclic redundancy check
* MP – Message Pack
* TB – Test Bench
* UART – Universal Asynchronous Receiver Transmitter
* VESA - Video Electronics Standards Association
* VGA - Video Graphics Array
* DVI - Digital Visual Interface
* IP – Intellectual Property

# Implementation

This section contains general information about the coded components in this project, the image manipulation block.

As mentioned before, this block is part of a system which is responsible for writing data to an external memory device and displaying images on a screen via vga protocol.

## Image Manipulation – Top Architecture



The top holds instances of components, parameters registers and the wiring between them. The img\_man\_top itself resides within the mds\_top.

### Parameters Registers

Parameter Registers are located within img\_man\_top.vhd. The registers hold user parameters (such as zoom, crop coordinates etc.) that are required for coordinate calculations in order to execute the image manipulation.

The table below describes all the properties of the registers

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Register's name | Address | Size (bytes) | Purpose | Place |
| Type\_reg | 1 | 1 | Type of message | Mem\_mng\_top, disp\_ctrl\_top, tx\_path |
| x\_start\_reg | E | 2 | X crop coordinate | Img\_man\_top |
| y\_start\_reg | 10 | 2 | Y crop coordinate | Img\_man\_top |
| zoom\_reg | 12 | 2 | Zoom ratio | Img\_man\_top |
| cos\_reg | 14 | 2 | Cosine of rotation angle, multiplied by 0x100 | Img\_man\_top |
| Sin\_reg | 16 | 2 | Sine of rotation angle, multiplied by 0x100 | Img\_man\_top |

**Write to Registers**

***Note***: *Type\_reg should not be written by the software. It is done automatically by the design at each UART message transmission (message = SOF, TYPE … EOF). Type\_reg* *value will be set to the TYPE of the UART message*.

In order to write to register, the following UART message should be sent:

* SOF (=0x64)
* TYPE, where the MSB is '1'. (i.e: 0x80 = write to registers)
* ADDRESS, which is the register's address. (i.e: 2 for dbg\_reg)
* LENGTH, which is the burst length minus 1. (i.e: 2 for dbg\_reg, which is 3 bytes wide)
* PAYLOAD, which is the register's value to be written. (i.e: for dbg\_reg, PAYLOAD might be 0x[01 FA 00] )
* CRC, which is the checksum for TYPE🡪PAYLOAD (inclusive)
* EOF (=0xC8)

This will generate Wishbone Write transaction to the relevant register.

**Register's structure**

The registers are wrapped by *wbs\_reg* component, which translates Wishbone transaction to write / read from a specific register, according to the table above.

## Address calculator

### General Description

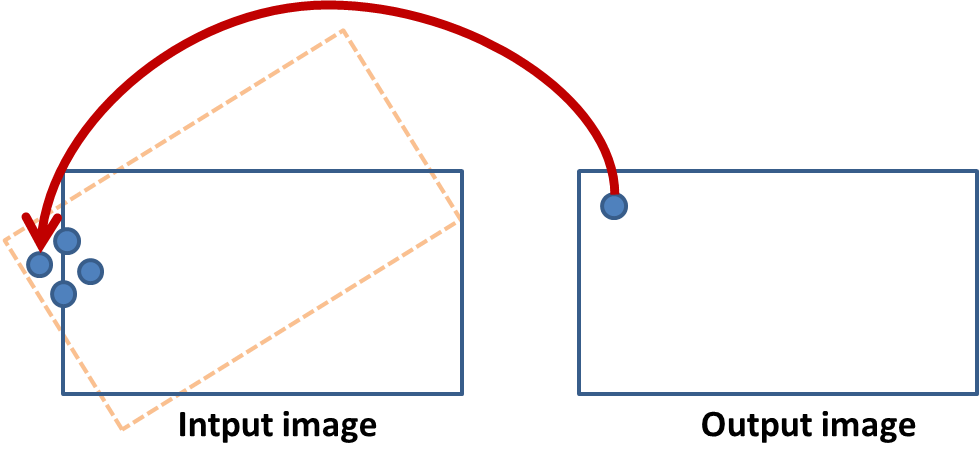
The unit calculates the source pixels address in matrix form a given current position (address, matrix form) in the output image.

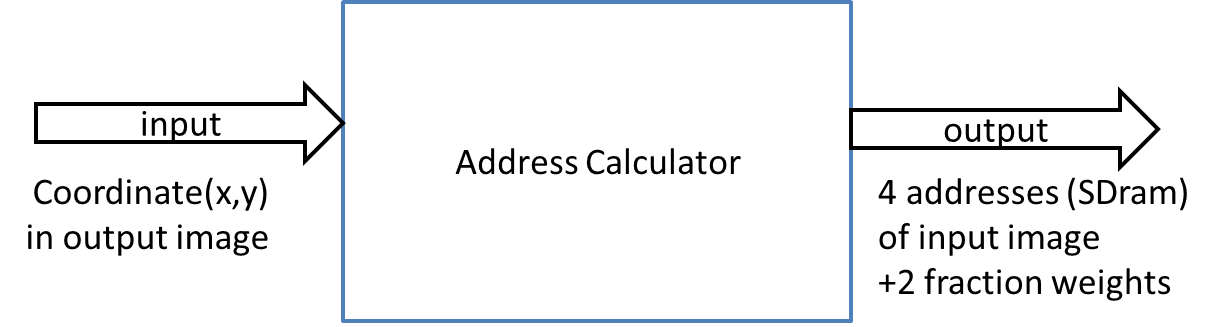
The output is addresses of 4 pixels that are required for the bilinear interpolation.

The input is address of 1 pixel of current position in output image.

**Note: X represents row indexes, Y represents column indexes.**

### Illustration

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### The algorithm

The algorithm calculates the desired coordinates from the origin image, from given [x,y] coordinates. The mathematical equation the algorithm uses is:

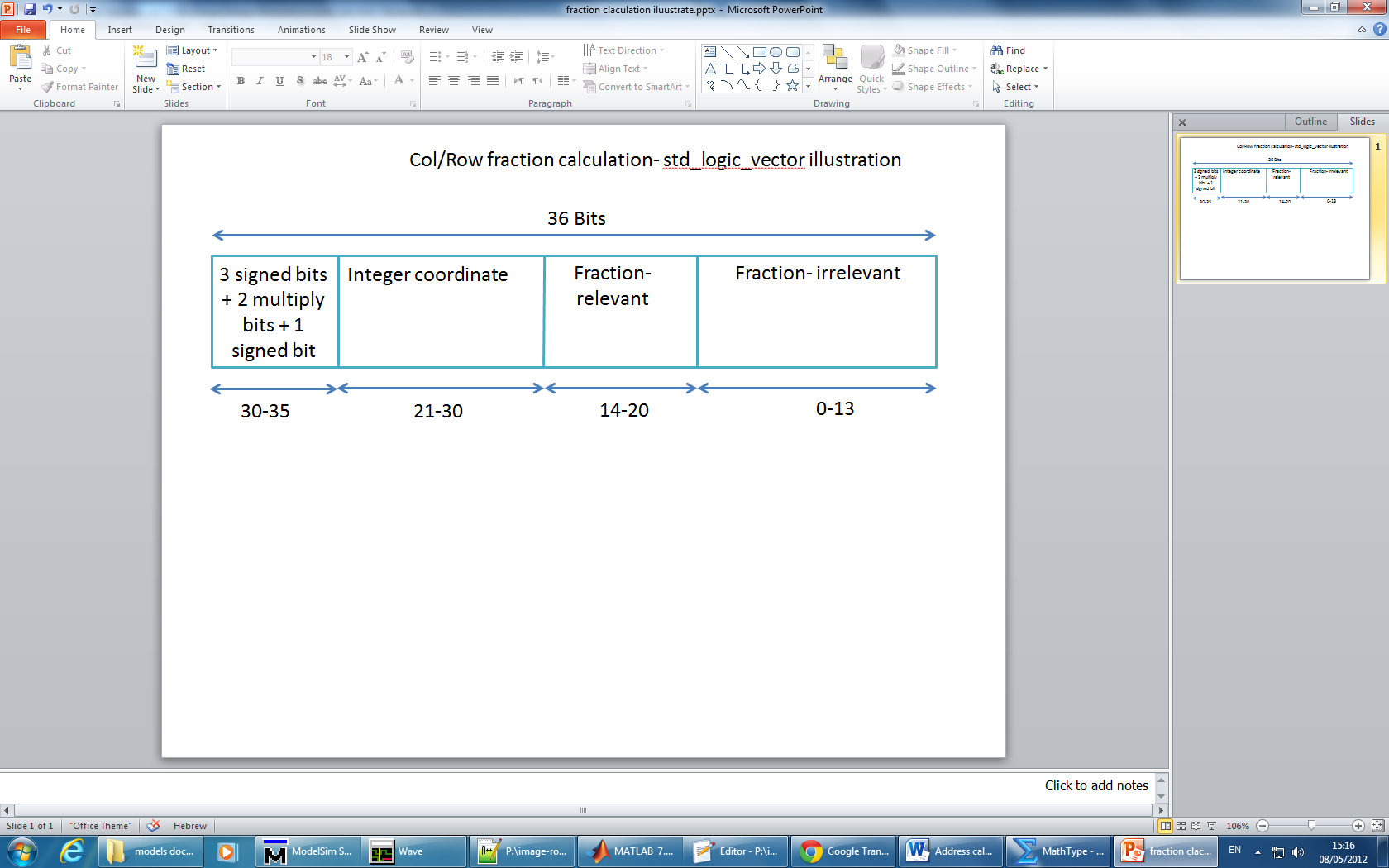


For horizontal calculation the algorithm uses the same equation after replacing the relevant parameters.

In order to reduce calculation time and improve throughput, the algorithm disassembles the equation into 5 parts (Pipeline).

Every multiply operation that should be made, 1 bit must be added to prevent overflow effects (in order to work with std\_logic\_vectors or signed). In addition, the new size must be the size of the two arguments together. Finally, 1 bit of signed type is added (mid calculations might include negative results). Thus, the sizes of output ports were determined.

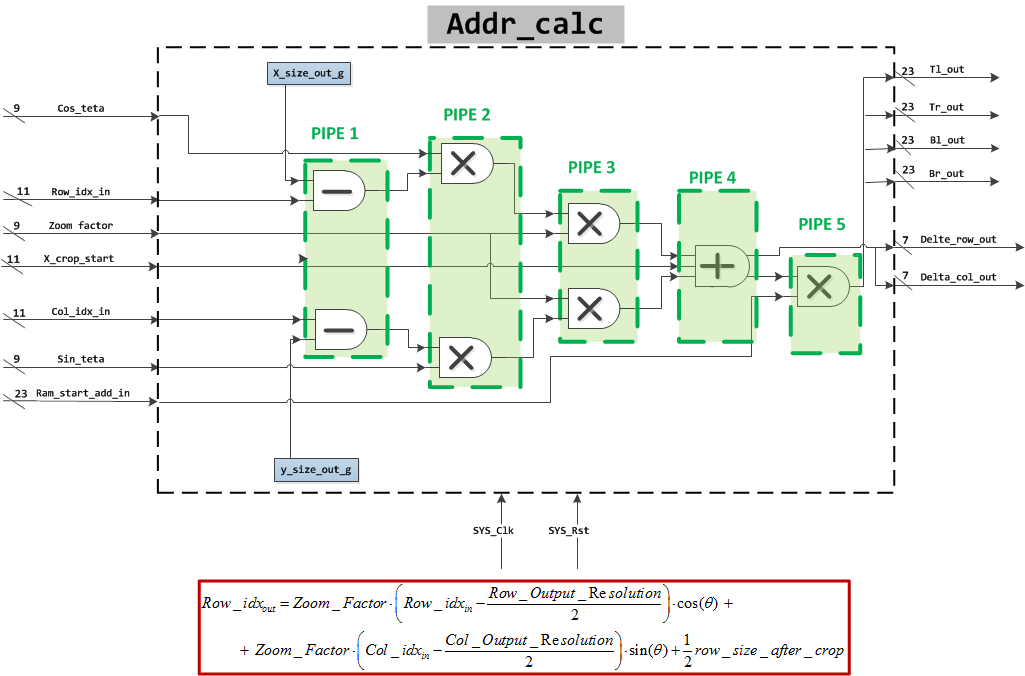
The following image may explain the final output form:



This std\_logic\_vector represent the desired output index in matrix form.

In order to convert this index to SDRAM form, the algorithm uses another simple equation and creates the output index port (23 bits).

### µArchitecture



### Inputs

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Name** | **description** | **type** | **Size(bit)** | **Received from** |
| System\_clk | System clock | Std\_logic | 1 |  |
| System\_rst | System reset | Std\_logic | 1 |  |
| Trigger unit | enable signal for addr\_calc | Std\_logic | 1 |  |
| Zoom\_factor | Holds the zoom factor | signed | 9 (trig\_frac\_size\_g+1 downto 0) | Param\_reg |
| Sin\_teta | Holds sin(teta) | signed | 9 (trig\_frac\_size\_g+1 downto 0) | Param\_reg |
| Cos\_teta | Holds cos(teta) | signed | 9 (trig\_frac\_size\_g+1 downto 0) | Param\_reg |
| Row\_idx\_in | Holds the current row index of the output image | signed | 11 | Param\_reg |
| col\_idx\_in | Holds the current column index of the output image | signed | 11 | Param\_reg |
| X\_crop\_start | Holds the row index of the top left pixel for crop | signed | 11 | Param\_reg |
| Y\_crop\_start | Holds the column index of the top left pixel for crop | signed | 11 | Param\_reg |
| X\_size\_in | Holds the number of rows in the input image | generic | 10 | Img\_man\_top (Mds\_top\_block) |
| Y\_size\_in | Holds the number of columns in the input image | generic | 10 | Img\_man\_top (Mds\_top\_block) |
| X\_size\_out | Holds the number of rows in the output image | generic | 10 | Img\_man\_top (Mds\_top\_block) |
| Y\_size\_out | Holds the number of columns in the output image | generic | 10 | Img\_man\_top (Mds\_top\_block) |

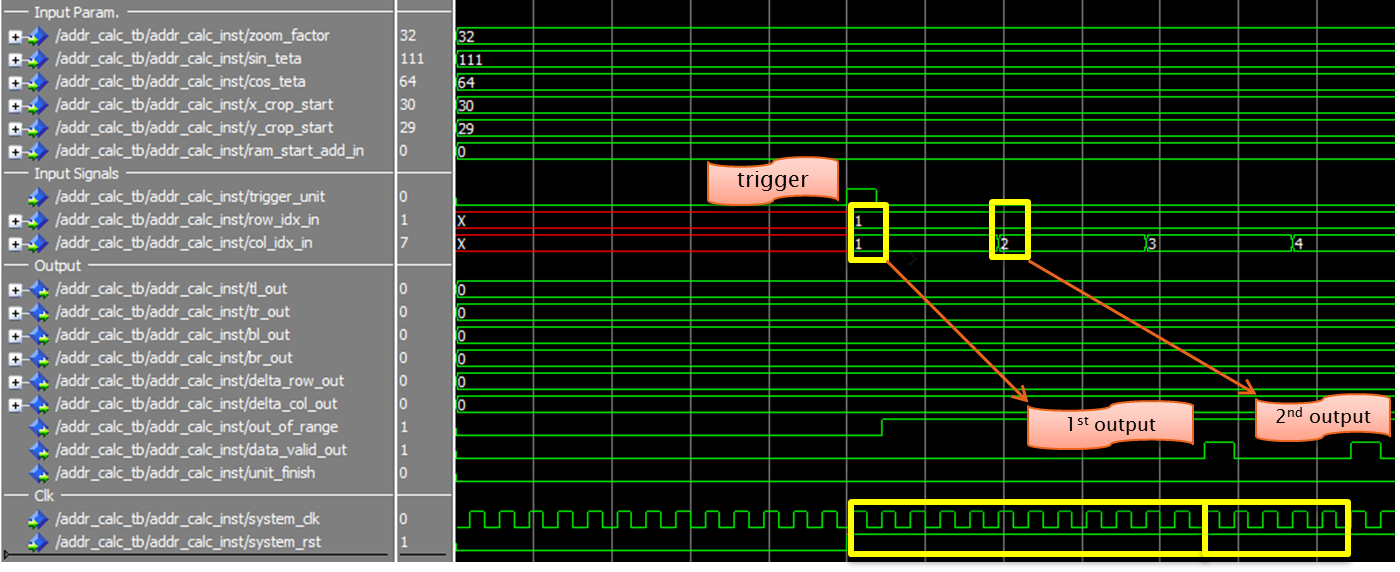
### Outputs

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Name** | **description** | **type** | **size** | **Destination** |
| TL\_out | Holds the top left row index in input image.  Index in SDRAM mode | Std\_logic\_vector | 23 | Img\_man\_manager |
| TR\_out | Holds the top right row index in input image. Index in SDRAM mode | Std\_logic\_vector | 23 | Img\_man\_manager |
| BL\_out | Holds the bottom left row index in input image. Index in SDRAM mode | Std\_logic\_vector | 23 | Img\_man\_manager |
| BR\_out | Holds the bottom right row index in input image. Index in SDRAM mode | Std\_logic\_vector | 23 | Img\_man\_manager |
| delta\_row\_out | Holds the delta of row, for bilinear-interpolation | Std\_logic\_vector | 7 (trig\_frac\_size\_g-1 downto 0) | Bilinear interpolation |
| delta\_col\_out | Holds the delta of col, for bilinear-interpolation | Std\_logic\_vector | 7 (trig\_frac\_size\_g-1 downto 0) | Bilinear interpolation |
| out\_of\_range | Signal indicating when pixel is out of range,  '0' in range '1' out of range | Std\_logic | 1 | Img\_man\_manager |
| Data\_valid\_out | Indicates ready data in outputs | Std\_logic | 1 | Img\_man\_manager |
| unit\_finish | Indicating when block is finish working on current pixel | Std\_logic | 1 | Img\_man\_manager |

Outputs coordinates are 23 bits because 22 bits is the SDRAM size + 1 bit for multiply calculations need.

### Simulations

**first valid output**



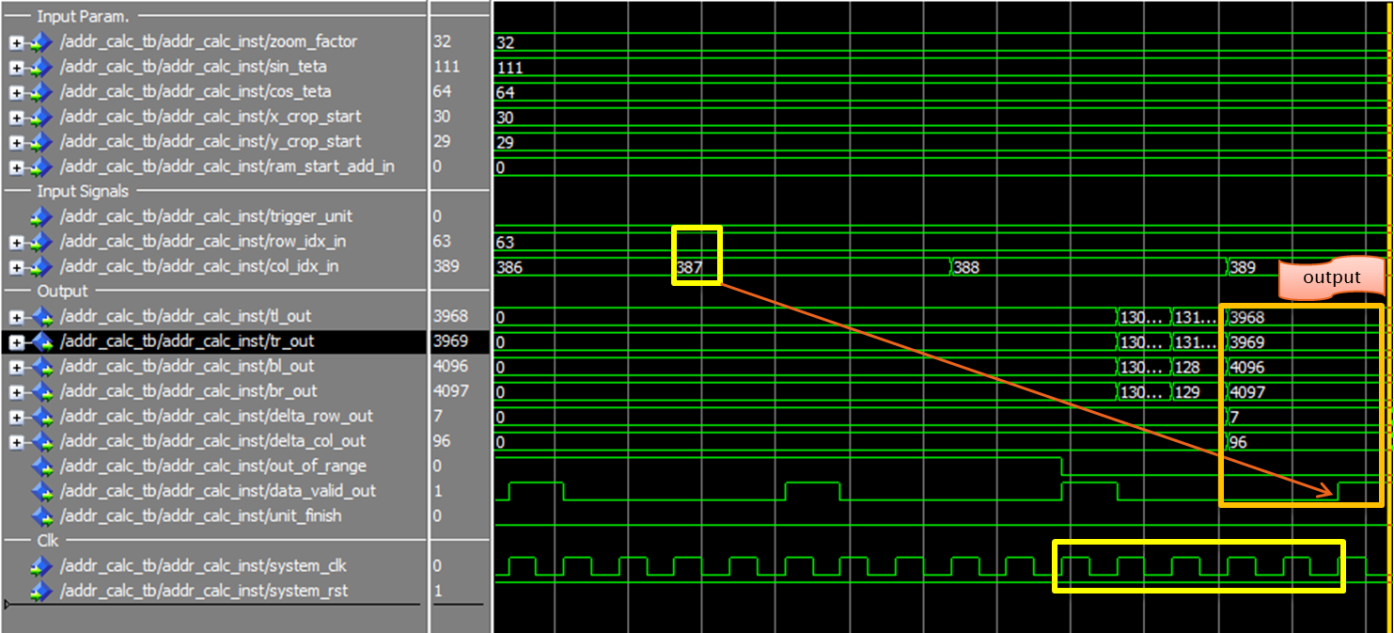
The unit has a 12 cycle latency(number of cycles before the 1st valid result). As shown above, 5 cycles is the throughput of the system (i.e. every 5 cycles a new result is valid).

These values are controlled via generic ports:

* pipe\_depth\_g – number of latency cycles.
* valid\_setup\_g – number of throughput cycles.

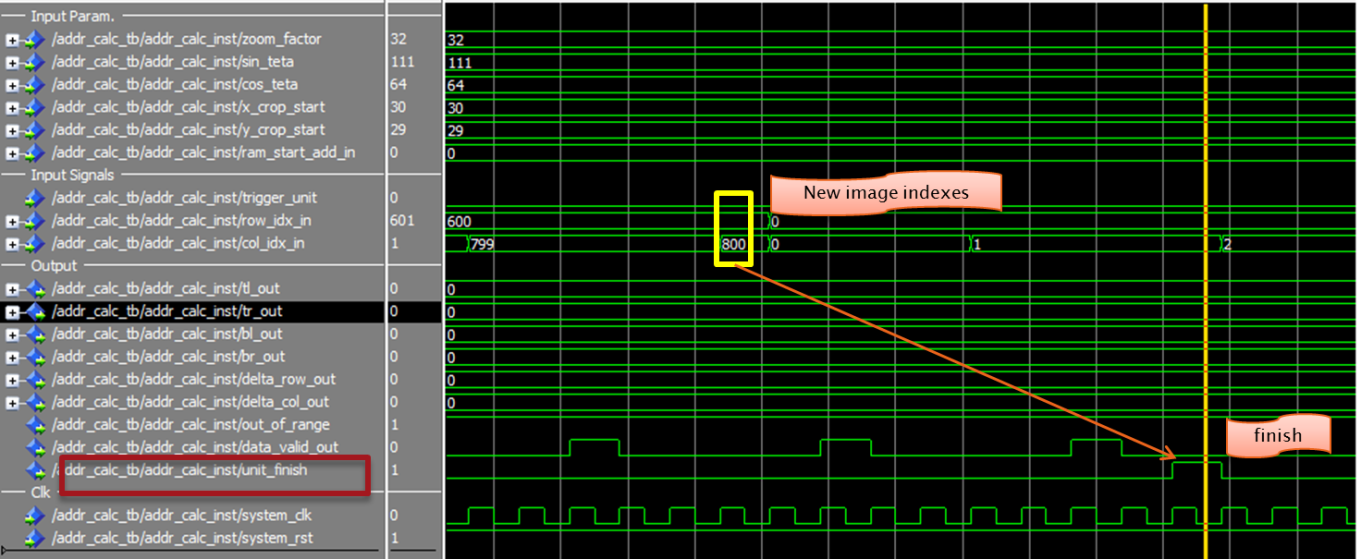
It should be noted that these values were determined after trial and error (simulations) and they should not be changed.

**Midway valid output**



5 cycles between every adjacent result is maintained.

**End of calculation process output**

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finish

A process called *unit\_finish\_proc* is responsible for counting the number of pixels calculated so far. When last pixel is reached a flag named *unit\_finish* is raised.

After the completion a new image may begin its processing.

### Testing

In order to validate the accuracy of the coordinate calculations, a test bench was created. The test bench is written in VHDL, it connects to the *addr\_calc* block and injects test inputs: row and column indexes and user parameters.  
The row and column are generated by a nested loop that emulates the (matrix) coordinates of a 600x800 image.

The output of the *addr\_calc* is written into a text file ("*test\_modelsim.txt*") by the following format:

**col row tl tr bl br d\_row d\_col oor**

310 189 0 0 0 0 0 0 1

311 189 0 0 0 0 0 0 1

312 189 0 0 0 0 0 0 1

313 189 0 0 0 0 0 0 1

314 189 0 0 0 0 120 116 0

315 189 3932 3933 4060 4061 25 56 0

316 189 3932 3933 4060 4061 53 72 0

317 189 3932 3933 4060 4061 80 88 0

318 189 3932 3933 4060 4061 108 104 0

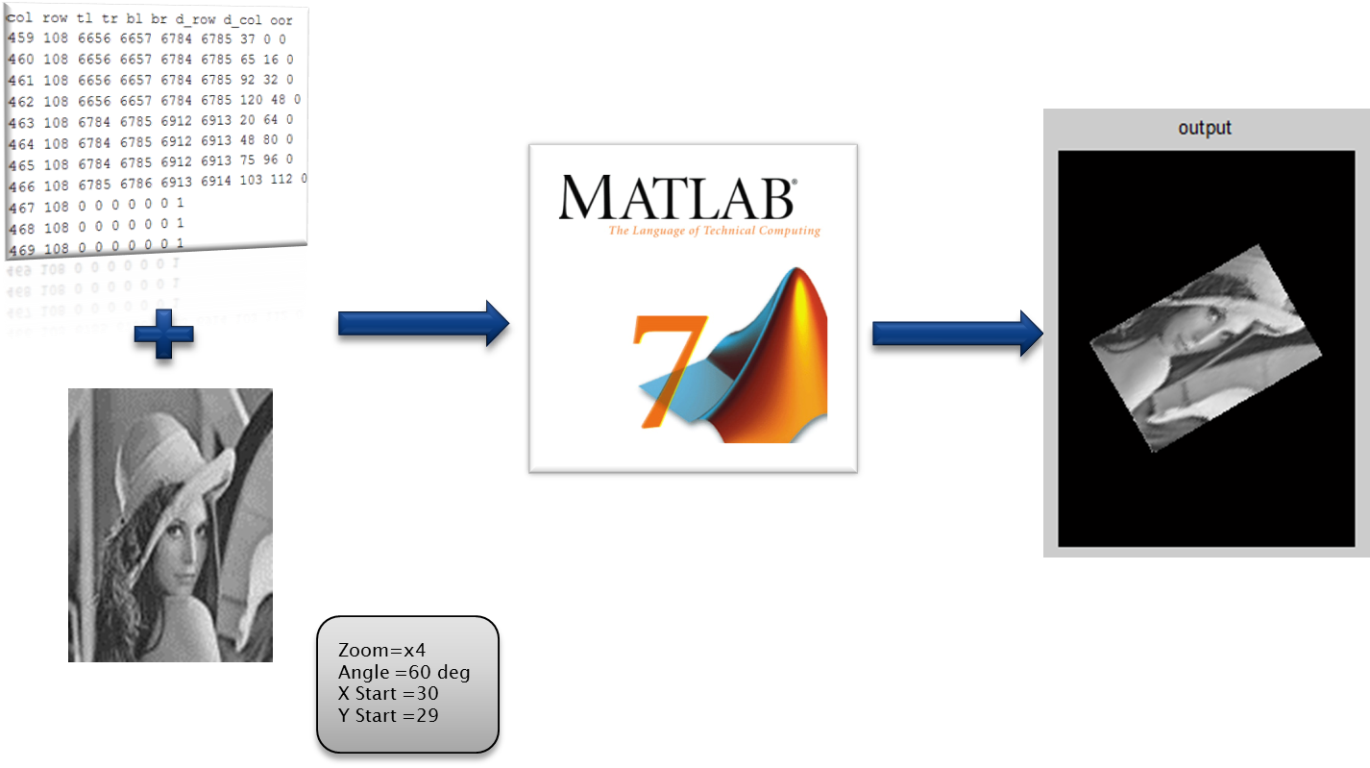
319 189 4061 4062 4189 4190 8 120 0

The next diagram describes the testing process:



The following stage was to inject the text file into a Matlab script ("*test\_addr\_calc\_output.m*") which simulates the full system. The system is simulated by implementing these main features:

* The image resides within the SDRAM ,modeled by 1d array
* Bilinear interpolation is done by Matlab instead of hardware
* The result image is displayed on the screen by Matlab

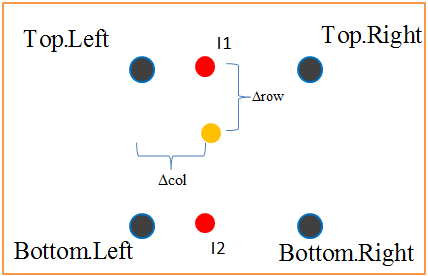


## Bilinear Interpolator

### General description

The unit calculates the mean average of 4 given gray-scale values, achieved by 2 stage calculation.

### The algorithm





The result is greyscale pixel, represented by 8 bits (256 grey levels).

### µArchitecture



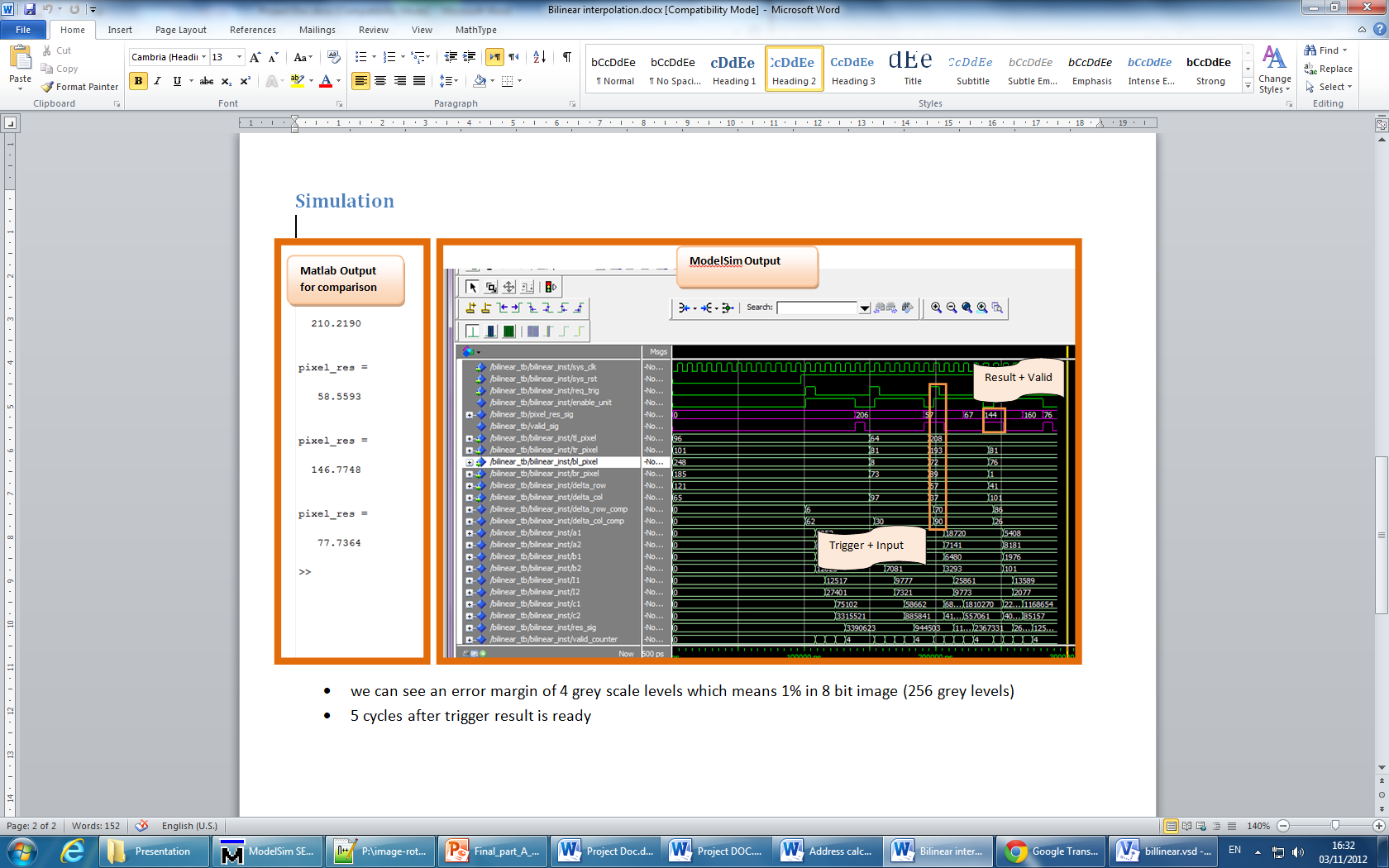
### Inputs

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Name** | **description** | **type** | **size** | **Recived from** |
| Pix\_1\_in | Value of 1st requested pixel | Std\_logic\_vector | 16/**8**? | Local\_register/SDRAM? |
| Pix\_2\_in | Value of 2nd requested pixel | Std\_logic\_vector | 16/**8**? | Local\_register/SDRAM? |
| Pix\_3\_in | Value of 3rd requested pixel | Std\_logic\_vector | 16/**8**? | Local\_register/SDRAM? |
| Pix\_4\_in | Value of 4th requested pixel | Std\_logic\_vector | 16/**8**? | Local\_register/SDRAM? |
| delta\_row | Holds the delta of row, for bilinear-interpolation | Std\_logic\_vector | 7 (trig\_frac\_size\_g-1 downto 0) | Addr\_calc |
| delta\_col | Holds the delta of col, for bilinear-interpolation | Std\_logic\_vector | 7 (trig\_frac\_size\_g-1 downto 0) | Addr\_calc |

### Outputs

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Name** | **description** | **type** | **size** | **Destination** |
| Pixel\_res | Gray scale value for output image | Std\_logic\_vector | 16/**8**? | WB to Sdram |
| Pixel\_valid | Valid signal for result | Std\_logic | 1 | manager |

### Simulation



* we can see an error margin of 4 grey scale levels which means 1.5% in 8 bit image (256 grey levels)
* 5 cycles after trigger result is ready