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Text-only version

Generate Statement

Concurrent Statement ---- used in ----> Architecture

Syntax -

See LRM section 9.7

Rules and Examples

The **for ..generate** statement isd usually used to instantiate "arrays" of components. The **generate** parameter may be used to index array-type signals associated with component ports:

```
architecture GEN of REG_BANK is
  component REG
    port(D,CLK,RESET : in std_ulogic;
        Q : out std_ulogic);
  end component;
begin
  GEN_REG:
  for I in 0 to 3 generate
    REGX : REG port map
        (DIN(I), CLK, RESET, DOUT(I));
  end generate GEN_REG;
end GEN;
```

A label is compulsory with a **generate** statement.

The **for ... generate** statement is particularly powerful when used with integer **generics**.

Instance labels inside a **generate** statement do **not** need to have an index:

-- Illegal

REGX(I):

for .. generate statements may be nested to create two-dimensional instance "arrays".

Another form of **generate** is the **if** ... **generate** statement. This is usually used within a **for** .. **generate** statement, to account for irregularity. For instance, a ripple-carry adder with no carry-in:

```
SUM, CARRY : out bit);
 end component;
  signal C : bit_vector(0 to 7);
begin
 GEN_ADD: for I in 0 to 7 generate
   LOWER_BIT: if I=0 generate
     U0: HALFADD port map
         (A(I),B(I),S(I),C(I));
   end generate LOWER_BIT;
   UPPER_BITS: if I>0 generate
      UX: FULLADD port map
         (A(I),B(I),C(I-1),S(I),C(I));
   end generate UPPER_BITS;
 end generate GEN_ADD;
 COUT \leftarrow C(7);
end GEN;
```

Synthesis Issues

Generate statements are usually supported for synthesis.



In VHDL-93, a generate statement may contain local declarations, followed by the kjeyword begin.

