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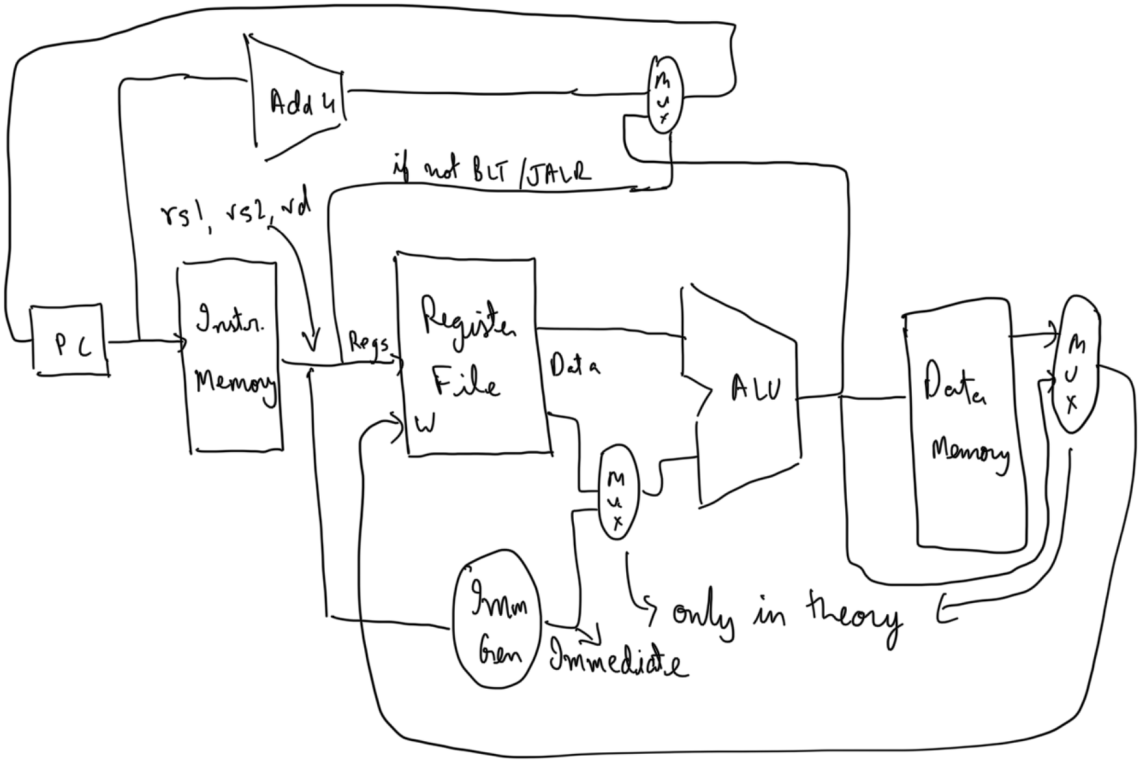
ECE M116C - CA1 Report

Datapath



The phases, from left to right, are Fetch, Decode, Execute, Memory, Register Write, Increase PC.

Control Signal Table

Since my implementation aims to mimic the datapath described in class, the control signals are virtually the same as those in the week 2 discussion slides with some additions.

Instruction	Opcode	RegWrite	AluSrc	Branch	MemRead	MemWrite	MemtoReg	ALUOp
R-type	0110011	1	0	0	0	0	0	func
I-type	0010011	1	1	0	0	0	0	func
lw	0000011	1	1	0	1	0	1	ADD
sw	0100011	0	1	0	0	1	0	ADD
beq	1100011	0	0	1	0	0	0	SUB

All values are the same for BLT as they are for beq in the above table. Additionally, for JALR, the values in the 2nd column onwards are: 1100111, 1, 1, 1, 0, 0, 0, ADD.

Questions

1. What is the total number of cycles for running “all” trace (ZERO instruction included)?

   13 cycles.

2. How many r-type instructions does this program (“all”) have?

   2 r-type instructions (sub and add).

3. What is the IPC of this processor (for “all” trace)?

   IPC = 1, simply because it performs one instruction per cycle.