Shayan (Shaan) Mukherjee

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Education

GEORGIA INSTITUTE OF TECHNOLOGY **Atlanta, GA**
Bachelor of Science in Computer Engineering Expected Graduation May 2027

- **GPA**: 3.5/4.0

Experience

Annapolis Micro Systems **Annapolis, MD**
Software Engineering Intern Aug 2025 - Present

- Developing embedded software in C/C++ for test suites that validate digital signal processing (DSP) boards, switches, chassis managers and I/O cards while incorporating feedback from Test, Hardware, and Firmware teams
- Conduct testing for all updates to Board Support Packages, testing all affected product families before releases
- Creating drivers for an in-house interrupt controller to execute interrupt service routines efficiently

Firmware Engineering Intern May 2025 - Aug 2025

- Designed an in-house interrupt controller in VHDL to tailor interrupt request generation for DSP use cases and reduced FPGA primitive resource utilization (LUTs and Registers) by 33% compared to general Interrupt Controller IPs
- Ensured timing closure in digital logic through pipelining, VHDL refactoring, and logic-level simplifications
- Automated unit tests through Tcl scripts, enabling iterative design cycles, and direct validation of in-house cores

Deca Defense (Remote) **Melbourne, FL**
Hardware Engineering Intern Dec 2024 - May 2025

- Accelerated vision transformer (ViT) architectures for intelligent flight controllers using a Zynq UltraScale+ Kria Board
- Developed a library of ViT primitives with Vitis HLS to tailor architectures to resource constrained FPGA targets

Georgia Tech School of ECE **Atlanta, GA**
Teaching Assistant (TA) Dec 2024 - May 2025

- Taught RISC-V ISA, C/C++ programming, manual memory management, and compiler foundations for ECE 2035
- Hosted 3 hours of office hours weekly to assist students digest content or debug C and RISC-V assembly projects

Secure Hardware Research at Georgia Tech **Atlanta, GA**
Research Assistant (RA) Aug 2024 - May 2025

- Simulated power consumption transients in NGSpice to validate analog and digital electronics in novel ADC designs that randomize power consumption patterns, protecting Single-Slope ADCs against power-rail snooping side-channel attacks
- Automated performance metric acquisition (latency, power, and area) with Tcl scripts, expanding test coverage 10x for stream ciphers in ***Scalable Nonlinear Sequence Generation using Composite Mersenne Product Registers***

Projects

AXI Memory Controller @ Silicon Jackets | *Verilog, Computer Architecture, Tape-out* March 2025 - Present

- Designing the specification and architecture for an AXI-Lite based Memory Controller which allows a custom ASIC processor to initiate stalls for memory access operations, targeting on-chip SRAM memory cells or peripheral devices
- Co-design with Digital Verification and Physical Design teams to optimize the core for performance, power, and area

Peripheral Memory Controller | *VHDL, FPGA Design, RTL Debugging* Nov 2024 - Dec 2024

- Created a 16-bit addressable SPI-based memory controller (64KB capacity) for a RISC architecture targeting the Cyclone V FPGA, featuring memory protection and configurable access modes for byte/half-word addressing
- Validated controller using VHDL Testbench and implemented tri-state drivers in peripheral I/O to keep signal integrity

Vex Robotics Team 2647: "Endgame" | *C++, Git, Controls, Fusion 360, CNC, ROS* May 2019 - May 2023

- Led 2647X to become ***2022 World Skills Challenge Champions*** [video is linked] as the Hardware Design Lead

Skills & Activities

Languages: Java, C/C++, Python, MIPS + RISC-V Assembly, VHDL, SystemVerilog, MATLAB, Tcl
Hardware: MCU (STM32 + Mbed), FPGA (Altera + Xilinx), Power Electronics, Oscilloscope, Waveform Generator
Software: Linux, JTAG, GDB, GoogleTest, Git, Synopsys VCS, ModelSim, Quartus, Vivado, Vitis

Involvements: Silicon Jackets @ GT, Delta Chi Fraternity, Peer Instructor @ The HIVE (ECE) Makerspace
Interests: FPGA projects, Martial Arts, Running, Visiting Parks, Woodworking/3D-Art