Question Bank (Unit -1 Number System)

Write Question No 1 (d), 2(d),3(d),4(c),5(b),6(a),7(b),8(c),9(d),10(c),11(d),12(d),13,17 ,20(a)as Assignment -1- (10) marks

Last Date of Submission: 10/8/2024

1. Subtract following decimal number by 9's & 10's complement method

(a) 274-86 (b) 93-615 (c) 574.6-279.7 (d) 376.3-765.6

2. Convert following binary number to decimal

(a) 1011 (b) 1101101 (c) 1101.11 (d) 1101110.011

3. Convert following decimal to binary

(a) 37 (b) 28 (c) 197.56 (d) 205.05

4. Add the following binary number

a) 11011 + 1101

b) 1011+1101+1001+1111

c) 10111.010 +110111.01

d) 1010.11 +1101.10+1001.11+1111.11

5. Subtract following binary number

a) 1011-101

b) 10110-1011

c) 1100.10-111.01

d) 10001.01-1111.11

6. Convert following octal number to hexadecimal & Binary.

a) 256

b) 2035

c) 1762.46

d) 6054.263

7. Convert following hexadecimal number to octal & Binary.

a) 2AB

b) 42FD

c) 4F7.A8

d) BC70.0E

8. Convert following octal to decimal

a) 463

b) 2056

c) 2057.64

d) 6534.04

9. Convert following decimal to octal

a) 287

b) 3956

c) 420.6

d) 8476.47

10. Convert decimal to hexadecimal

(a) 452 (b) 4796 (c) 1248.56 (d) 8957.75

11. **Convert hexadecimal to decimal.**

(a) AB6 (b) 2EB7 (c)A08F.EA (d) 8E47.AB

11. Convert following binary number to octal & hexadecimal Number

(a) 1011 (b) 1101101 (c) 1101.11 (d) 1101110.011

1's & 2's Complement Method:

12. Add -75 to 26 using 8 bit 2's complement arithmetic .
13. Add -45.75 to 87.5 using 2's complement arithmetic
14. Add 27.125 to -79.625 using 2's complement arithmetic
15. Add 47.25 to 55.75 using 12 bit 2's complement arithmetic
16. Add -75 to 26 using 8 bit 1's complement arithmetic .
17. Add -45.75 to 87.5 using 1's complement arithmetic
18. Add 27.125 to -79.625 using 1's complement arithmetic
19. Add 47.25 to 55.75 using 12 bit 1's complement arithmetic

20. Multiply Following binary numbers

a) 1101*101

b) 11001*10

c) 1101.11*101.1

d) 10110*10.1

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Digital Electronics (EC0319)

(Boolean Algebra Question Bank)

1. Reduce the expression: [(A+B') (C+D')]'
2. Reduce the expression :[(AB)'+A'+AB]'
3. Prove that AB +A'C+BC = AB +A'C
4. Prove that (A+B) (A'+C) (B+C) = (A+B) (A'+C)
5. Prove that AB +A'C =(A+C) (A'+B)
6. Reduce the expression f= A+B [AC+(B+C')D]
7. Reduce the expression f=A[B+C'(AB+AC')']
8. Reduce Expression f= [A+(BC)']' (AB'+ABC)
9. Using Boolean Algebra solve the expression: (B+BC) (B+B'C) (B+D)
10. Show that AB+AB'C+BC' =AC+BC'
11. Prove that AB'C +B+BD'+ABD'+A'C = B+C
12. Prove the following Boolean Expression
    i. ABCD'+A+ABD'+D'(A'B'C') =A+B'C'D'
    ii. A'B (D'+C'D) + B (A+A'CD) = B
    iii. (A'+C) (A'+C') (A'+B+C'D) =A'
13. Simplify following Boolean Expression :X [Y+Z (XY+YZ)']
14. Prove that A+B [AC+(B+C')D] =A+BD
15. Prove that X'YZ+XZ+X'Z = Z
16. Simplify the following Boolean Expression

    (a) (BC'+A'D) (AB'+CD')
    (b) (X'YZ+XZ+X'Z)
    (c) (X+Y)' (X'+Y')
    (d) XY+XY'+X'Y
    (e) Y=(AB+C)(AB+D)

17. Simplify following Boolean expression (using Demorgan's theorem)
    i. [(A+C') (B+C')]' [CD]'
    ii. [[A'BC+ D (AB+C)] A']'

18. Draw Logic Diagram using only NAND Gate to Implement following
    i. F=(AB+A'B') (CD'+C'D)
    ii. F=(A+B') (CD+E')

19. Simplify the following Expression and Implement them with NAND gate Circuits.
    i. F=AB'+ABD+ABD'+A'C'D'+A'BC'
    ii. F=BD+BCD'+AB'C'D'

20. 20.Draw Logic Diagram using only NOR Gate to Implement following function **OR** Implement following function using only NOR Gate :
    i. F=(AB+A'B') (CD'+C'D)
    ii. F=(A+B') (CD+E')

21. Simplify the following Expression and Implement them with NOR gate Circuits.
    i. F=AB'+ABD+ABD'+A'C'D'+A'BC'
    ii. F=BD+BCD'+AB'C'D'

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(K map ,tabulation Method & SOP,POS Question Bank)

1) Obtain the simplified expressions & Find out F & F' in sum of products and product of sum for the Following Boolean functions: F(A,B,C,D,E) =Σ(0,1,4,5,16,17,21,25,29)

2) Simplify the Boolean function using kmap :
(1) F(w,x,y,z) = Σm (0,1,2,4,5, 12,13,)
(2) F =A'B'D'+A'CD+A'BC d=A'BC'D+ACD+AB'D' Where "d " indicates Don't care Conditions

3) Simplify the Boolean function using k-map & implement the expression using NOR & NAND logic. F(w,x,y,z) = Σm (0,1,2,4,5, 12,13)

4) Obtain the simplified expressions for the Following Boolean functions & Implement this logic into AOI logic:
F(A,B,C,D,E) = ⊓M (0,1,2,4,7,8,12,14,15,16,17,18,20,24,28,30,31)

5) Reduce the following expression in SOP form using mapping and implement the minimal expression using NAND and NOR logic F=Σm (0,2,3,10,11,12,13,16,17,18,19,20,21,26,27)

6) Simplify the following Boolean expression using K-map. Implement same using NAND gates only.F(a,b,c,d) = ∑m (0,3,6,7,11,14,15)

7) Minimize the following expression using K-map and and implement the minimal expression using NAND and NOR logic F(A,B,C,D) = ⊓M (4,5,7,12,14,15) +Σd (3,8,10)

8) Minimize the following expression using K-map:F=⊓M(2,3,7,8,9,10,11,12,16,17,18,19,20,21,23,26,27)

9) Obtain the simplified expressions in sum of products for the Following Boolean function, implement this logic into AOI logic and implement the minimal expression using NAND and NOR logic.: (A,B,C,D,E) = ⊓M (0,1,4,5,16,17,21,25,29)

10) Minimize the following expression using K-map and implement this logic into AOI logic and implement the minimal expression using NAND and NOR logic.:
11) F(A,B,C,D) = Σm (1,3,7,11,15)+ Σ d (0,2,5)

12) 11.Obtain the simplified expressions using k-map. *F*(A,B,C,D,E) =Σm(0,1,2,4,7,8,12,14,15,16,17,18,20,24,28,30,31)

13) Obtain the simplified expressions for the Following Boolean functions: F(A,B,C,D,E) = πM (0,1,4,5,16,17,21,25,29)

14) Expand F(A,B,C,D)= A+BC'+ABD'+ABCD to Maxtern & Minterm .

15) Obtain thr product of sum of the function: A (B'+A) B

16) Expand A (A'+B) (A'+B+C') to Maxtern & Minterm

17) Obtain the simplified expressions in sum of products for the Following Boolean functions & Implement it into Kmap : A′B′CE′ + A′B′C′D′ +B′D′E′ + B′C D.

18) Obtain the simplified expressions in SOP form for the following Boolean function & Implement it into Kmap: F(A, B, C, D) = ABD+A'C'D'+A' B+A'CD'+AB'D

19) Obtain minimal expression for Σm (1,2,3,5,6,7,8,9,12,13,15) using tabular method.

20) Minimize the following expression Σm(0,12,8,9,15,17,21,24,25,27,31) using tabular method.

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Unit 3 Combinational Logic design

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1. Explain Half adder& full adder with truth table & logic diagram and kmap.
2. Explain half subtractor and full subtractor with truth table & logic diagram and kmap.
3. Explain 4 bit parallel binary subtractor in detail.
4. Explain 4 bit binary adder -subtractor .
5. Explain 4 bit parallel binary adder in detail.**OR** Design the 4-bit parallel adder.
6. Explain 2 bit magnitude comparator in detail.
7. Explain following Encoder with logic diagram and truth table .
   Octal to binary Encoder
   Decimal to BCD Encoder
8. Explain following Decoder with logic diagram and truth table.
   3 to 8 line decoder
   2 to 4 line decoder
   BCD to seven segment decoder
9. Explain following Multiplexer with logic diagram and truth table.
   2*1 Multiplxer
   4*1 Multiplexer
   8*1 Multiplexer
10. Explain following Demultiplexer with logic diagram and truth table.
    1 to 4 line demultiplexer
    1 to 8 line demultiplexer
11. Design full adder circuit with multiplexer
12. Usa a multiplexer have three data select input to implement the logic for the function given below. Also realize the same using 16:1 MUX
    F= ∑m (0,1,2,3,4,10,11,14,15)
13. Use 4*1 Mux to implement the logic function
    F = ∑m (1,2,4,7)
14. Use 8*1 Mux to implement the logic function
    F = ∑m (1,3,4,11,12,13,14,15)
15. Design 16:1 MUX using 4:1 Mux modules
16. Design 32:1 Mux using two 16:1 MUX and one 2:1 mux modules
17. Design 8 to 1 Multiplexer using 2 to 1 multiplexer.

18. Design a 4 bit binary to gray code converter **OR** Design a combinational circuit that takes 4-bit binary number and produces Gray code of the input.
19. Design a 4 bit gray to binary code converter.
20. Design a SOP circuit to detect decimal numbers 5 through 12 in a 4 bit gray code input.
21. Design a combinational circuit to produce the 2's Complement of a 4 bit binary number
22. Design a circuit to detect decimal numbers 0,1,4,6,7 and 8 in a 4 bit XS-3 code input.
23. Design a logic circuit with 4 inputs A,B,C,D That Will Produce Output '1' only whenever two adjacent input variables are 1s.
24. Design a even parity bit generator for 4 bit input.
25. Design a odd parity bit generator for 4 bit input.

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Unit 3 Flip flop

1. What is the difference between combination circuit and sequential circuit?
2. Explain following flip flop with truth table and logic diagram.
    i. Positive edge triggered S-R flip flop
    ii. Positive edge triggered J-Kflip flop
    iii. Positive edge triggered D flip flop
    iv. Positive edge triggered T flip flop
    v. Negative edge triggered S-R flip flop
    vi. Negative edge triggered J-K flip flop
    vii. Negative edge triggered T flip flop
    viii. Negative edge triggered D flip flop
    ix. Master-Slave (Pulse Triggered) S-R Flip flop
    x. Master-Slave (Pulse Triggered) J-K Flip flop
    xi. Master-Slave (Pulse Triggered) D Flip flop .

3. Convert following flip flop
    S-R flip flop TO J-K flip flop
    J-K flip flop TO S-R flip flop
    S-R flip flop TO D flip flop
    D flip flop TO S-R flip flop
    J-K flip flop TO T flip flop
    T flip flop to J-K Flip flop
    J-K flip flop TO D flip flop
    D flip flop TO J-K flip flop

III Sem

Unit 4 Counter

1. What is difference between asynchronous counter and synchronous counter?
2. Explain two bit ripple up counter using negative and positive edge triggered flip flop
3. Explain two bit ripple down counter using negative and positive edge triggered flip flop
4. Implement 3 bit OR 4 bit ripple (asynchronous)counter using D flip flop.
5. Design following asynchronous counter using T flip and J-K Flip flop.
    I. Mod 6
    II. Mod 9
    III. Mod 10
6. Design synchronous 3 bit up counter using J-K flip flop.
7. Design synchronous 3 bit down counter using J-K flip flop.

III Sem

Digital Electronics

shift registers

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1. Explain following registers with necessary diagram
    I. 4 bit Serial-In Serial-Out Shift Register (with D flip flop , J-K flip flop ,S-R flip flop)
    II. 4 bit Serial-In parallel –Out Shift Register
    III. Parallel-In serial-Out Shift Register
    IV. 4 bit Parallel-In Parallel-Out Shift Register.