F15 VLSI Testing Term Project

Stuck-At Fault Simulation

20151223_v1.1:

1. pattern format file modified (marked in red)
2. evaluation criteria updated (marked in red)

Project Overview

The single stuck-at fault model is the most popular fault model. The objective of this project is to develop a single stuck-at fault simulator that determines the fault coverage with respect to the given fault list and test patterns.

Input Format

The inputs to your program consists of the benchmark circuit, the fault list, and the test patterns.

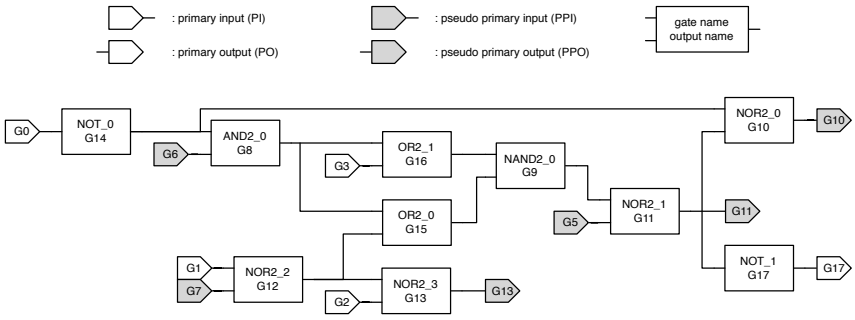
```
//# 4 inputs, 1 outputs, 3 D-type flipflops, 2 inverters
//# 8 gates (1 ANDs + 1 NANDs + 2 ORs + 4 NORs)
module s27(GND,VDD,CK,G0,G1,G17,G2,G3);
input GND,VDD,CK,G0,G1,G2,G3;
output G17;
  wire G5,G10,G6,G11,G7,G13,G14,G8,G15,G12,G16,G9;
  dff DFF_0(CK,G5,G10);
  dff DFF_1(CK,G6,G11);
  dff DFF_2(CK,G7,G13);
  not NOT_0(G14,G0);
  not NOT_1(G17,G11);
  and AND2_0(G8,G14,G6);
  or OR2_0(G15,G12,G8);
  or OR2_1(G16,G3,G8);
  nand NAND2_0(G9,G16,G15);
  nor NOR2_0(G10,G14,G11);
  nor NOR2_1(G11,G5,G9);
  nor NOR2_2(G12,G1,G7);
  nor NOR2_3(G13,G2,G12);
endmodule
module dff (clk, d, q);
input clk, q;
output d;
reg d;
always @(posedge clk) d = q;
endmodule
```

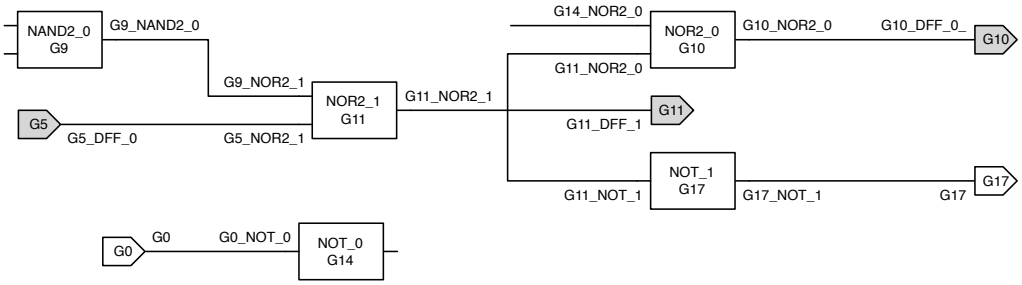
Benchmark Circuits

The gate-level benchmark circuits are in Verilog format. For example, s27.v is given below with its combinational part drawn — note that we ignore the flip-flops and treat their inputs and outputs as pseudo primary outputs (PPOs) and pseudo primary inputs (PPIs), respectively.

The Fault List

First, we name a "net" according to the driving gate's output signal name. For example, the net that connects the output of "NAND_2_0" and the input of "NOR2_1" is "G9". A net driven by a primary input is named after the primary input's name. For example, the net that connects the output of "AND2_0" and the inputs of "OR2_1" and "OR2_0" is named "G8" which is the output name of the driving gate "AND2_0." On the other hand, the net that connects the primary input "G0" to the input of





"NOT_0" is "G0."

Stuck-at faults are associated with wires. In this project, the following wires are considered:

1. Each input of a gate.
2. The output of a gate.
3. Each primary input.
4. Each primary output.

The name of a gate input or output wire is in the form below

NetName_GateName

where "NetName" is the name of the net that the wire belongs to and "GateName" is the name of the gate that contains the wire. For example, the output wire of "NAND2_0" is named "G9_NAND2_0." Pay attention to the case regarding flip-flop inputs and outputs. More examples can be found in the figure below.

In s27, there are 39 wires to consider (listed below); thus, the complete single stuck-at fault list consists of 78 faults.

G0, G0_NOT_0

G1, G1_NOR2_2

G2, G2_NOR2_3

G3, G3_OR2_1

G5_DFF_0, G5_NOR2_1

G6_DFF_1, G6_AND2_0

G7_DFF_2, G7_NOR2_2

G8_AND2_0, G8_OR2_0, G8_OR2_1

G9_NAND2_0, G9_NOR2_1

G10_NOR2_0, G10_DFF_0

G11_NOR2_1, G11_NOT_1, G11_NOR2_0, G11_DFF_1

G12_NOR2_2, G12_OR2_0, G12_NOR2_3

G13_NOR2_3, G13_DFF_2

G14_NOT_0, G14_AND2_0, G14_NOR2_0

G15_OR2_0, G15_NAND2_0

G16_OR2_1, G16_NAND2_0

G17_NOT_1, G17

For each wire, say "XYZ", there are two stuck-at-faults: "XYZ_sa0" and "XYZ_sa1."

Inside the fault list file, each line corresponds to a fault of interest. For example, if we are interested in the faults at the inputs of "NOR2_1", the fault list file will be as follows.

XYZ_f1, 4 faults

G9_NOR2_1_sa0

G9_NOR2_1_sa1

G5_NOR2_1_sa0

G5_NOR2_1_sa1

Note that a line starts with "#" is a comment line and will be skipped.

The Test Pattern Set

In the test pattern file, each pattern is enclosed by a pair of curly bracket, i.e., "{}", in which input signal values (0 or 1) ~~separated by space(s)~~ are specified. Note that the input signals are named after the net names and they are ordered according to the dictionary order. For example, in s27.v, the six inputs (ordered) are G0, G1, G2, G3, G5, G6, and G7. Thus, the pattern {0 0 1 1 0 0} corresponds to G0/G1/G2/G3/G5/G6/G7 = 0/0/1/1/0/0. The patterns are indexed (starting from 0) according to the order they are defined.

One fault list file example of is as follows.

XYZ_p1, 2 patterns

{ 000111}

{ 010101}

Note that the definition of a pattern may expand over multiple lines. However, each line contains the definition of at most one pattern.

Fault Simulation Techniques

You can download the book "Essentials of Electronic Testing" from the following link:

http://link.springer.com/book/10.1007/b117406

Several fault simulation techniques are discussed in Chap. 5.

Command Line Parameters

Your executable should be named "fsim". "fsim" takes four command line input parameters: the circuit, the fault list, the test pattern, and the simulation output files.

fsim s27.v faults1 patterns1 result

Output Format

In the output file, you first specify the number of faults by using the keywords DETECTED and UNDETECTED. For example,

DETECTED 20

UNDETECTED 36

Then, you list the undetected faults, one per line.

Evaluation

You should submit your source codes (in your preferred programming language); they will be compiled in Linux environment.

Your program will be evaluated based on (1) correctness, (2) CPU time, and (3) memory usage.