

# Design of 32-Bit Brent Kung Adder

Self Project

Muhammad Shoaib Iqbal  
Mtech (Electronics System)  
IIT-B

Date : 25 july, 2021

## Introduction

Truth table for addition of 3-bits is given in the following table

A	B	$C_{in}$	Sum	$C_{out}$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The equations for Sum and  $C_{out}$  are

$$Sum = A \oplus B \oplus C$$

$$C_{out} = AB + BC + CA$$

- The worst case of ripple carry adder is linear in number of bits to be added
- Carry propagation is the critical path for a multi-bit adder
- To speed up the adder, an architecture is used where logic term are classified as those dependent on carry and those independent of carry bit

The sum and carry can also be written as

$$C_{i+1} = G_i + P_i \cdot C_i, \text{ where}$$

$$G_i = A \cdot B$$

$$P_i = A + B$$

Here computation of  $G_i$  and  $P_i$  are independent of carry, and can be generated as soon as input comes.

## Tree Adder

Tree adders use the idea of carry look ahead addition. Due to tree structure, the delay is the order of  $\log n$  for n-bit adder.

$$C_{i+1} = G_i + P_i \cdot C_i$$

$$C_{i+1} = G_i + P_i \cdot (G_{i-1} + P_{i-1} C_{i-1})$$

Labelling the single bit G and P value as  $G_i^1$  and  $P_i^1$ , the higher order G and P values can be written as

$$G_{i,i-1}^2 = G_i^1 + P_i^1 G_{i-1}^1$$

$$P_{i,i-1}^2 = P_i^1 P_{i-1}^1$$

Hence, we can write carry as

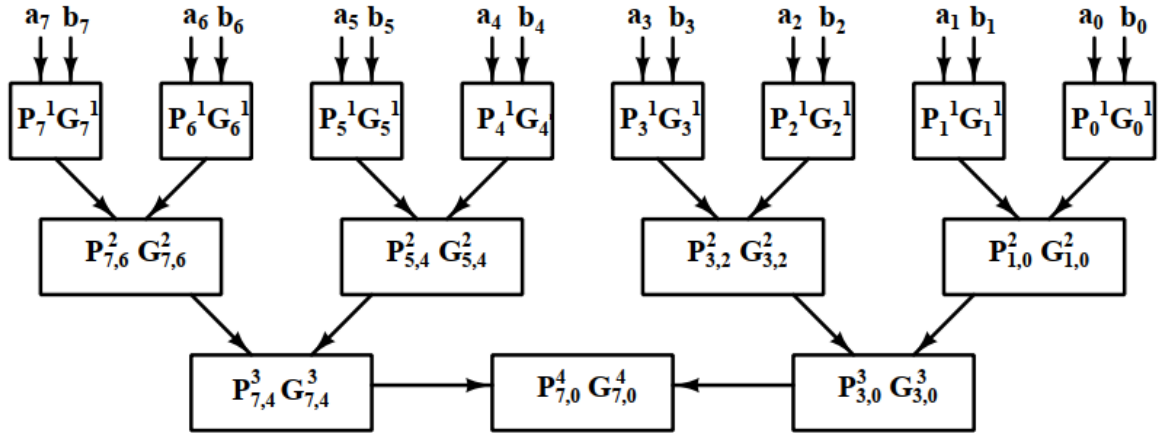
$$C_{i+1} = G_{i,i-1}^2 + P_{i,i-1}^2 C_{i-1}$$

Continuing the same process, we can write  $C_{i+1}$  from  $C_{i-3}$ , as

$$C_{i+1} = G_{i,i-3}^3 + P_{i,i-3}^3 C_{i-3}$$

## Brent Kung Adder

- The brent kung adder is a logarithmic adder of low complexity
- Values of G and P are computed in a tree fashion
- The figure shows the generation of P and G for an 8-bit adder



Once P and G values are generated, carry bits can be calculated as

$$C_1 = G_0^1 + P_0^1 C_0$$

$$C_2 = G_{1,0}^2 + P_{1,0}^2 C_0$$

$$C_4 = G_{3,0}^3 + P_{3,0}^3 C_0$$

$$C_8 = G_{7,0}^4 + P_{7,0}^4 C_0$$

$C_0$  is the input carry and is available at  $t = 0$ . Rest all carry are calculated as

$$C_3 = G_2^1 + P_2^1 C_2$$

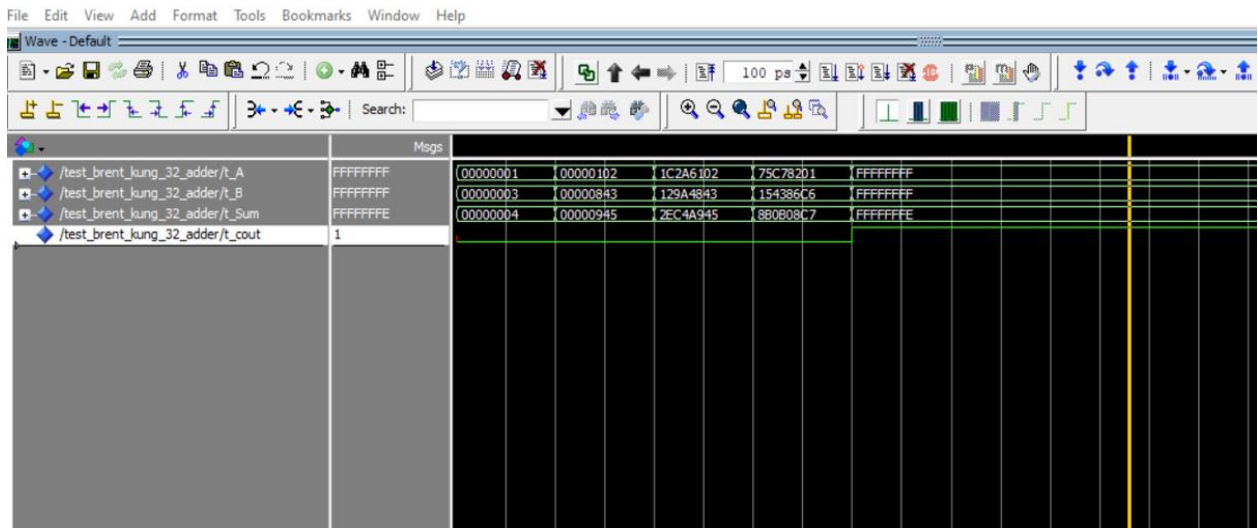
$$C_5 = G_4^1 + P_4^1 C_4$$

$$C_6 = G_{5,4}^2 + P_{5,4}^2 C_4$$

$$C_7 = G_6^1 + P_6^1 C_6$$

## Simulation and Result

A VHDL code is written in Quartus and simulated in ModelSim. Following figure shows the result of two 32-bit numbers in ModelSim.



## Comparison with Ripple Carry Adder using Timing Analysis

Timing analysis for 32-bit Brent Kung and 32-bit Ripple adder is done in Quartus. The result for worst case timing path for both the adders is shown in following figures.

Project Navigator: Files

Files: Brent\_kung\_32\_adder.vhd, gp\_generator.vhd, carry\_calculator.vhd, FA.vhd, RA.vhd

Table of Contents:

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
  - Fitter
  - Assembler
  - Timing Analyzer
    - Summary
    - Parallel Compilation
    - Clocks
    - Slow 1200mV 85C Model
      - Fmax Summary
      - Timing Closure Recommendations
      - Setup Summary
      - Hold Summary
      - Recovery Summary
      - Removal Summary
      - Minimum Pulse Width Summary
      - Worst-Case Timing Paths
      - Setup: 'clk'

Tasks: Compilation

Task: Compile Design

Messages:

```

Type ID Message
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off Brent_kung_32_adder -c Brent_kung_32_adder
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS
204019 Generated file Brent_kung_32_adder.vho in folder "E:/Brent_kung_32_adder/simulation/modelsim/" for EDA simulation tool
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 14 warnings
  
```

System (3) Processing (121)

Creates a new file

### Timing Analysis for Brent Kung Adder

Project Navigator: Files

Files: RA.vhd

Table of Contents:

- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
  - Fitter
  - Assembler
  - Timing Analyzer
    - Summary
    - Parallel Compilation
    - Clocks
    - Slow 1200mV 125C Model
      - Fmax Summary
      - Timing Closure Recommendations
      - Setup Summary
      - Hold Summary
      - Recovery Summary
      - Removal Summary
      - Minimum Pulse Width Summary
      - Worst-Case Timing Paths
      - Setup: 'clk'

Tasks: Compilation

Task: Compile Design

Messages:

```

Type ID Message
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off RA -c RA
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS
204019 Generated file RA.vho in folder "E:/RA/simulation/modelsim/" for EDA simulation tool
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 14 warnings
  
```

System (3) Processing (121)

Creates a new file

### Timing Analysis for Ripple Carry Adder

## Conclusion

The clock-slack for Brent Kung adder is lower than that of ripple carry adder. Hence Brent Kung is faster than ripple carry adder.

## References

*Digital VLSI lectures by Prof. Dinesh Sharma, IIT-bombay*