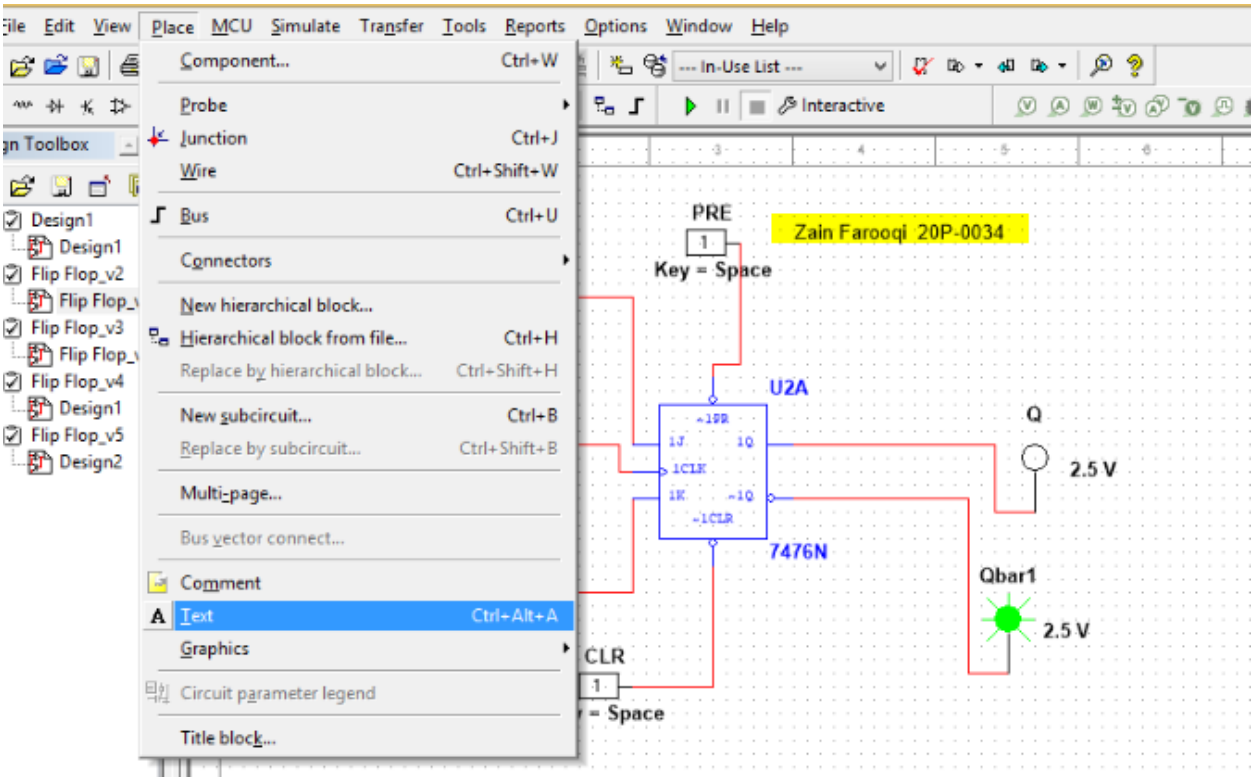
(EL-227) Digital Logic Design Lab

Spring 2021

FAST-NU Peshawar Campus

Assignment # 02

- The due date for this homework is **June 29th, 2021**
- Copied assignments will be awarded zero marks.
- All submissions should be made on Google Class Room.
- Upload only a PDF/MS word file including all tasks.
- Label your inputs and outputs properly on Multisim.
- Use **Multisim** to design circuit diagrams.
- Before doing the task I recommend you all to go through the manuals 14 & 15
- Note: Attach your name and roll no with each screen shot of circuit as shown below.



1. Design a 3 bit Up Counter using JK Flip Flop.
2. Design a 4 bit Up Counter using IC 74LS393D.
3. Construct the Four bit register on Multisim using IC 74LS194 and Check the universal shift register in following modes.
    - Shift Left
    - Shift Right
    - Parallel load data