Bahria University
Discovering Knowledge

Computer Architecture and Logic Design (CALD)

Lecture 16

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Design Process of Synchronous Sequential Circuits

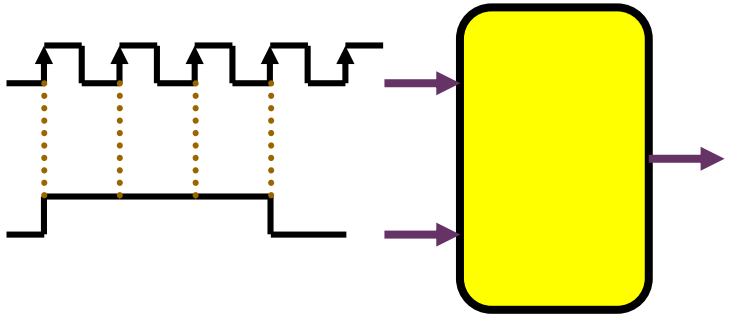
Design Procedure

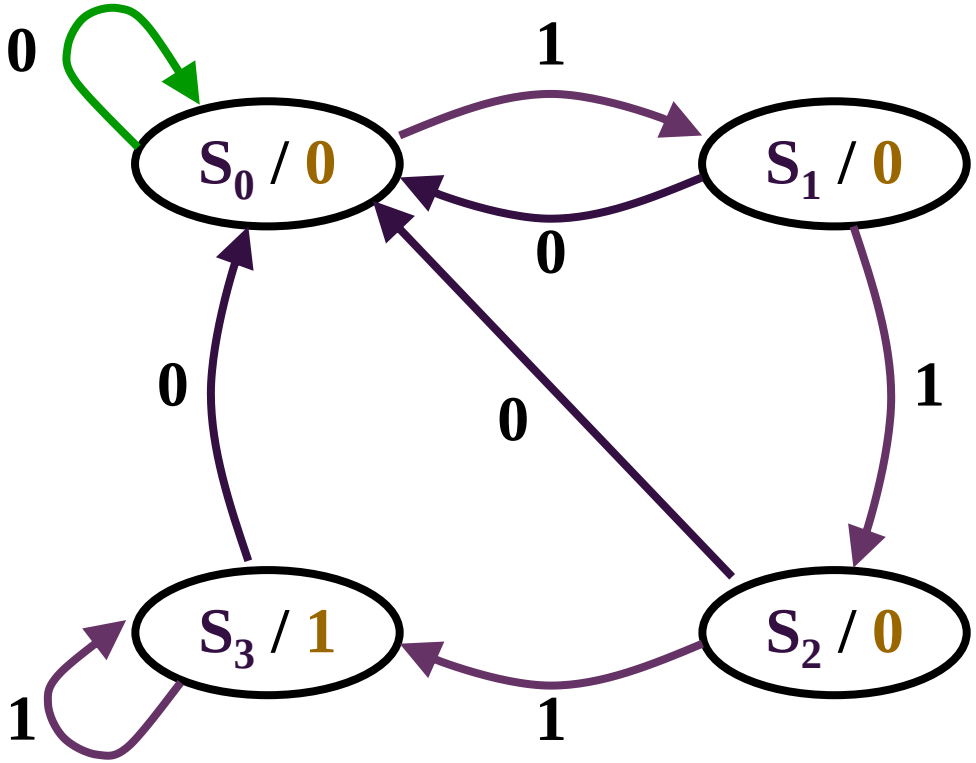
- Design Procedure for sequential circuit
  - The word description of the circuit behavior to get a state diagram;
  - State reduction if necessary;
  - Assign binary values to the states;
  - Obtain the binary-coded state table;
  - Choose the type of flip-flops;
  - Derive the simplified flip-flop input equations and output equations;
  - Draw the logic diagram;

Design of Clocked Sequential Circuits

- *Example*:

Detect 3 or more consecutive 1's



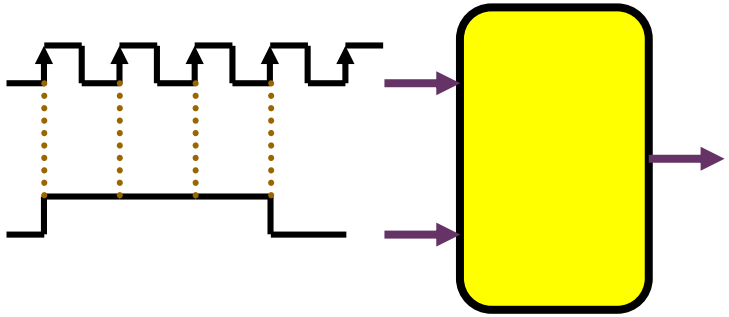


State	*A* *B*
S_0	0 0
S_1	0 1
S_2	1 0
S_3	1 1

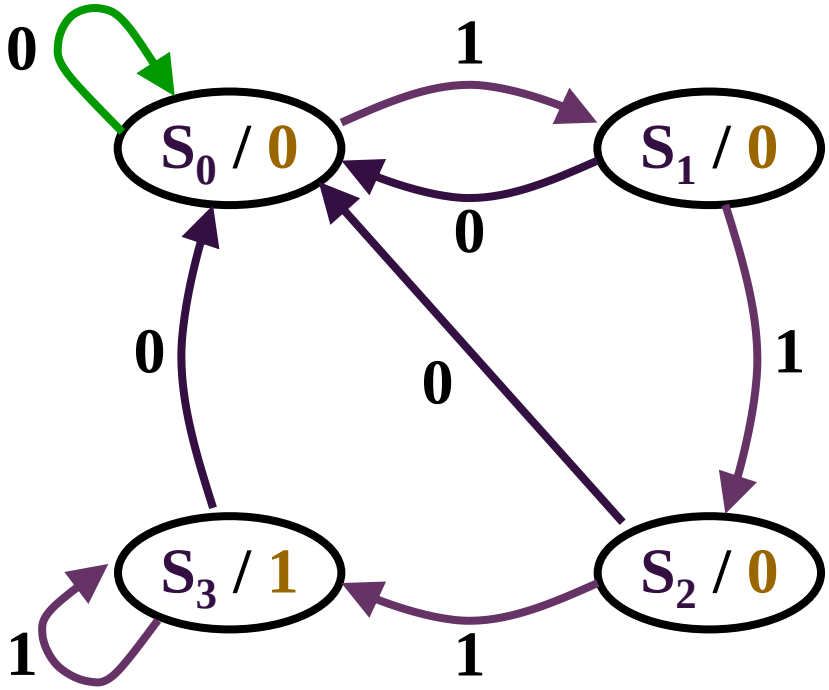
Design of Clocked Sequential Circuits

- *Example*:

Detect 3 or more consecutive 1's



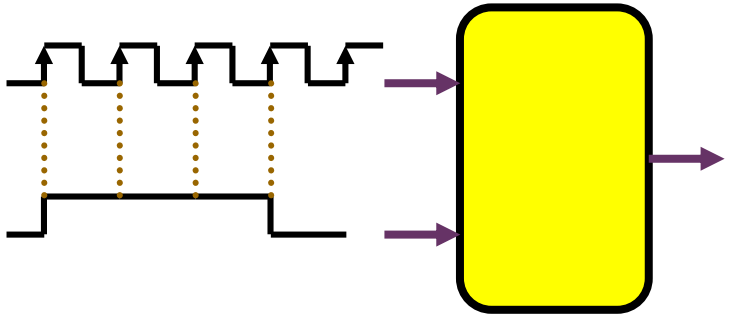
Present State		Input	Next State		Output
A	*B*	*x*	*A*	*B*	*y*
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1



Design of Clocked Sequential Circuits

- *Example*:

Detect 3 or more consecutive 1's



Present State		Input	Next State		Output
A	*B*	*x*	*A*	*B*	*y*
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

Synthesis using *D* Flip-Flops

$$A(t+1) = D_A(A, B, x)$$

$$= \sum(3, 5, 7)$$

$$B(t+1) = D_B(A, B, x)$$

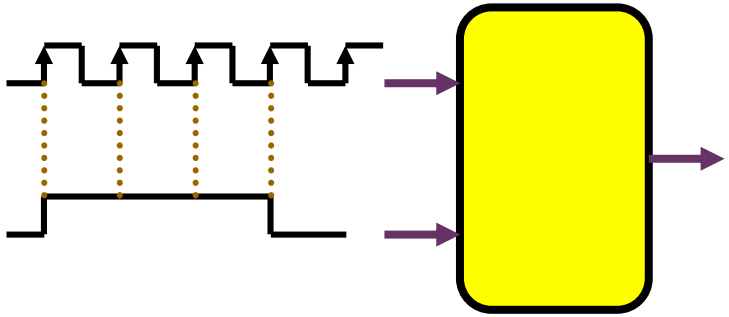
$$= \sum(1, 5, 7)$$

$$y(A, B, x) = \sum(6, 7)$$

Design of Clocked Sequential Circuits with *D* F.F.

- *Example*:

Detect 3 or more consecutive 1's



Synthesis using *D* Flip-Flops

$$D_A(A, B, x) = \sum(3, 5, 7)$$

$$= A\,x + B\,x$$

A \ Bx	00	01	11	10
0	0	1	1	0

$$D_B(A, B, x) = \sum(1, 5, 7)$$

$$= A\,x + B'x$$

A \ Bx	00	01	11	10
0	0	1	1	0

$$y(A, B, x) = \sum(6, 7)$$

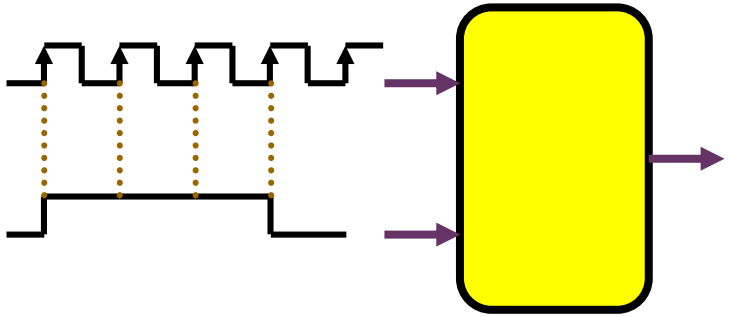
$$= A\,B$$

A \ Bx	00	01	11	10
0	0	0	0	0
1	0	0	1	1

Design of Clocked Sequential Circuits with *D* F.F.

- *Example*:

Detect 3 or more consecutive 1's

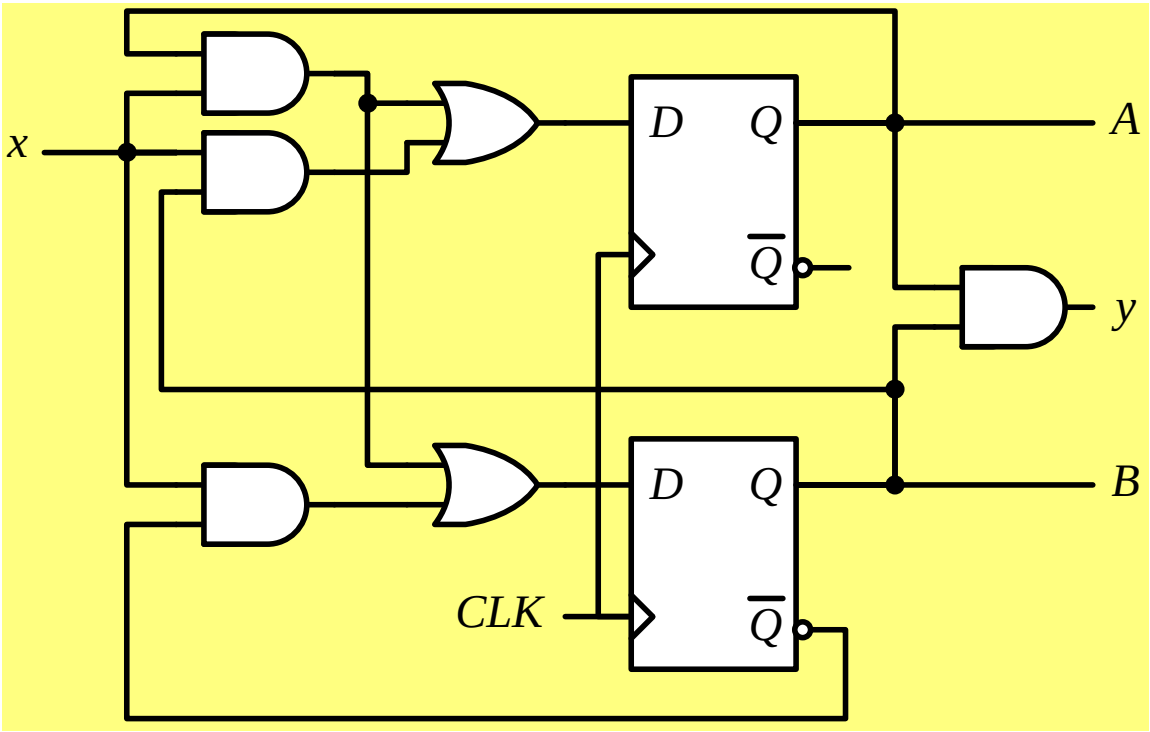


Synthesis using *D* Flip-Flops

$$D_A = A\,x + B\,x$$

$$D_B = A\,x + B'\,x$$

$$y = A\,B$$



Flip-Flop Excitation Tables

Present State	Next State	F.F. Input
$Q(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

Present State	Next State	F.F. Input	
$Q(t)$	$Q(t+1)$	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

0 0 (No change)
0 1 (Reset)

1 0 (Set)
1 1 (Toggle)

0 1 (Reset)
1 1 (Toggle)

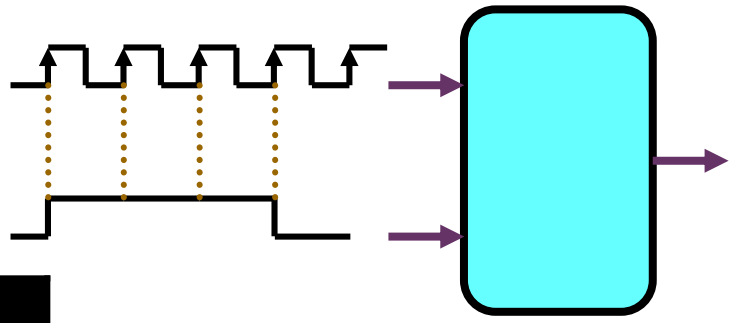
0 0 (No change)
1 0 (Set)

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

Design of Clocked Sequential Circuits with *JK* F.F.

- *Example*:

Detect 3 or more consecutive 1's



Present State		Input	Next State		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	x	0	x
0	0	1	0	1	0	x	1	x
0	1	0	0	0	0	x	x	1
0	1	1	1	0	1	x	x	1
1	0	0	0	0	x	1	0	x
1	0	1	1	1	x	0	1	x
1	1	0	0	0	x	1	x	1
1	1	1	1	1	x	0	x	0

Synthesis using *JK* F.F.

$J_A(A, B, x) = \sum(3)$

$d_{JA}(A, B, x) = \sum(4,5,6,7)$

$K_A(A, B, x) = \sum(4, 6)$

$d_{KA}(A, B, x) = \sum(0,1,2,3)$

$J_B(A, B, x) = \sum(1, 5)$

$d_{JB}(A, B, x) = \sum(2,3,6,7)$

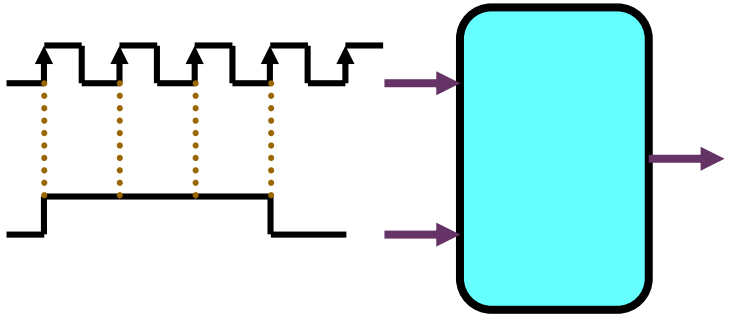
$K_B(A, B, x) = \sum(2, 3, 6)$

$d_{KB}(A, B, x) = \sum(0,1,4,5)$

Design of Clocked Sequential Circuits with *JK* F.F.

- *Example*:

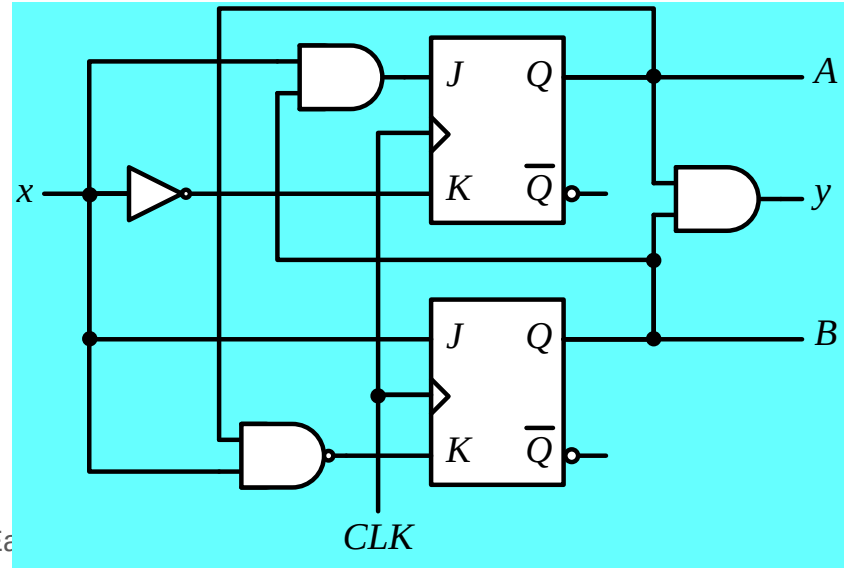
Detect 3 or more consecutive 1's

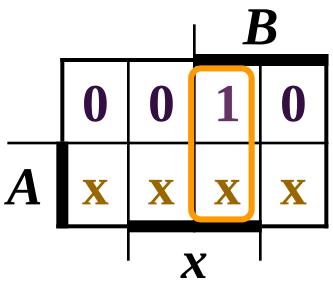


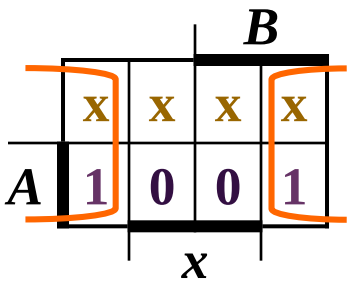
Synthesis using *JK* Flip-Flops

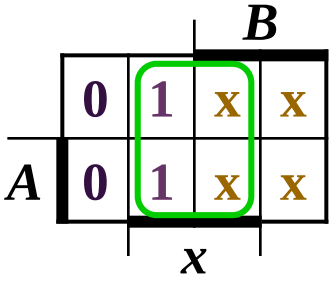
$J_A = B\,x \qquad K_A = x'$

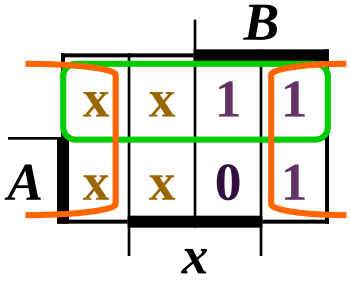
$J_B = x \qquad K_B = A' + x'$









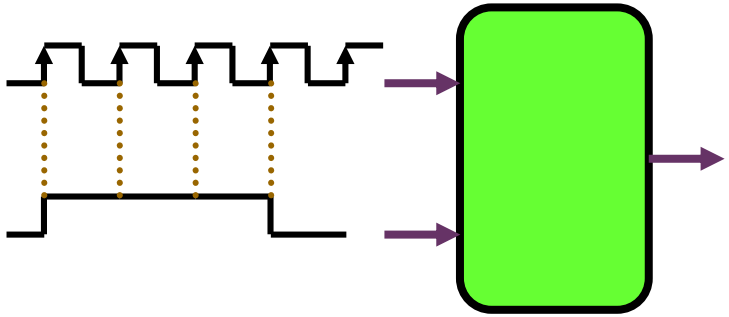


Design of Clocked Sequential Circuits with *T* F.F.

- *Example*:

Detect 3 or more consecutive 1's

Present State		Input	Next State		F.F. Input	
A	*B*	*x*	*A*	*B*	T_A	T_B
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	0	0	0	1
0	1	1	1	0	1	1
1	0	0	0	0	1	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	1	1	1	0	0



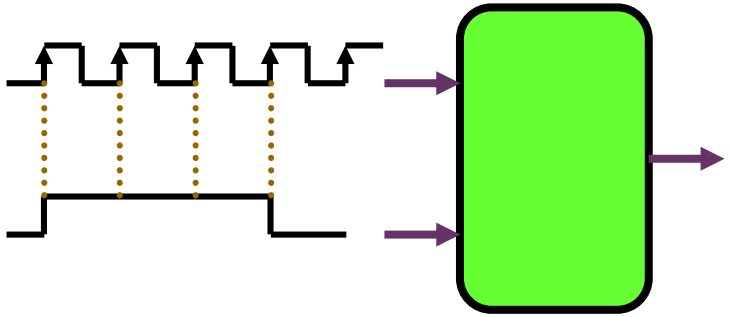
Synthesis using *T* Flip-Flops

$$T_A(A, B, x) = \sum(3, 4, 6)$$
$$T_B(A, B, x) = \sum(1, 2, 3, 5, 6)$$

Design of Clocked Sequential Circuits with *T* F.F.

- *Example*:

Detect 3 or more consecutive 1's



Synthesis using *T* Flip-Flops

$$T_A = A\,x' + A'\,B\,x$$

$$T_B = A'\,B + B \oplus x$$