Bahria University
Discovering Knowledge

Computer Architecture and Logic Design (CALD)

Lecture 13

Dr. Sorath Hansrajani

Assistant Professor

Department of Software Engineering

Bahria University Karachi Campus

Email: sorathhansrajani.bukc@bahria.edu.pk

Sequential Logic

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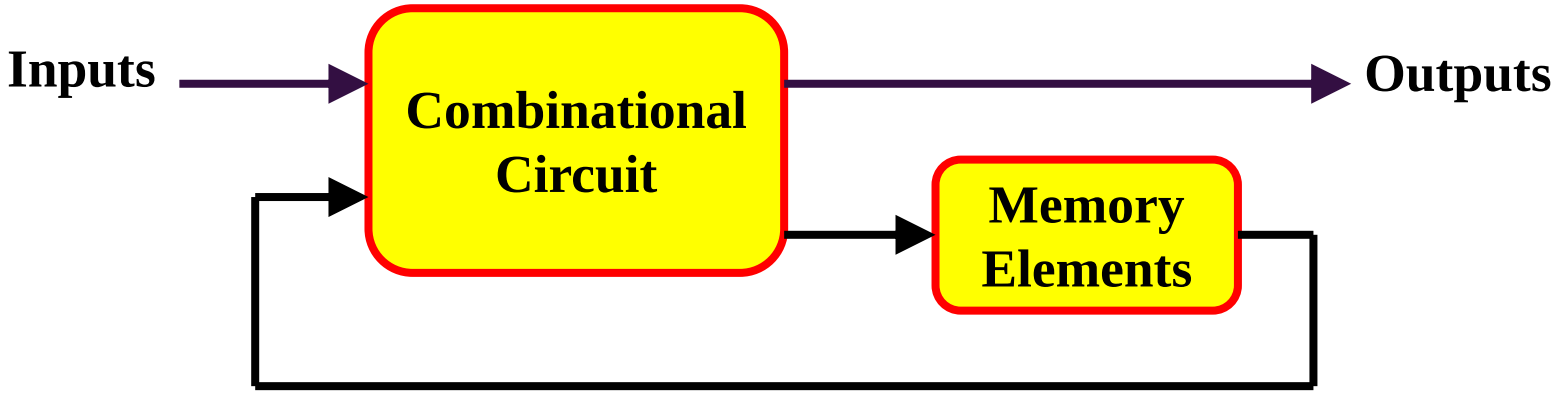
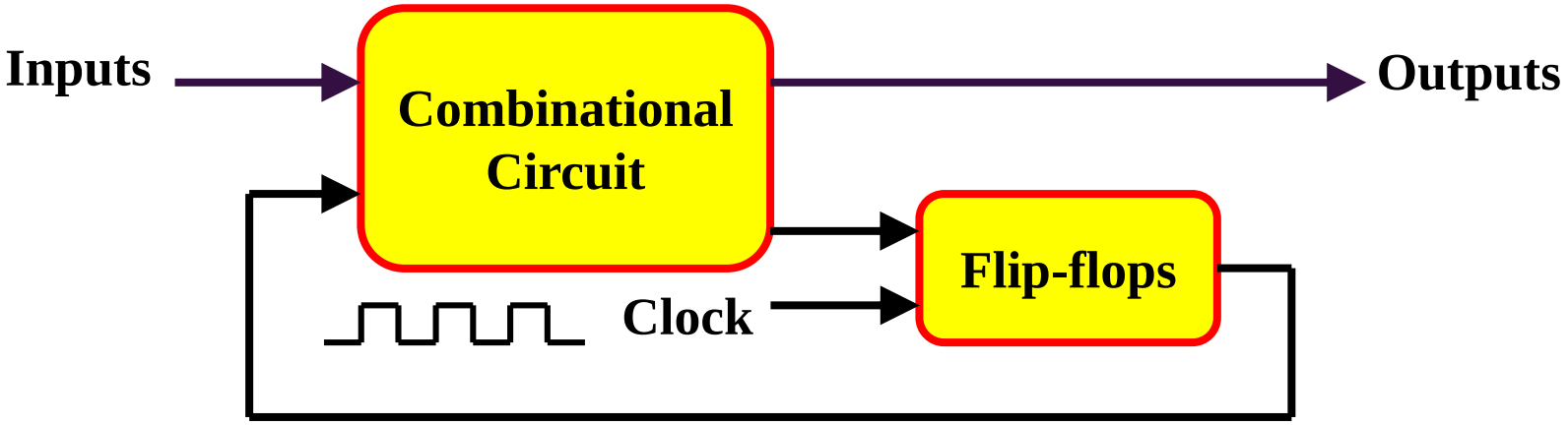
Sequential Circuits

- Asynchronous



- Synchronous



Flip-Flops

- The memory elements used in clocked sequential circuits are called flip-flops.
- These circuits are binary cells capable of storing one bit of information.
- A flip-flop circuit has two outputs; one for the normal value and one for the complement value of the bit stored in it.
- Binary information can enter a flip-flop in a variety of ways.
- A flip-flop circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit) until directed by an input signal to switch states.

Flip-Flops

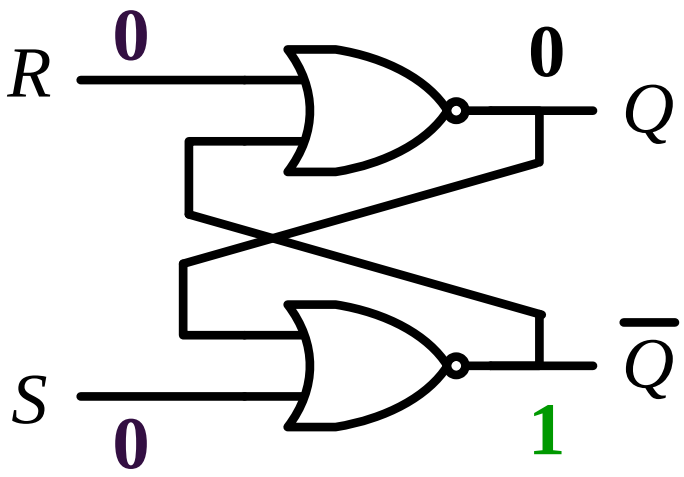
- There are mainly four types of flip-flops:
- SR (Set-Reset) Flip-Flop
- D (Data) Flip-Flop
- T (Toggle) Flip-Flop
- JK Flip-Flop

Latch

- A latch is an electronic device that changes its output immediately on the basis of the applied input.
- One can use it to store either 0 or 1 at a specified time.
- A latch contains two inputs- SET and RESET, and it also has two outputs. They complement each other.
- One can use a latch for storing one bit of data.
- It is a memory device- just like the flip-flop.
- But it is not synchronous, and it does not work on the edges of the clock like the flip-flop.

Latches

- *SR* Latch



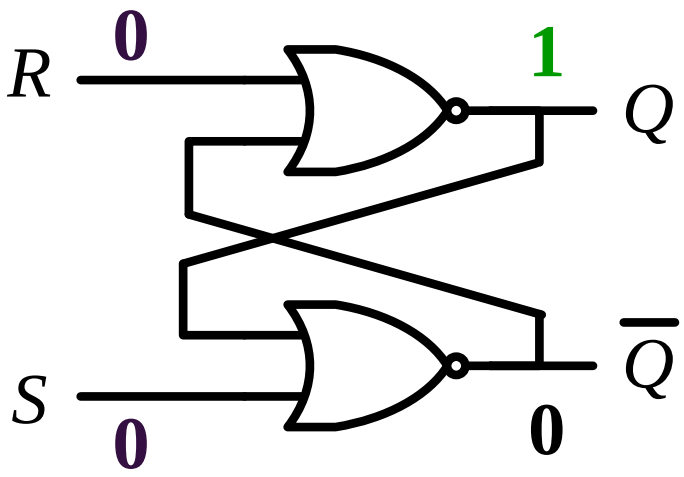
S	R	Q_0	Q	Q'
0	0	0	0	1

$Q = Q_0$

Initial Value

Latches

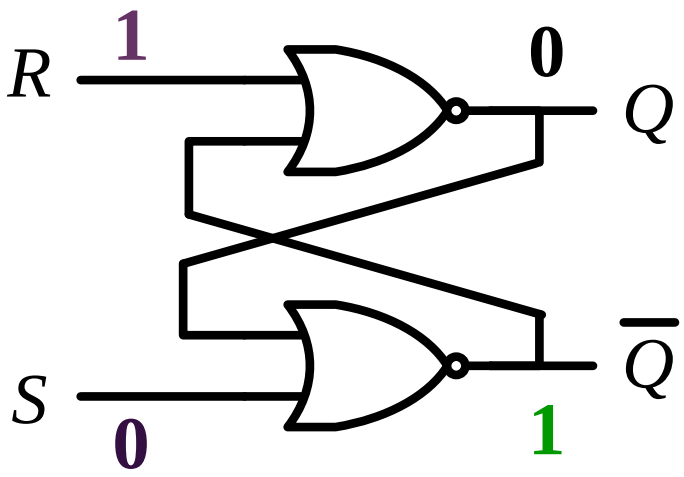
- *SR* Latch



S	R	Q_0	Q	Q'	
0	0	0	0	1	$Q = Q_0$
0	0	1	1	0	$Q = Q_0$

Latches

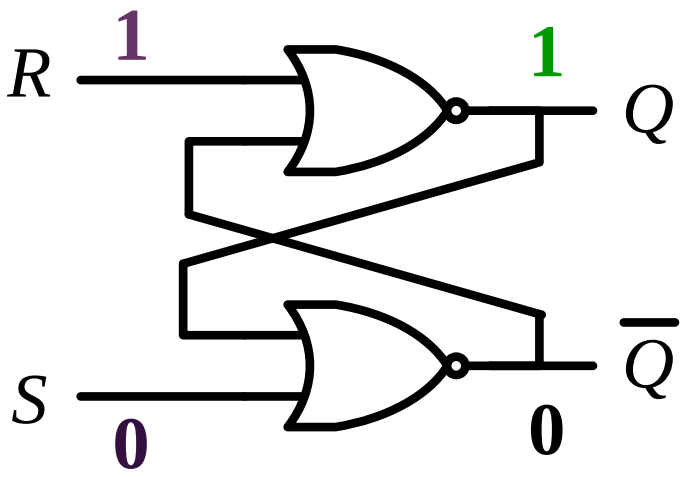
- *SR* Latch



S	R	Q_0	Q	Q'	
0	0	0	0	1	$Q = Q_0$
0	0	1	1	0	
0	1	0	0	1	$Q = 0$

Latches

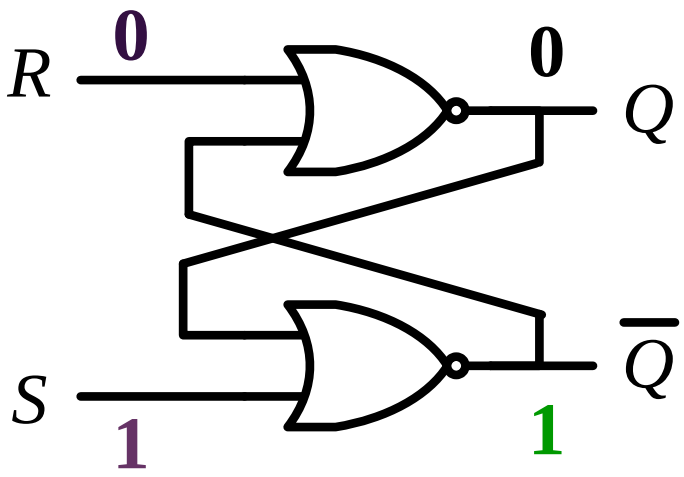
- *SR* Latch



S	R	Q_0	Q	Q'	
0	0	0	0	1	$Q = Q_0$
0	0	1	1	0	
0	1	0	0	1	$Q = 0$
0	1	1	0	1	$Q = 0$

Latches

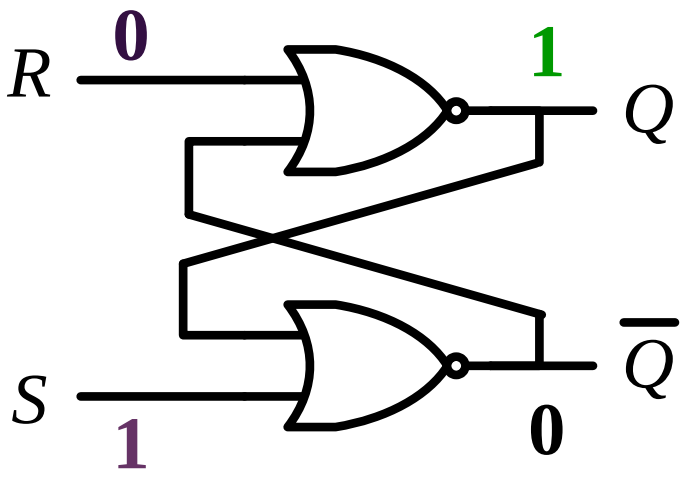
- *SR* Latch



S	R	Q_0	Q	Q'	
0	0	0	0	1	$Q = Q_0$
0	0	1	1	0	
0	1	0	0	1	$Q = 0$
0	1	1	0	1	
1	0	0	1	0	$Q = 1$

Latches

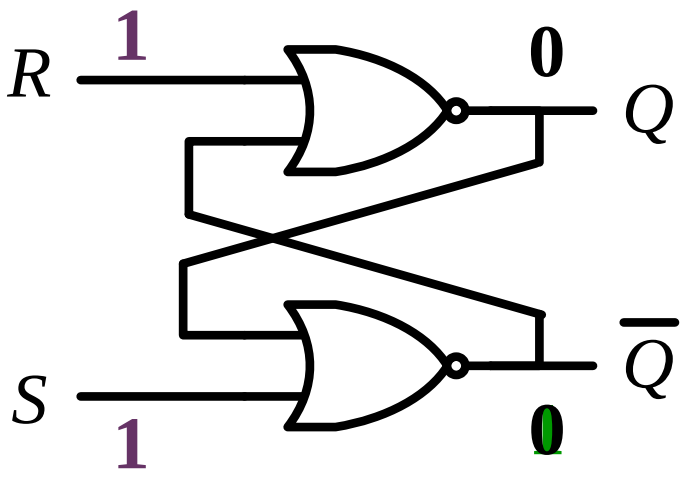
- *SR* Latch



S	R	Q_0	Q	Q'	
0	0	0	0	1	$Q = Q_0$
0	0	1	1	0	
0	1	0	0	1	$Q = 0$
0	1	1	0	1	
1	0	0	1	0	$Q = 1$
1	0	1	1	0	$Q = 1$

Latches

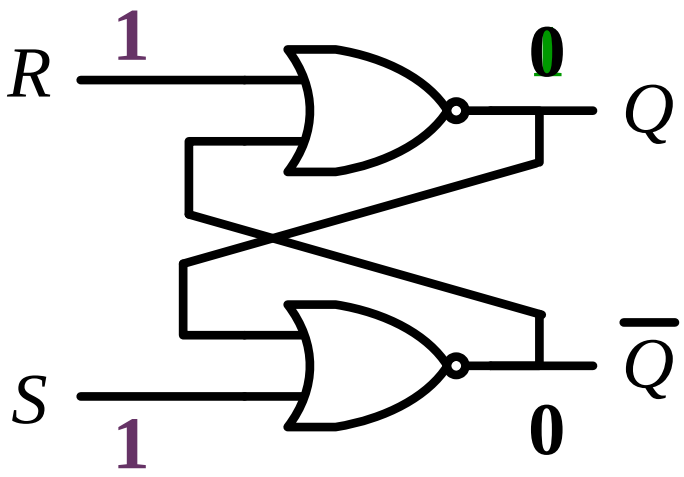
- *SR* Latch



S	R	Q_0	Q	Q'	
0	0	0	0	1	$Q = Q_0$
0	0	1	1	0	
0	1	0	0	1	$Q = 0$
0	1	1	0	1	
1	0	0	1	0	$Q = 1$
1	0	1	1	0	
1	1	0	0	0	$Q = Q'$

Latches

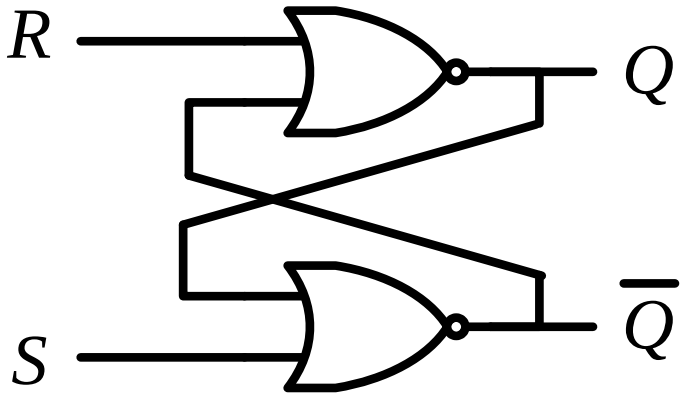
- *SR* Latch



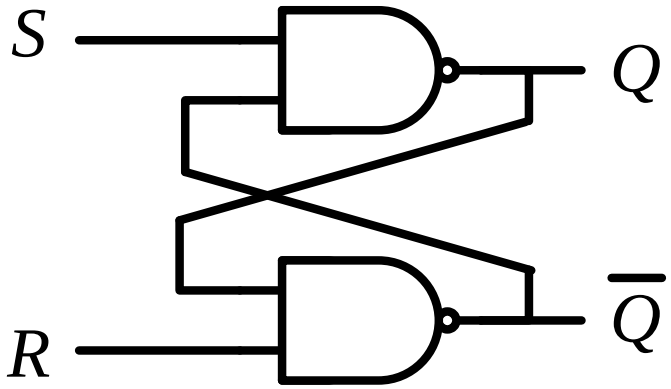
S	R	Q_0	Q	Q'	
0	0	0	0	1	$Q = Q_0$
0	0	1	1	0	
0	1	0	0	1	$Q = 0$
0	1	1	0	1	
1	0	0	1	0	$Q = 1$
1	0	1	1	0	
1	1	0	0	0	$Q = Q'$
1	1	1	0	0	$Q = Q'$

Latches

- *SR* Latch



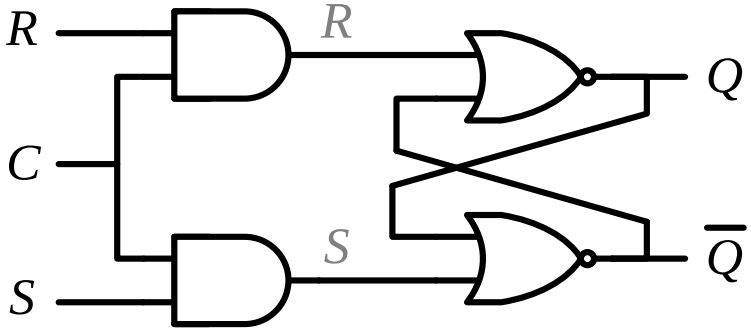
S	R	Q	
0	0	Q_0	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q=Q'=0$	Invalid

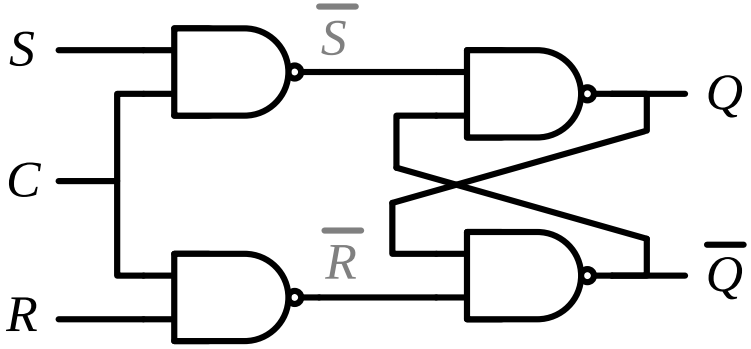


S	R	Q	
0	0	$Q=Q'=1$	Invalid
0	1	1	Set
1	0	0	Reset
1	1	Q_0	No change

Controlled Latches

- *SR* Latch with Control Input

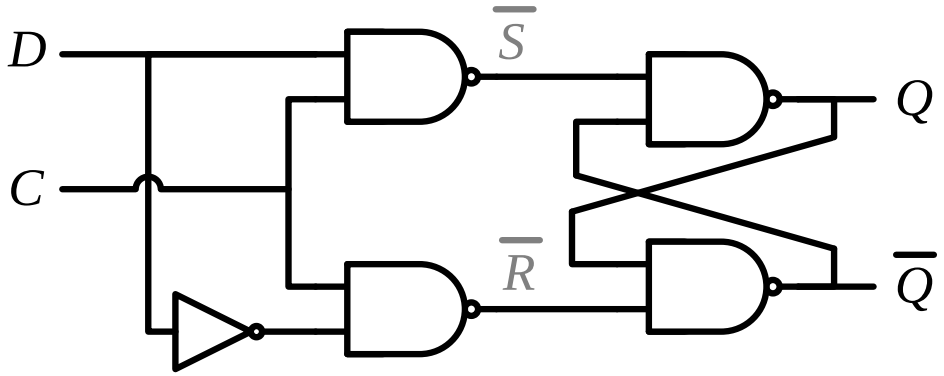




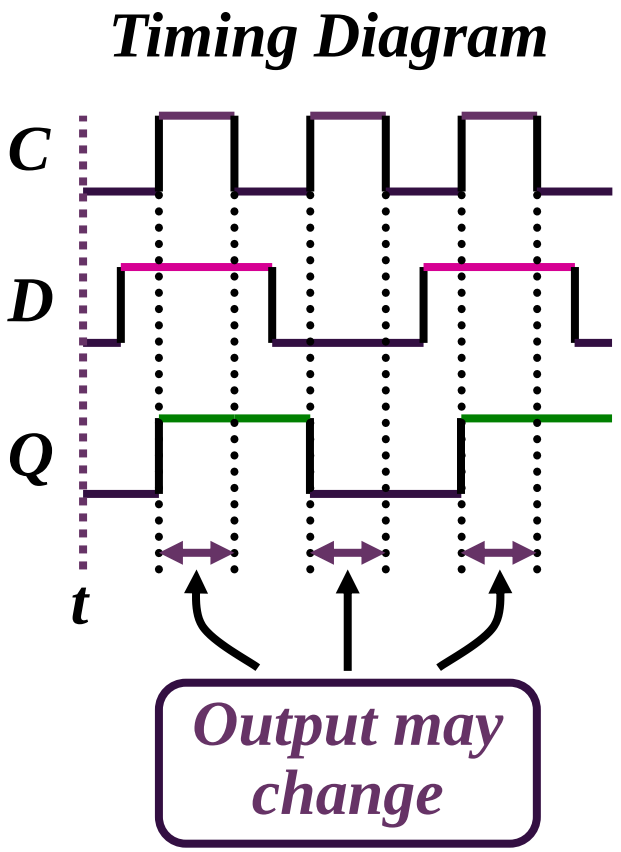
C S R	Q	
0 x x	Q_0	No change
1 0 0	Q_0	No change
1 0 1	0	Reset
1 1 0	1	Set
1 1 1	$Q=Q'$	Invalid

Controlled Latches

- *D* Latch (*D* = *Data*)

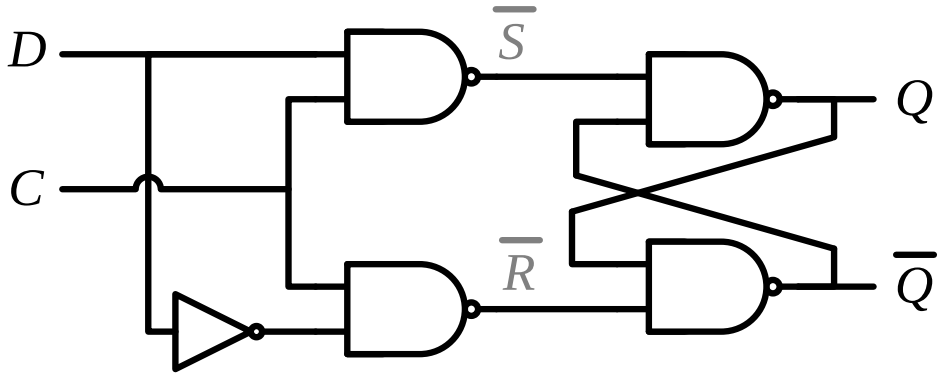


C D	Q	
0 x	Q_0	No change
1 0	0	Reset
1 1	1	Set

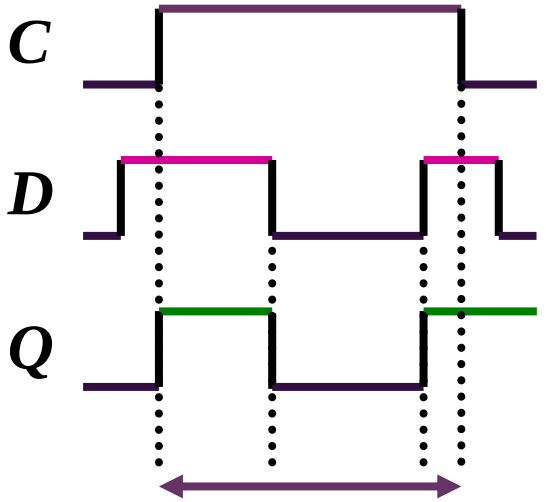


Controlled Latches

- *D* Latch (*D* = *Data*)



Timing Diagram

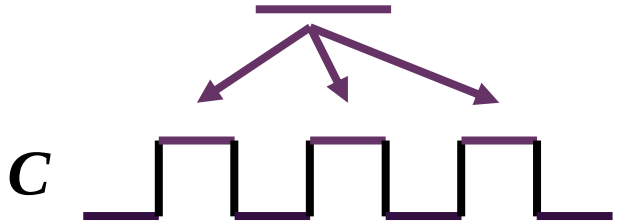


C D	Q	
0 x	Q_0	No change
1 0	0	Reset
1 1	1	Set

Output may change

Flip-Flops

- Controlled latches are level-triggered



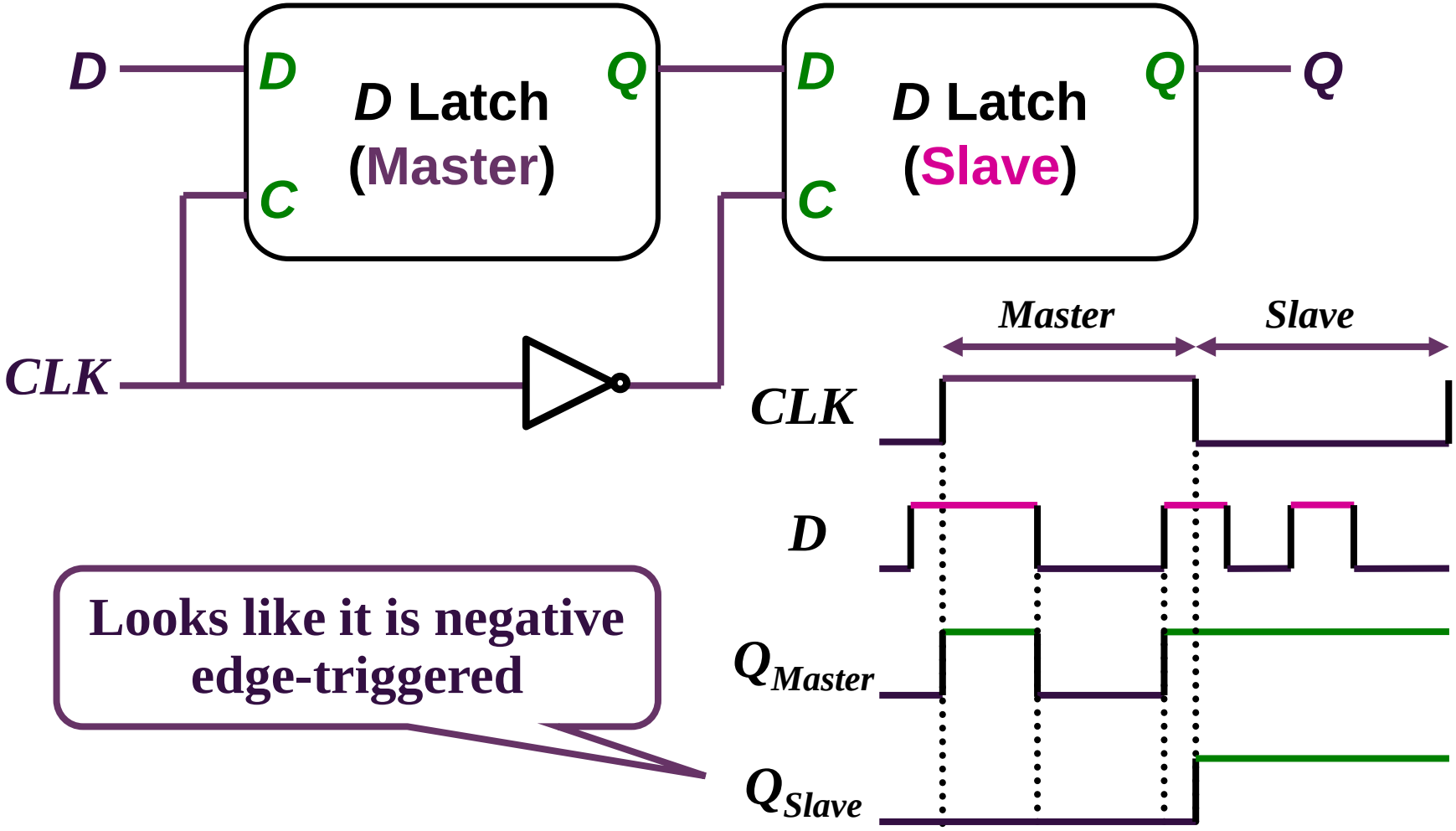
- Flip-Flops are edge-triggered

Positive Edge

Negative Edge

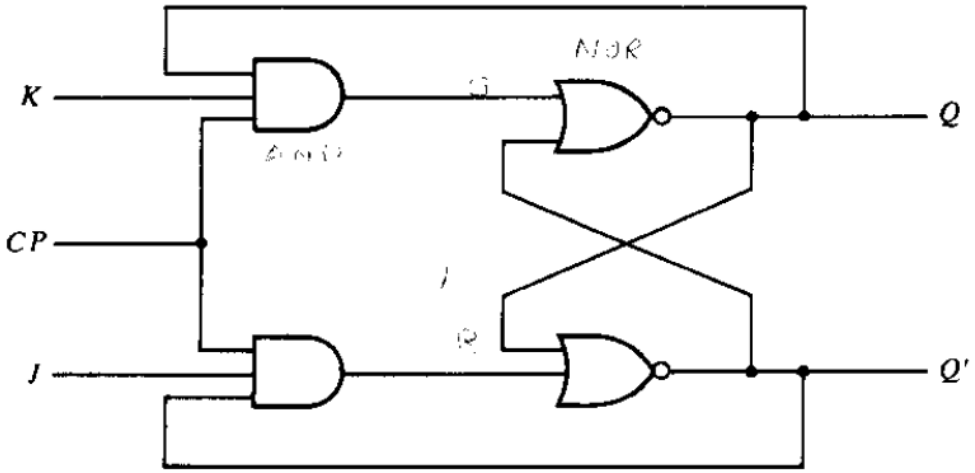
Flip-Flops

- Master-Slave *D* Flip-Flop

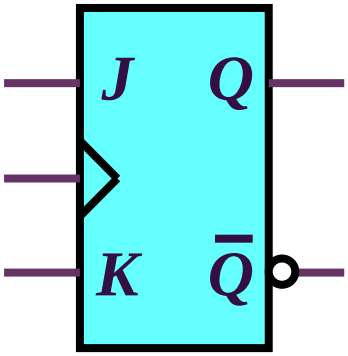


Flip-Flops

- *JK* Flip-Flop

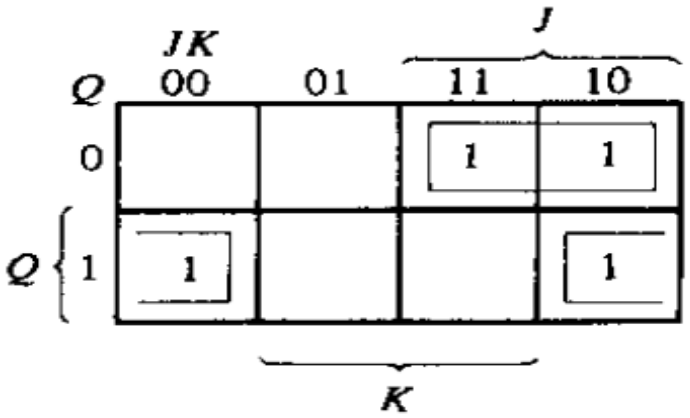


(a) Logic diagram



Q	J	K	$Q(t+1)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(b) Characteristic table

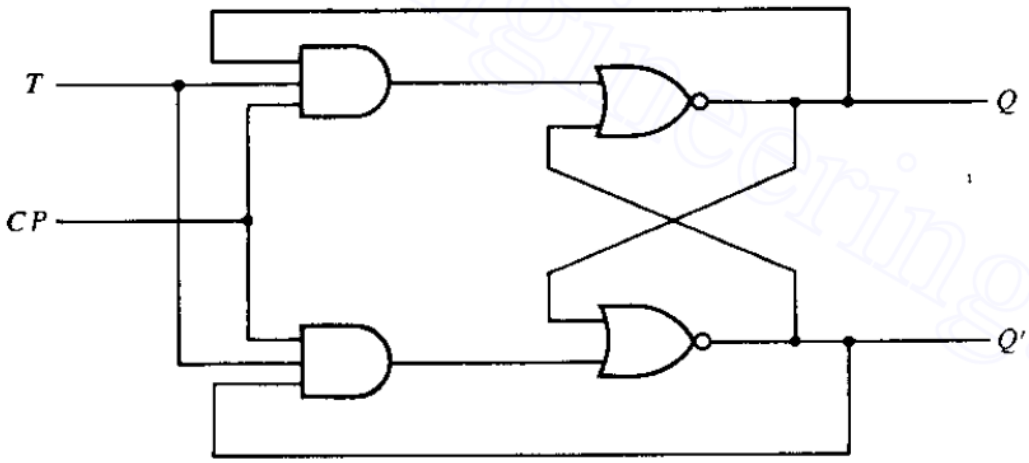


$$Q(t+1) = JQ' + K'Q$$

(c) Characteristic equation

Flip-Flops

- *T* Flip-Flop



(a) Logic diagram

Q	T	Q(t + 1)
0	0	0
0	1	1
1	0	1
1	1	0

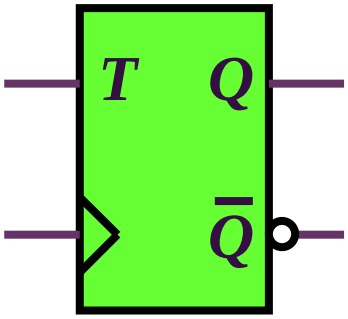
(b) Characteristic table

Q \ T	0	1
0		1
1	1	

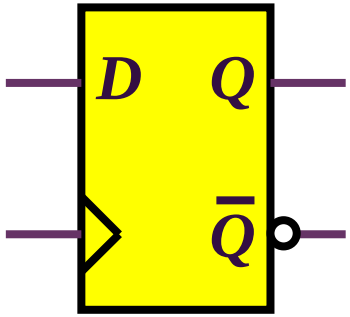
$Q(t+1) = TQ' + T'Q$

(c) Characteristic equation

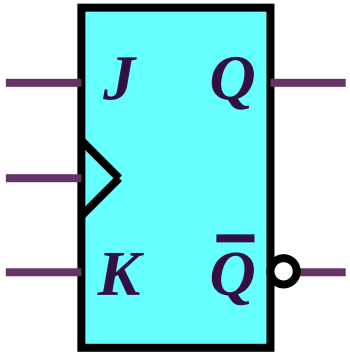
FIGURE 6-7
T flip-flop



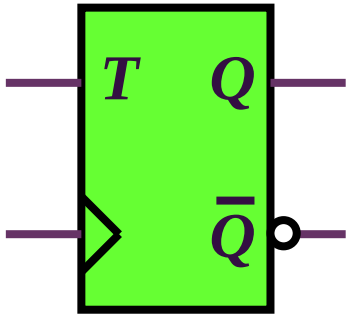
Flip-Flop Characteristic Tables



D	Q(t+1)	
0	0	Reset
1	1	Set

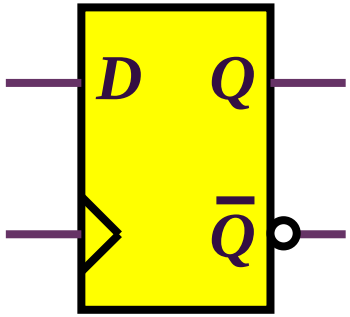


J	K	Q(t+1)	
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Toggle



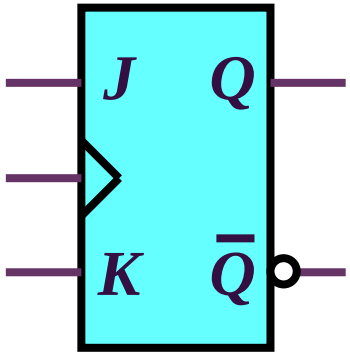
T	Q(t+1)	
0	Q(t)	No change
1	Q'(t)	Toggle

Flip-Flop Characteristic Equations



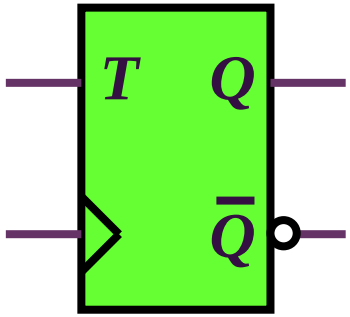
D	Q(t+1)
0	0
1	1

$Q(t+1) = D$



J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

$Q(t+1) = JQ' + K'Q$

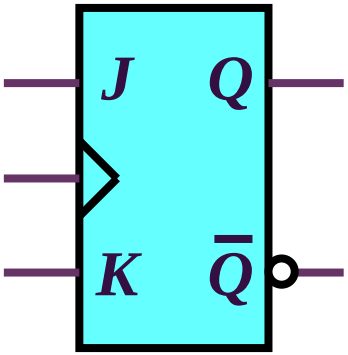


T	Q(t+1)
0	Q(t)
1	Q'(t)

$Q(t+1) = T \oplus Q$

Flip-Flop Characteristic Equations

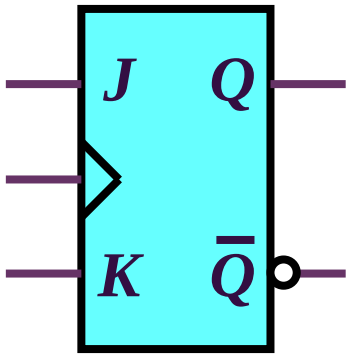
- Analysis / Derivation



J	K	$Q(t)$	$Q(t+1)$	
0	0	0	0	No change
0	0	1	1	
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Flip-Flop Characteristic Equations

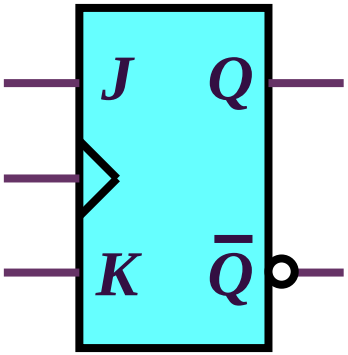
- Analysis / Derivation



J	K	$Q(t)$	$Q(t+1)$	
0	0	0	0	No change
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Flip-Flop Characteristic Equations

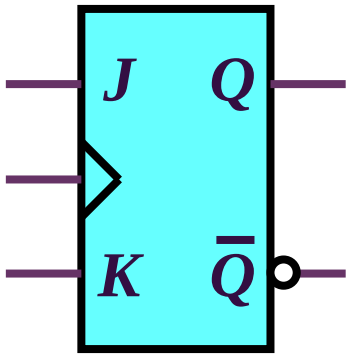
- Analysis / Derivation



J	K	$Q(t)$	$Q(t+1)$	
0	0	0	0	No change
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0		
1	1	1		

Flip-Flop Characteristic Equations

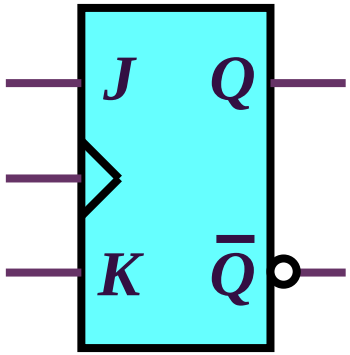
- Analysis / Derivation



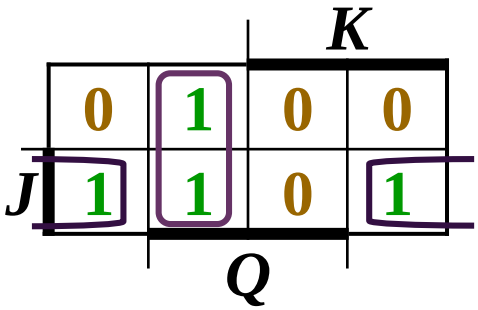
J	K	Q(t)	Q(t+1)	
0	0	0	0	No change
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	1	Toggle
1	1	1	0	

Flip-Flop Characteristic Equations

- Analysis / Derivation



J	K	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



$$Q(t+1) = JQ' + K'Q$$