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A no: 1.3

(a)

32 bit instruction ; 16 bits opcode ; 16 bit address
+ 32 bit instruction ; 16 bits opcode ; 16 bit address
64 bit instruction ; 32 bits opcode (4 Bytes) ; 32 bit address

2^{32} - 4294967296 bytes or 4GB memory can be directly addressed.

(b)

The ideal size of microprocessor address buses should be 64 bits.

* 64 bit data bus:
If data bus is 64 bits then it would take a single access to the memory.

* 32 bit data bus:
64 bit local address bus & a 32-bit local data bus. Instruction and data transfers would take three bus cycles each, one for the address and two for the data. Since if address bus is 64 bits, the whole address can be

transferred to memory at once and decoded there; however, since the data bus is only 32 bits, it will require 2 bit cycles (accesses to memory) to fetch the 64-bit instruction or operand.

* 16 bit data bus.

64-bit local address bus and a 16 bit local data bus. Instruction and data transfers would take five bus cycles each, one for the address and four for the data. Therefore, the data bus is 16 bits, the microprocessor will need 4 bus cycles to fetch the 64-bit instruction or operand.

(c)

32 bits instruction register needs if IR is only contain the opcode.
64-bits instructions register needs to contain the whole instruction.

A no 1.4

(a)

The maximum memory address space = 2^{16} = 64 Kbytes

(b)

The maximum memory address space = 2^{16} = 64 Kbytes
Therefore in (a) & (b), the microprocessor is to access 64K bytes, but the difference thing between them is that the access of

8 bit memory will transfer a 8-bits and the access of 16-bit memory may transfer 8-bits or 16-bits word.

(c)

Separate I/O instructions are needed because during its execution will generate separate it own signals I/O signals. That signals will be different from the memory signals which is generated during the execution for memory instructions. Therefore, one more output pin will be needed to carry I/O signals.

(d)

With an 8-bit I/O port number, the micro-processor can support $2^8 = 256$ 8 bit input ports and $2^8 = 256$ 8-bit output ports. With an 8-bit I/O port number, the micro-processor can support $2^8 = 256$ ~~16-bit input port and 2~~ or Input port a $2^8 = 256$ 16-bit output ports. Thus, the size of the I/O port will not change the number of I/O ports since the number of I/O ports depends on the number of bits which is used to represent the I/O port number (equals to 8-bits in both cases).

Q no. 1.5

The microprocessor has a 32-bit external data-bus, this means that 32 bits are transferred in 1 bus cycle.

Input clock = 16 MHz

$$\text{clock cycle} = \frac{1}{16\text{MHz}} = \frac{1}{16\times10^{6}} = 62.5\times10^{-9}\text{s}$$

Therefore, 1 cycle takes 62.5 ns

Since 1 bus cycle = 4 clock cycles =

$4 \times 62.5 = 250\text{ns}$

Since 4 bytes are transferred (32-bit data) for every 250ns.

$$\text{Thus Transfer Rate} = \frac{4}{250\text{ns}} = \frac{4}{250\times10^{-9}} = 16\times10^{6}\ \text{bytes/sec}$$

Transfer Rate = 16 MB/s

To increase its performance.

By doubling the frequency, it may mean adopting a new chip manufacturing technology (assuming each instruction will have the same number of clock cycles).

By doubling the external data bus, that means wider (may be never) on-chip data bus drivers / latches and modifications to the bus control logic.

Therefore, in the first situation the speed of the memory chips will need to double, not to show down the micro-processor. Regarding the second situation, the word length of the memory will must double to able to send/receive 64-bit quantities.

Ex: 1.6

(a)

Input from the Teletype is stored in INPR. The INPR will only accept data from the Teletype when FGI = 0, when data arrives, it is stored in INRR, and FGI is set to 1. The CPU periodically checks FGI. If FGI=1, the CPU transfers the contents of INPR to the AC and sets FGI to 0.

When CPU has data to send the Teletype, it checks FGO. If FGO=0, the CPU must wait. If FGO=1, the CPU transfers the contents of the AC to OUTR and sets FGI to 1 after the word is printed.

(b)

The process described in (a) is very wasteful. The CPU, which is ~~most~~ much faster than Teletype, must repeatedly check FGI and FGO. If interrupts are used, Teletype can issue an interrupt to the CPU whenever it is ready to accept or send data. The IEN register can be set by the CPU (under programmer Control)