BAHRIA UNIVERSITY (KARACHI CAMPUS)

ASSIGNMENT I – Fall 2021

COMPUTER ARCHITECTURE & LOGIC DESIGN

Class: **BSE[4]- 2(A)/(B)**

Course Instructor: **Dr. Syed Samar Yazdani**

Due Date: _____

Date: 17.11.2021

Max Marks: **10 Marks**

Student's Name: _____

Reg. No: _____

Note:

- *Attempt all questions*

Question 1 [CLO 3]

A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45,000	1
Data transfer	32,000	2
Floating point	15,000	2
Control transfer	8000	2

Determine the effective *CPI*, and execution time for this program.

Question 2 [CLO 3]

Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs:

Instruction Type	Instruction Count (millions)	Cycles per Instruction
Machine A		
Arithmetic and logic	8	1
Load and store	4	3
Branch	2	4
Others	4	3
Machine A		
Arithmetic and logic	10	1
Load and store	8	2
Branch	2	4
Others	4	3

a. Determine the effective *CPI*, MIPS rate, and execution time for each machine.
b. Comment on the results.

Question 3 [CLO 3]

The hypothetical machine of Figure 3.4 also has two I/O instructions:

0011 = Load AC from I/O
0111 = Store AC to I/O

In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 3.5) for the following program:

1. Load AC from device 5.
2. Add contents of memory location 940.
3. Store AC to device 6.

Assume that the next value retrieved from device 5 is 3 and that location 940 contains a value of 2.

Question 4 [CLO 3]

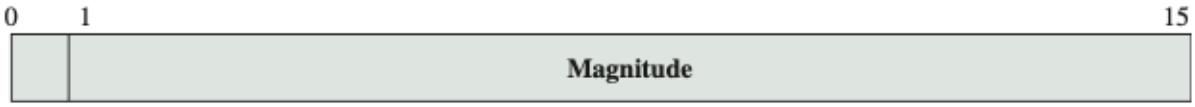
The program execution of Figure 3.5 is described in the text using six steps. Expand this description to show the use of the MAR and MBR.

Question 5 [CLO 3]

Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.

a. What is the maximum directly addressable memory capacity (in bytes)?
b. Discuss the impact on the system speed if the microprocessor bus has:
1. 32-bit local address bus and a 16-bit local data bus, or
2. 16-bit local address bus and a 16-bit local data bus.
c. How many bits are needed for the program counter and the instruction register?

(a) Instruction format



(b) Integer format

Program counter (PC) = Address of instruction
Instruction register (IR) = Instruction being executed
Accumulator (AC) = Temporary storage

(c) Internal CPU registers

0001 = Load AC from memory
0010 = Store AC to memory
0101 = Add to AC from memory

(d) Partial list of opcodes

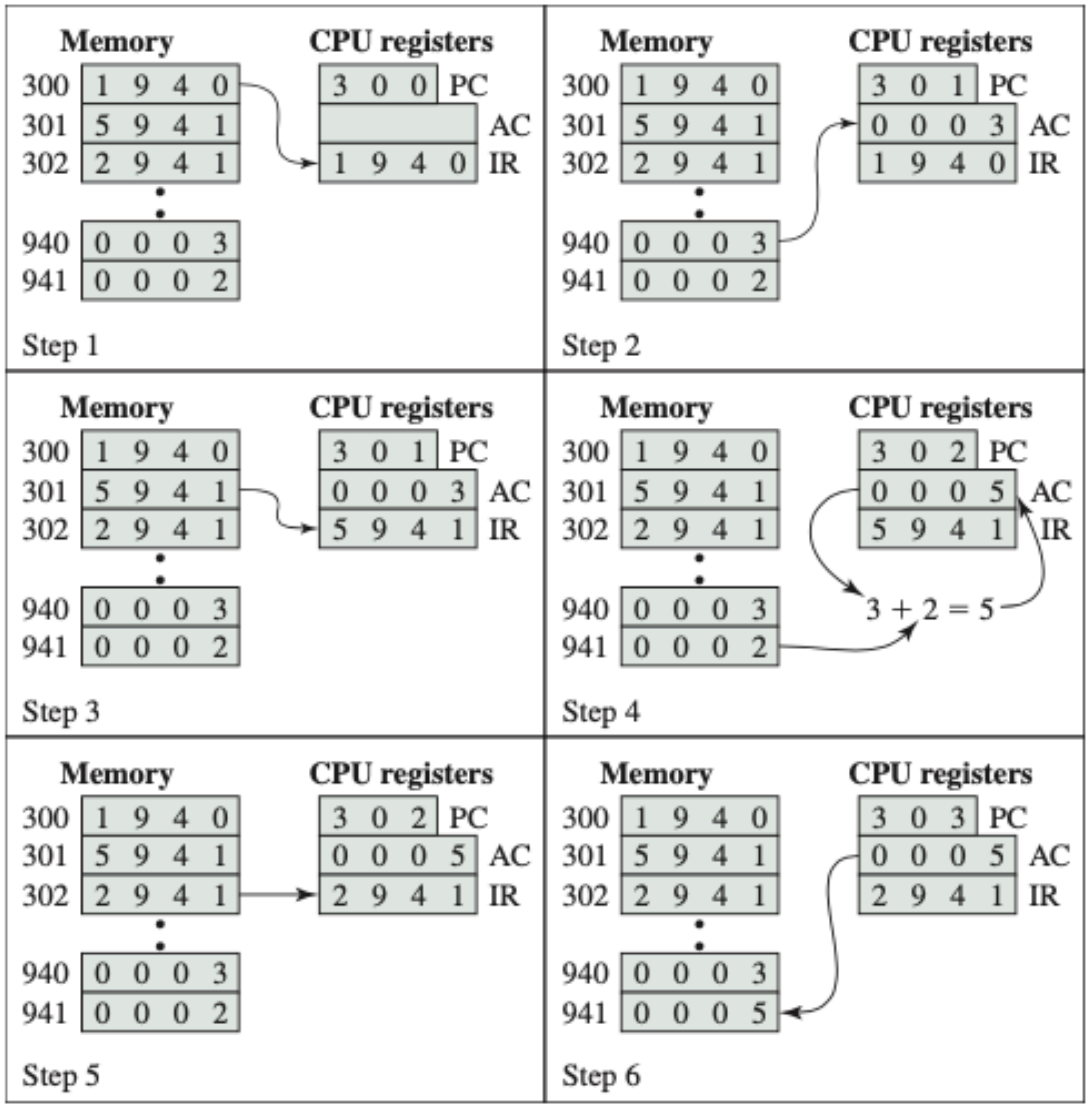


Figure 3.5 Example of Program Execution (contents of memory and registers in hexadecimal)