Computer Organization and Architecture MCQ

- [x] **Machine Instructions and Addressing Modes**
- [x] **ALU and Data-Path**
- [x] **CPU Control Design and Memory Interface**
- [x] **I/O Interface (Interrupt and DMA mode)**
- [x] **Instruction Pipelining and Cache**
- [x] **Main Memory and Secondary Storage**

Show

In which addressing mode the operand is given explicitly in the instruction itself?

A. Absolute mode
B. **Immediate mode**
C. Indirect mode
D. Index mode

Submitted By Payal Preet
Answer B

A basic instruction that can be interpreted by computer generally has

A. **An operand and an address**
B. A decoder and an accumulator
C. Sequence register and decoder
D. An address and decoder

Submitted By Payal Preet
Answer A

What is the bit storage capacity of a ROM with a 512 4-organization?

A. **2048**
B. 2049
C. 2047
D. 2046

Submitted By Payal Preet
Answer A

Which of the following is the internal memory of the system?

A. CPU register
B. Cache
C. Main memory
D. **All of these**

Submitted By Payal Preet
Answer D

Which of the following interrupt is non maskable

A. INTR
B. RST 7.5
C. RST 6.5
D. **TRAP**

Submitted By Payal Preet
Answer D

Intel 80486 was introduced in

A. 1985
B. 1986
C. 1987
D. **1989**

Submitted By Raghu Garg
Answer D

Which of following register pair can be directly stored in memory?

A. **BC**
B. HI
C. CD
D. DE

Submitted By Raghu Garg
Answer A

An instruction pipeline can be implemented by means of

A. LIFO buffer
B. **FIFO buffer**
C. Stack
D. None of the above

Submitted By Payal Preet
Answer B

The concept of pipelining is most effective in improving performance if the tasks being performed in different stages

A. Require different amount of time
B. **Require about the same amount of time**
C. Require different amount of time with time difference between any two tasks being same
D. Require different amount with time difference between any two tasks being different

Submitted By Payal Preet
Answer B

Performance of a pipelined processor suffers if

A. The pipeline stages have different delays
B. Consecutive instructions are dependent on each other
C. The pipeline stages share hardware resources
D. **All of these**

Submitted By Payal Preet
Answer D

<< ... 5 6 7 8 9 10 11 12 13 14