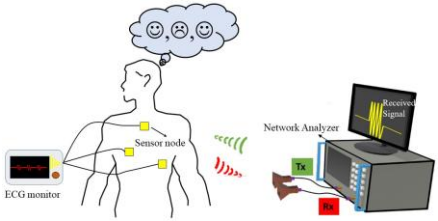
A novel artificial intelligence (AI) approach based on wireless signals could help to reveal our inner emotions, according to new research from Queen Mary University of London.

“The study, published in the journal *PLOS ONE*, demonstrates the use of radio waves to measure heartrate and breathing signals and predict how someone is feeling even in the absence of any other visual cues, such as facial expressions.”

“Participants were initially asked to watch a video selected by researchers for its ability to evoke one of four basic emotion types; anger, sadness, joy and pleasure. Whilst the individual was watching the video the researchers then emitted harmless radio signals, like those transmitted from any wireless system including radar or WiFi, towards the individual and measured the signals that bounced back off them. By analysing changes to these signals caused by slight body movements, the researchers were able to reveal 'hidden' information about an individual's heart and breathing rates.”

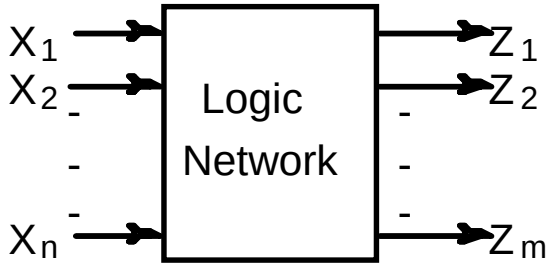


“Methods to detect human emotions are often used by researchers involved in psychological or neuroscientific studies but it is thought that these approaches could also have wider implications for the management of health and wellbeing.”

https://www.sciencedaily.com/releases/2021/02/210203144447.htm

Synchronous Digital Systems (SDS)

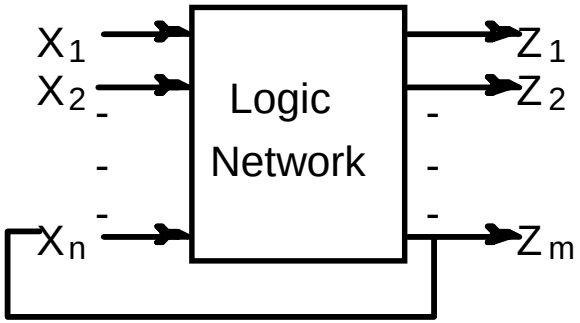
- Combinational Logic (CL)



Network of logic gates without feedback.

Outputs are functions only of inputs.

- Sequential Logic (SL)



The presence of feedback introduces the notion of "state."

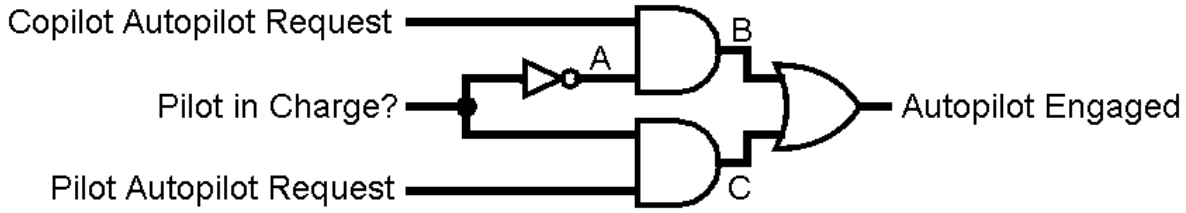
Circuits can "remember" or store information.

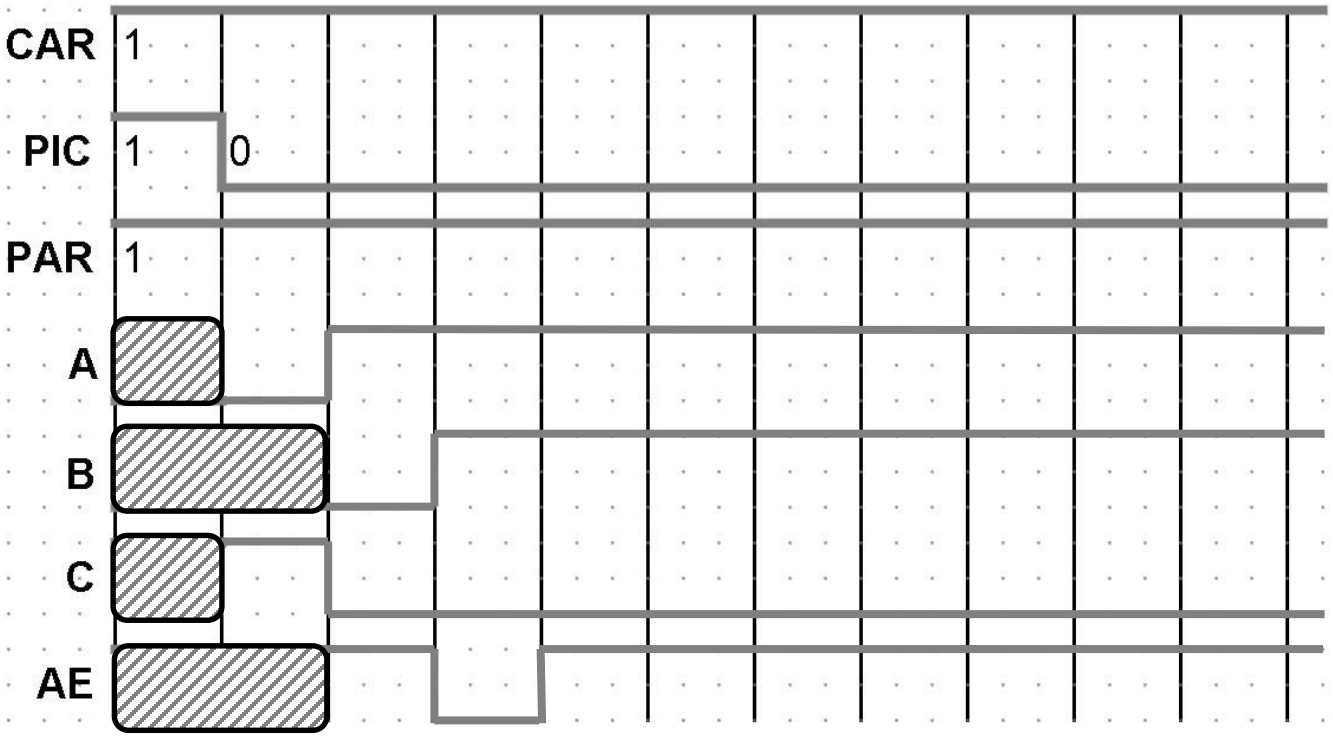
Uses for Sequential Logic

- Place to store values for some amount of time:
  - Registers
  - Memory
- *Help control flow of information between combinational logic blocks*
  - Hold up the movement of information to allow for orderly passage through CL

Circuit Timing: Hazards/Glitches

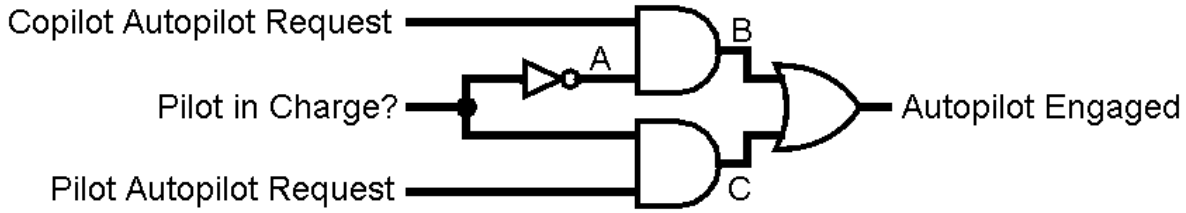
- Circuits can temporarily go to incorrect states!
  - Must assume output and intermediate signals are unknown if no other information is given

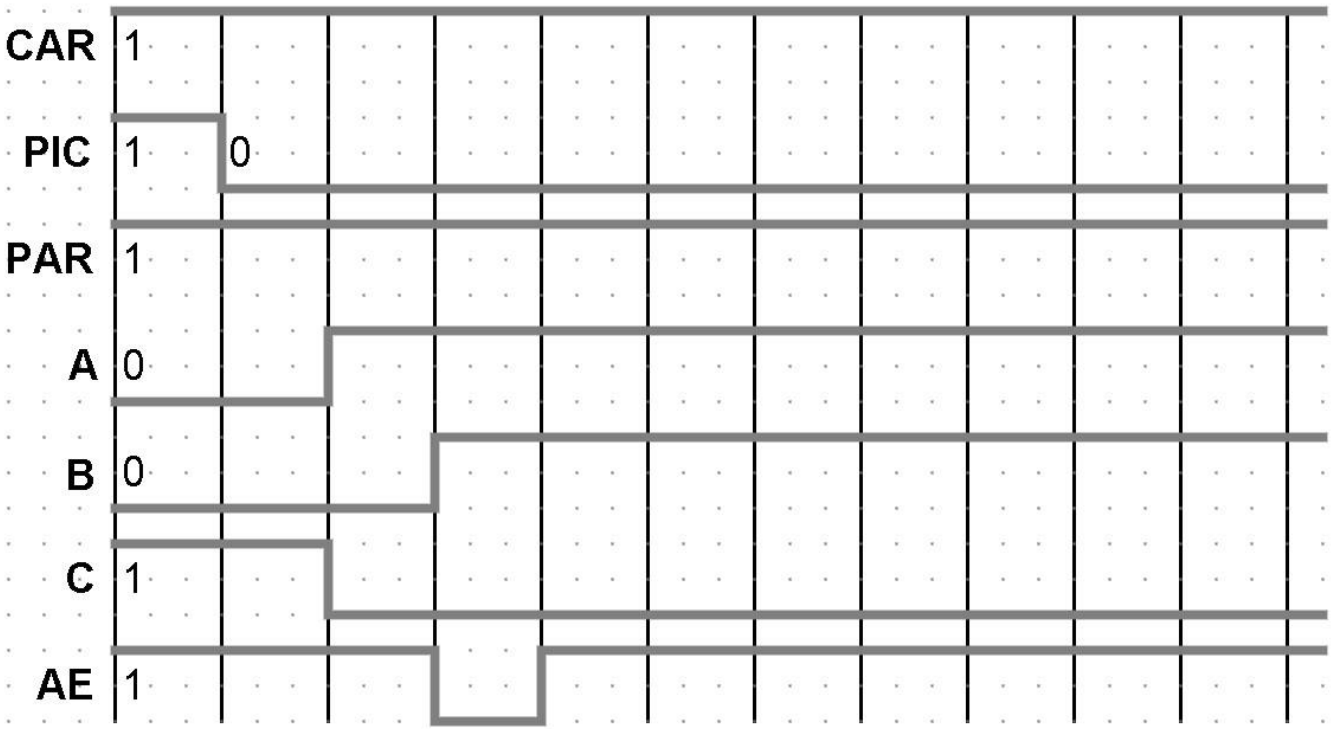




Control Flow of Information?

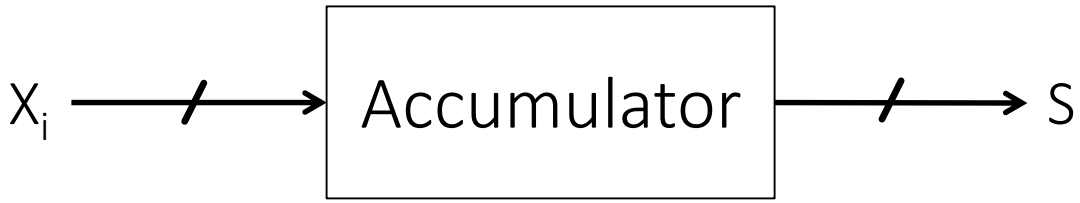
- Circuits can temporarily go to incorrect states!
  - Given values for intermediate and output signals





Accumulator Example

- An example of why we would need to control the flow of information.



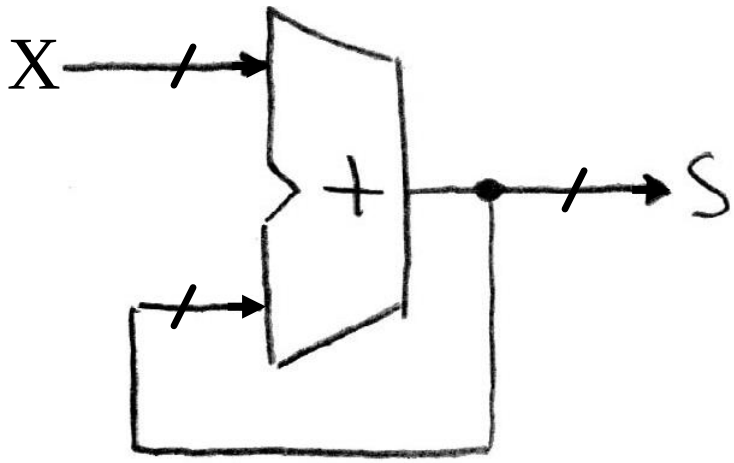
- Want:

```
S = 0;
for (i=0; i<n; i++)
    S = S + Xi;
```

- Assume:
  - Each X value is applied in succession, one per cycle
  - The sum since cycle 0 is present on S

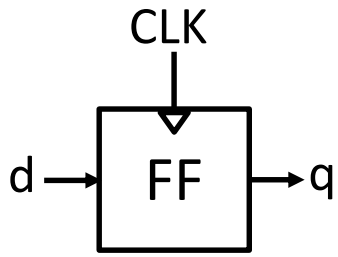
Accumulator: First Try

Does this work?

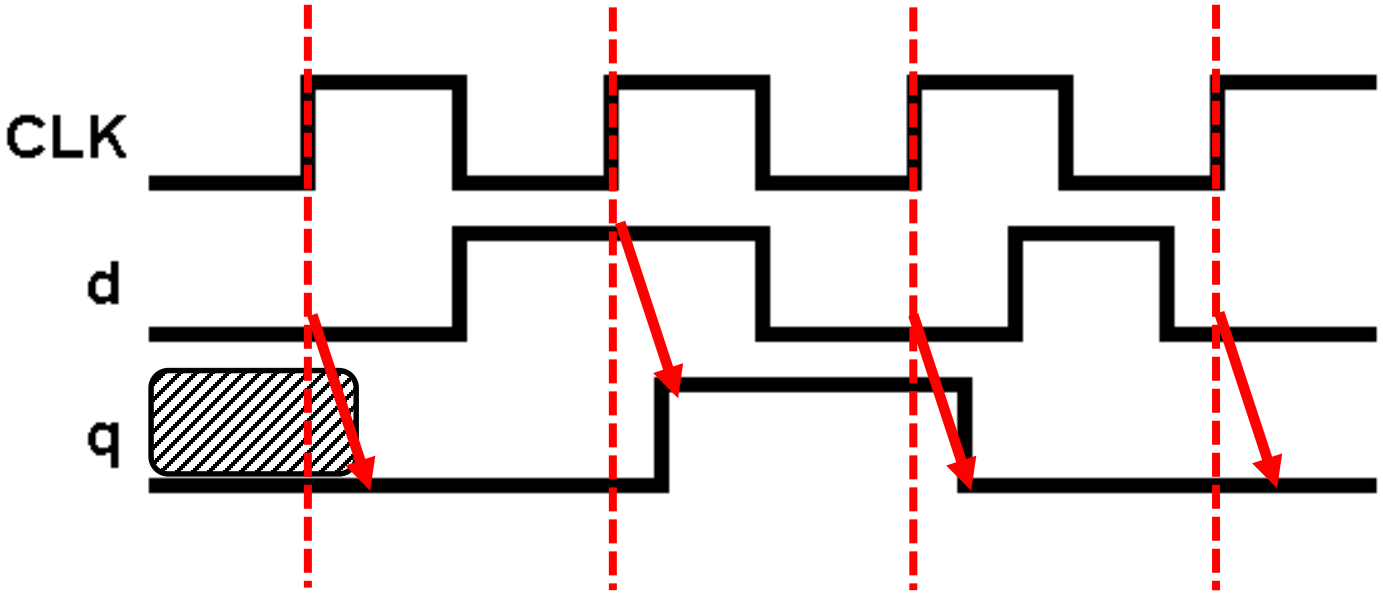


1) How to control the next iteration of the ‘for’ loop?
2) How do we say: ‘S=0’?

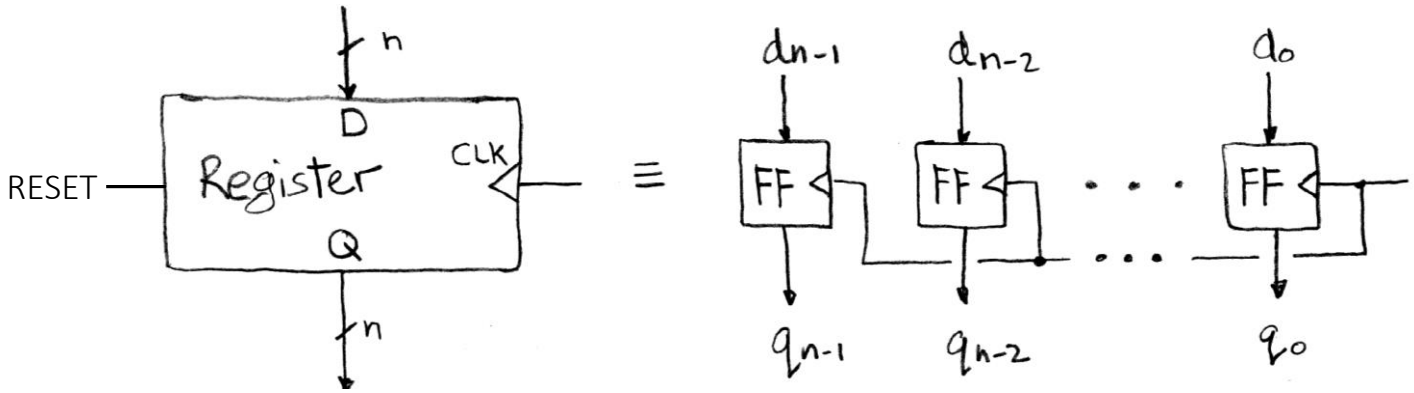
State Element: Flip-Flop



- Positive edge-triggered D-type flip flop
  - "On the rising edge of the clock (⌐↑), input d is sampled and transferred to the output q. At other times, the input d is ignored, and the previously sampled value is retained."

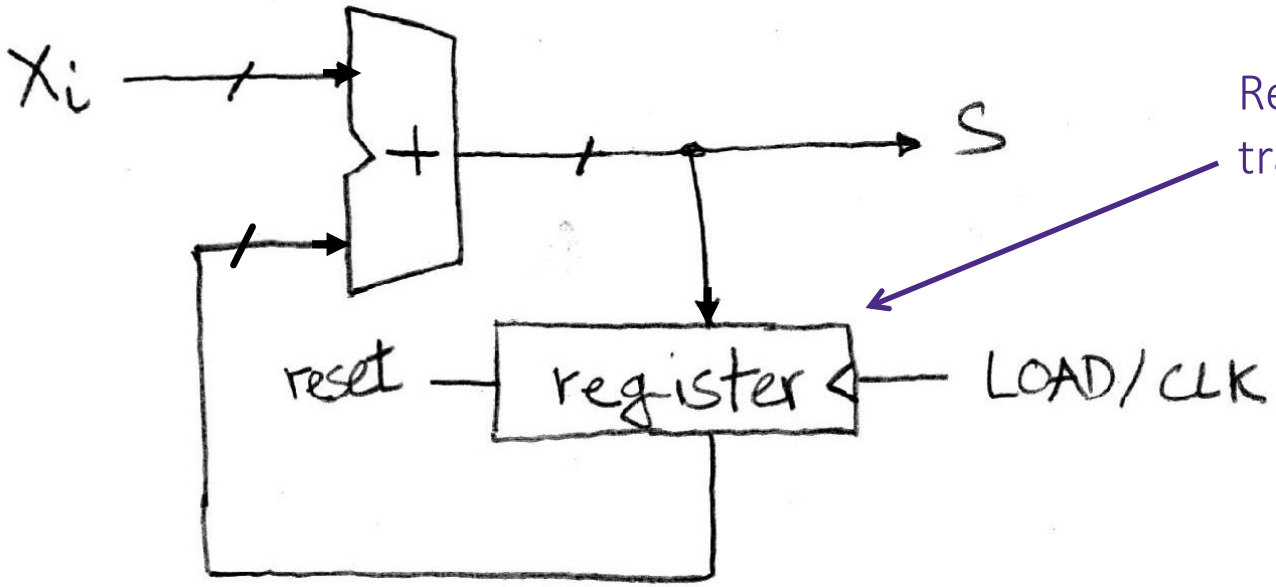


State Element: Register



- n instances of flip-flops together
  - One for every bit in input/output bus width
- Output `Q` resets to zero when `RESET` signal is high *during* clock trigger
  - Some extra circuitry required for this

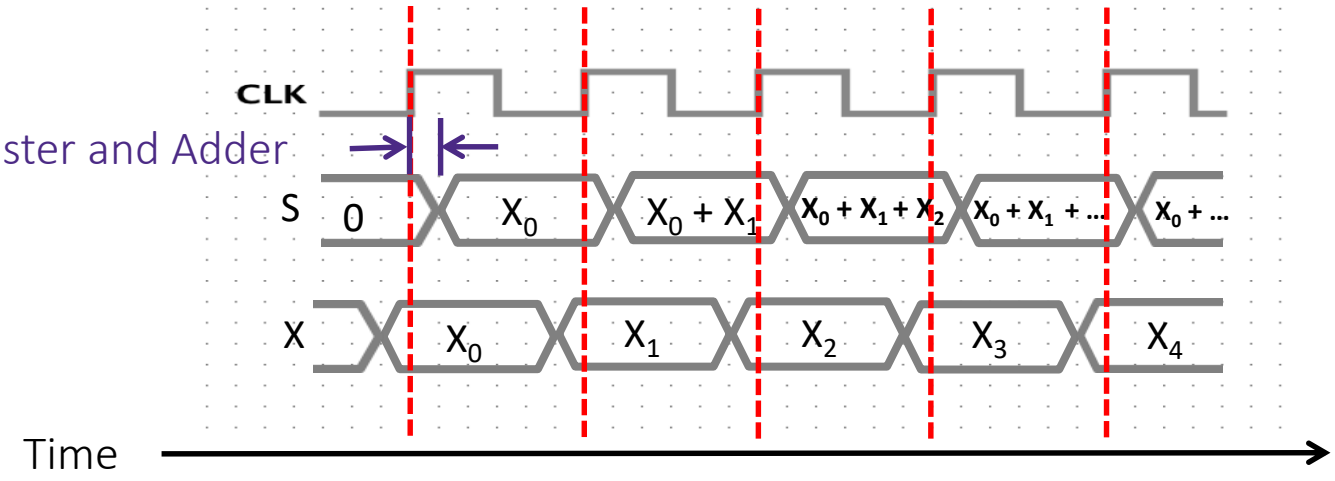
Accumulator: Second Try



Register holds up the transfer of data to adder

Delay through Register and Adder

Timing Diagram



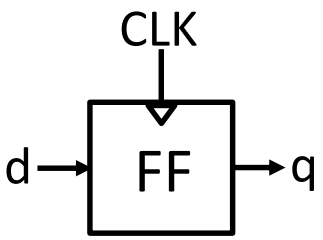
Flip-Flop Timing Terminology (1/2)

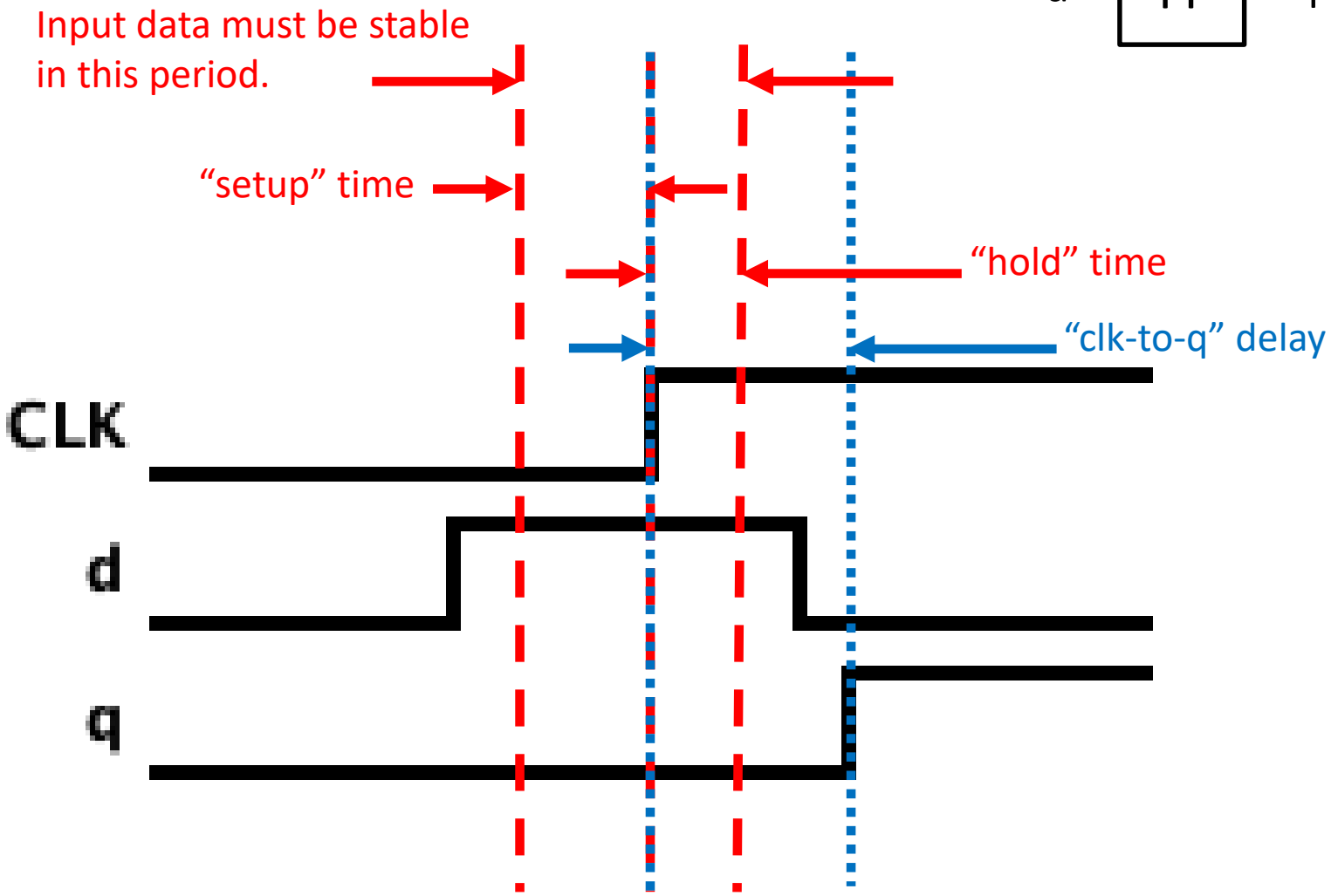
- Camera Analogy: non-blurry digital photo
  - *Don't move* while camera shutter is opening
  - *Don't move* while camera shutter is closing
  - *Check for blurriness* once image appears on the display

Flip-Flop Timing Terminology (2/2)

- Now applied to sequential logic elements:
  - *Setup Time:* how long the input must be stable *before* the CLK trigger for proper input read
  - *Hold Time:* how long the input must be stable *after* the CLK trigger for proper input read
  - *"CLK-to-Q" Delay:* how long it takes the output to change, measured from the CLK trigger

Flip-Flop Timing Behavior





Accumulator: Proper Timing

- `reset` signal shown
- Also, in practice X_i might not arrive at the adder at the same time as S_{i-1}
- S_i temporarily is wrong, but register always captures correct value
- In good circuits, instability never happens around rising edge of `CLK`