



Islamic University of Gaza
Faculty of Engineering
Computer Engineering Dept.

ECOM 3421 **Computer Architecture**

**Ch #3 | A Top-Level View of Computer
Function and Interconnection**

"We think of computers as smart and powerful machines.
But your goldfish is smarter.." 😊

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3.1 The hypothetical machine of Figure 3.4 also has two I/O instructions:

0011 = Load AC from I/O

0111 = Store AC to I/O

In these cases, the 12-bit address identifies a particular I/O device.

Show the program execution (using the format of Figure 3.5) for the following program:

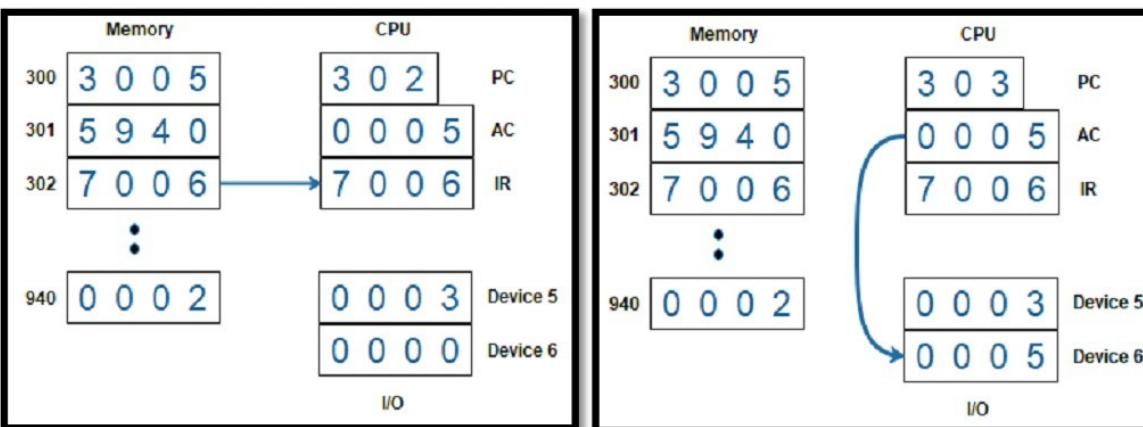
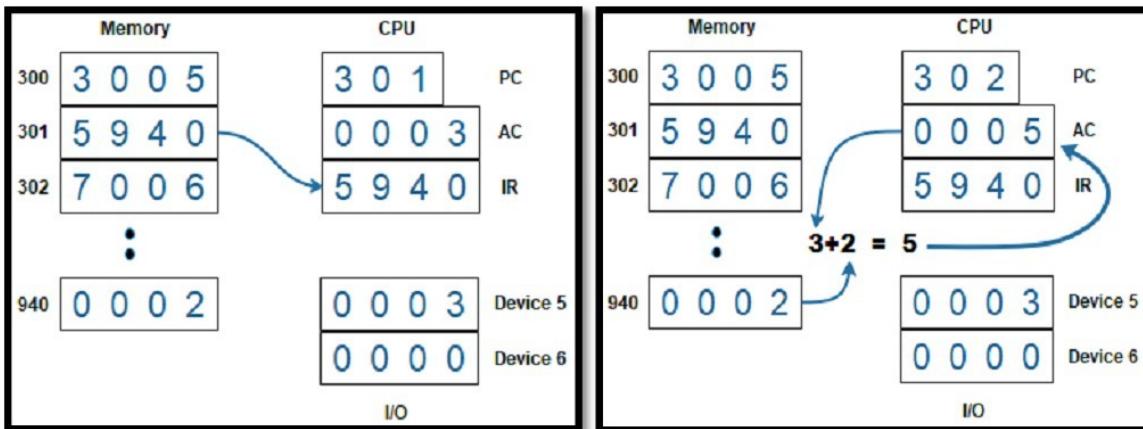
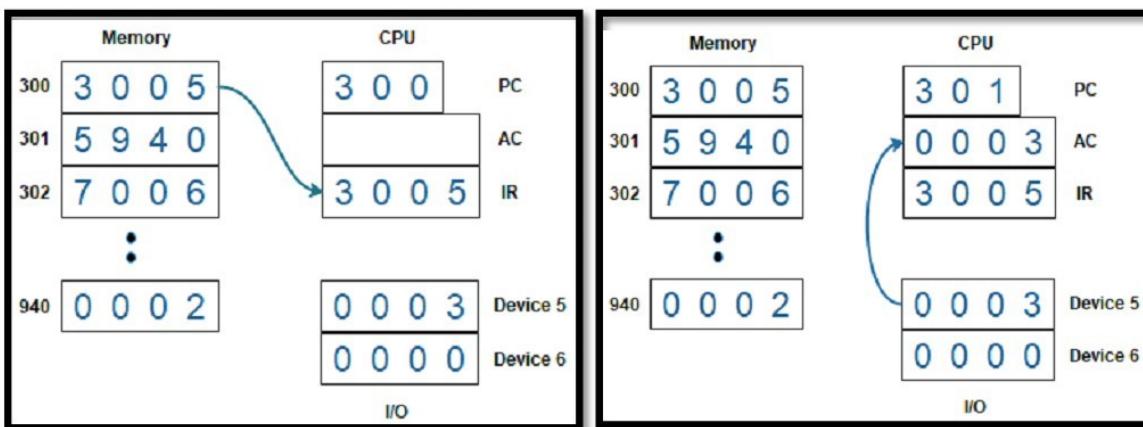
1. Load AC from device 5.

2. Add contents of memory location 940.

3. Store AC to device 6.

"Assume that the next value retrieved from device 5 is 3 and that location 940 contains a value of 2."

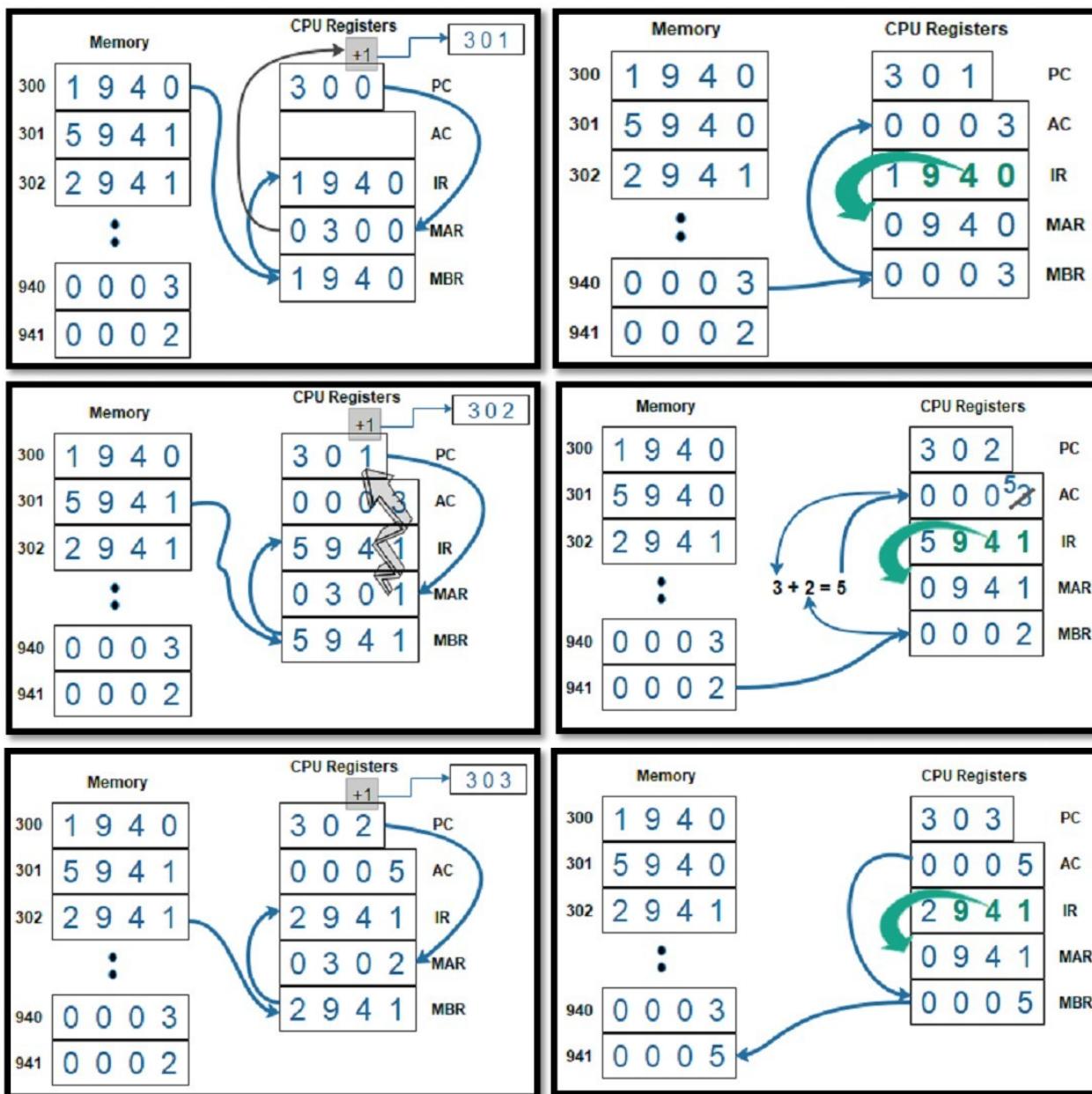
Answer:



3.2 The program execution of Figure 3.5 is described in the text using six steps.

Expand this description to show the use of the MAR and MBR.

Answer:



Description:

1. a) The PC contains 300, the address of the first instruction. This value is loaded in to the MAR.
b) The value in location 300 is loaded into the MBR, and the PC is incremented.
These two steps can be done in parallel.
c) The value in the MBR is loaded into the IR.

2. a) The address portion of the IR(940) is loaded into the MAR.
b) The value in location 840 is loaded into the MBR.
c) The value in the MBR is loaded into the AC.

3. a) The value in the PC(301) is loaded in to the MAR.
b) The value in location301 is loaded into the MBR, and the PC is incremented.
c) The value in the MBR is loaded into the IR.

4. a) The address portion of the IR(941) is loaded into the MAR.
b) The value in location 941 is loaded into the MBR.
c) The old value of the AC and the value of location MBR are added and
the result is stored in the AC.

5. a) The value in the PC (302) is loaded in to the MAR.
b) The value in location 302 is loaded into the MBR, and the PC is incremented.
c) The value in the MBR is loaded into the IR.

6. a) The address portion of the IR (941) is loaded into the MAR.
b) The value in the AC is loaded into the MBR.
c) The value in the MBR is stored in location 941.

- 3.3 Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.**

a. What is the maximum directly addressable memory capacity (in bytes)?

$$2^{24} = 16 \text{ MBytes.}$$

b. Discuss the impact on the system speed if the microprocessor bus has:

1. 32-bit local address bus and a 16-bit local data bus.

If the local address bus is 32 bits, the whole address can be transferred at once and decoded in memory.

However, since the data bus is only 16 bits, it will require 2 cycles to fetch a 32-bit instruction or operand.

2. 16-bit local address bus and a 16-bit local data bus.

The 16 bits of the address placed on the address bus can't access the whole referenced word of memory. Thus a more complex memory interface control is needed to latch the first part of the address and then the second part.

In addition to the two-step address operation , the microprocessor will need 2 cycles to fetch the 32 bit instruction/operand since the data bus is only 16 bits.

c. How many bits are needed for the program counter and the instruction register?

The program counter must be at least 24 bits.

The instruction register have to be 32-bits long, typically.

- 3.4 Consider a hypothetical microprocessor generating a 16-bit address (for example ,assume that the program counter and the address registers are 16 bits wide) and having a 16-bit data bus.**

a. What is the maximum memory address space that the processor can access directly if it is connected to a "16-bit memory"?

$2^{16} = 64 \text{ KBytes}$. Because address is 16-bit length.

b. What is the maximum memory address space that the processor can access directly if it is connected to an "8-bit memory"?

$2^{16} = 64 \text{ KBytes}$. Because address is 16-bit length.

Therefore, in (a) and (b), the microprocessor is to access 64K bytes, but the difference between them is that the access of 8-bit memory will transfer a 8 bits and the access of 16-bit memory may transfer 8 bits or 16 bits word.

c. What architectural features will allow this microprocessor to access a separate "I/O space"?

Separate I/O instructions are needed to generate separated I/O signals. That signals will be different from the memory signals which is generated during the execution for memory instructions.

Therefore, one more output pin will be needed to carry I/O signals.

/** Read this note:

As a CPU needs to communicate with the various memory and input-output devices (I/O) as we know data between the processor and these devices flow with the help of the system bus. There are three ways in which system bus can be allotted to them :

1. Separate set of address, control and data bus to I/O and memory.
this way is simple but require more buses.
2. Have common bus (data and address) for I/O and memory but separate control lines.
this way is called "Isolated I/O", and it is the mentioned in the question ☺.
Here we have different read-write instruction for both I/O and memory.
3. Have common bus (data, address, and control) for I/O and memory.
this way is called "Memory Mapped I/O", here the same set of instructions work for memory and I/O. Hence we manipulate I/O same as memory and both have same address space! **/

d. If an input and an output instruction can specify an 8-bit I/O port number.

How many 8-bit I/O ports can the microprocessor support?

$2^8 = 256$ of 8bit input ports and $2^8 = 256$ of 8bit output ports.

How many 16-bit I/O ports?

$2^8 = 256$ of 16bit input ports and $2^8 = 256$ of 16bit output ports.

Explain!

the microprocessor will distinguish between the same number of the input and output port by the signal that is generated by the executed I/O instruction.

- 3.5 Consider a 32-bit microprocessor, with a 16-bit external data bus, driven by an 8-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles.**

What is the maximum data transfer rate across the bus that this microprocessor can sustain, in bytes/sec?

$$\begin{aligned}\text{min bus cycle duration} &= 4 * \text{input clk cycles duration} \\ &= 4 * \frac{1}{\text{input clk freq}} = 4 * \frac{1}{8\text{MHZ}} = 0.5 * 10^{-6} \text{sec.}\end{aligned}$$

$$\begin{aligned}\text{max Data transfer rate across the bus} &= \frac{\# \text{bytes of bus}}{\text{min bus cycle duration}} \\ &= \frac{2 \text{bytes}}{0.5 * 10^{-6} \text{sec}} = 4 * 10^6 \frac{\text{bytes}}{\text{sec}}.\end{aligned}$$

To increase its performance, would it be better to make its external data bus 32 bits or to double the external clock frequency supplied to the microprocessor?
State any other assumptions you make, and explain.

Doubling the frequency may require a new chip manufacturing technology (assuming each instruction will have the same number of clock cycles),

** but we need to double the speed of the memory to prevent slowing the new microprocessor down.

Doubling the external data bus means wider on-chip data bus drivers / latches and modifications to the bus control logic.

** In this case, the "word length" of the memory will have to double to be able to send / receive 32-bit words.

it would be better to make the external bus 32 bits. This would double the bit rate across the external bus by the least cost.

- 3.6 Consider a computer system that contains an I/O module controlling a simple**

keyboard/printer teletype. The following registers are contained in the processor and connected directly to the system bus:

INPR	Input Register, 8 bits
OUTR	Output Register, 8 bits
FGI	Input Flag, 1 bit
FGO	Output Flag, 1 bit
IEN	Interrupt Enable, 1 bit

Keystroke input from the teletype and printer output to the teletype are controlled by the I/O module.

The teletype is able to encode an alphanumeric symbol to an 8-bit word and decode an 8-bit word into an alphanumeric symbol.

- a. *Describe how the processor, using the first four registers listed in this problem, can achieve I/O with the teletype.*

Input from the Teletype is stored in INPR.

The INPR will only accept data from the Teletype when FGI=0.

When data arrives, it is stored in INPR, and FGI is set to 1.

** The CPU **periodically** checks FGI, because there is no IEN!

If FGI =1, the CPU transfers the contents of INPR to the AC and sets FGI to 0.

** When the CPU has data to send to the Teletype, it checks FGO.

If FGO = 0, that means a transferring operation is happening now, the CPU must wait.

If FGO = 1, the CPU transfers the contents of the AC to OUTR and sets FGO to 0.

- b. *Describe how the function can be performed more efficiently by also employing IEN.*

The process described in (a) requires periodically checks which is very wasteful.

The CPU, which is much faster than the Teletype, must repeatedly check FGI and FGO!

If interrupts are used,

By employing IEN register, the Teletype can issue/make an interrupt to the CPU

whenever it is ready to accept or send data. The IEN register can be set by the CPU.

- 3.7 *Consider two microprocessors having 8- & 16-bit-wide external data buses, respectively. The two processors are identical otherwise and their bus cycles take just as long.*

*a. Suppose all instructions and operands are **two bytes** long. By what factor do the maximum data transfer rates differ?*

To transfer the 2-bytes instruction or operand, the 16-bit microprocessor takes single bus cycle for the transfer, but the 8-bit microprocessor takes two cycles.

The date transfer rate of the 16-bit microprocessor is as twice of the transfer rate of the 8-bit microprocessor.

2:1

b. Repeat assuming that half of the operands and instructions are one byte long

Assume we do "2N" transferring operations of operands and instructions, so N of them are one byte long and N of them are two bytes long.

The 16-bit microprocessor takes $2N$ cycles for the transfer, but The 8-bit microprocessor takes $3N$ cycles.

The date transfer rate of the 16-bit microprocessor is as " $3/2$ " of the transfer rate of the 8-bit microprocessor.