



# BAHRIA UNIVERSITY, (KARACHI CAMPUS)

Department of Software Engineering

Digital Assignment 2 - Fall 2021

COURSE TITLE:	<b>Computer Architecture &amp; Logic Design</b>	COURSE CODE:	<b>CEN-220</b>
Class:	BSE[3]-A/B	Shift:	<b>Morning</b>
Course Instructor:	<b>DR. SYED SAMAR YAZDANI</b>	Time Allowed:	
Submission Date:	<b>13-01-2022</b>	Max. Marks:	<b>10 Marks</b>

## Cache Sim Demo

Now that we are more familiar with how caches work, let's get some practice with the cache simulator!

Before generating set:

"Address Width"  $\Rightarrow$  6, "Cache Size"  $\Rightarrow$  16, "Block Size"  $\Rightarrow$  4, "Associativity"  $\Rightarrow$  2

A) Determine the following:

i) Highest Address in Memory: \_\_\_\_\_ ii) Number of Sets in Cache: \_\_\_\_\_

B) We want to make a read at address 0x2A. Determine the following:

i) The Set containing the block that was read is number \_\_\_\_\_. ii) The tag bit in this block is \_\_\_\_\_.

iii) The full 4 bytes in this block are (in order) 0x\_\_\_\_\_, 0x\_\_\_\_\_, 0x\_\_\_\_\_, 0x\_\_\_\_\_.

C) We want to write at address 0x1B the value '0xB1'. Determine the following:

i) The Set containing the block that was read is number \_\_\_\_\_. ii) The tag bit in this block is \_\_\_\_\_.

iii) Notice that the value stored in the cache is now different from the value stored in memory. What, in the cache, indicates this disparity? Given that this was a write miss, what would have happened if our write miss policy were "No Write-Allocate" instead?

D) We want to make a read at address 0x01. Determine the following:

i) The Set containing the block that was read is number \_\_\_\_\_.

ii) The Tag bit in this block is \_\_\_\_\_.

iii) Will this read cause a conflict in the cache? Yes ☐ No ☐

iv) If yes, which block will be evicted? Read made in B Write made in C

E) We want to write at address 0x1C the value '0xE9'. Determine the following:

i) The Set containing the block that was read is number \_\_\_\_\_. ii) The tag bit in the block is \_\_\_\_\_.

iii) Will this write cause a conflict in the cache? Yes ☐ No ☐

iv) If yes, which block will be evicted? Read made in B Write made in C

As a note, your history should look like this:

$R(0 \times 2a) = M$

$W(0 \times 1b, 0 \times b1) = M$

$R(0 \times 01) = M$

$W(0 \times 1c, 0 \times e9) = M$

G) Append the following text to the current History:

$W(0 \times 03, 0 \times ff)$

$R(0 \times 27)$

$R(0 \times 10)$

$W(0 \times 1d, 0 \times 00)$

You'll notice that appended to each of these memory accesses is “ = ?”

Determine if ‘?’ will resolve to Hit (H) or Miss (M) for each execution.

i)  $W(0 \times 03, 0 \times ff) = \underline{\hspace{2cm}}$ . ii)  $R(0 \times 27) = \underline{\hspace{2cm}}$ . iii)  $R(0 \times 10) = \underline{\hspace{2cm}}$ .

iv)  $W(0 \times 1d, 0 \times 00) = \underline{\hspace{2cm}}$ .

H) The cache, after the 8 executions detailed above should look like this:

V D T Cache Data									
Set 0	1	1	0	20	f6	ef	ff		2
	1	0	2	b8	bd	1a	ca		1
Set 1	1	1	3	e9	00	f6	e5		1
	1	0	4	1a	6f	7e	63		2

The numbers on the right indicate the mode recent use of the cache (where 1 was more recent).

i) A LRU replacement policy will evict which block on the next cache conflict?

ii) What is one benefit of using LRU over Random?

iii) What is one benefit of using Random over LRU?

I) If we were to flush the cache right now (don't actually) how many bytes in memory would change? \_\_ Bytes

How many bytes would change if our “Write Hit” policy were “Write Through” instead of “Write Back”? \_\_ Bytes

Can you explain why these numbers are the same/different? (If not, try changing the write hit policy and re-running using the same history above).