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BAHRIA UNIVERSITY (KARACHI CAMPUS)

ASSIGNMENT I – Fall 2021

COMPUTER ARCHITECTURE & LOGIC DESIGN

Class: **BSE[4]- 2(A)/(B)**

Course Instructor: **Dr. Syed Samar Yazdani**

Date: **17.11.2021**

Student's Name: **Muhammad Junaid Saleem Qadri**

Due Date: _____

Max Marks: **10 Marks**

Reg. No: **70003**

Note:

❖ *Attempt all questions*

Question 1

[CLO 3]

A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45,000	1
Data transfer	32,000	2
Floating point	15,000	2
Control transfer	8000	2

Determine the effective *CPI*, and execution time for this program.

SOLUTION:-

CPI (average Clocks per instructions) =

$$45000 + (2 \times 32000) + (2 \times 15000) + (8000 \times 2) / (100\ 000) = 155 / 100 = \mathbf{1.55}$$

$$\text{MIPS} = 40\ \text{M clocks / sec} \times (1 / 1.55\ \text{clocks per instruction}) = 40 / 1.55 / 1000000 = \mathbf{25.8\ \text{MIPs}}$$

$$\text{Execution time} = (100\ 000\ \text{instructions}) \times 1.55\ \text{CPI} = 155\ 000\ \text{cycles} \times 1 / 40\ \text{M sec} = \mathbf{3.87\ \text{ms}}$$

Stallings: CPI = 1.55; MIPS rate = 25.8; Execution time = 3.87 ms.

Enrollment number : 02-131202-057

Reg. no : 70003

Question 2**[CLO 3]**

Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs:

Instruction Type	Instruction Count (millions)	Cycles per Instruction
Machine A		
Arithmetic and logic	8	1
Load and store	4	3
Branch	2	4
Others	4	3
Machine B		
Arithmetic and logic	10	1
Load and store	8	2
Branch	2	4
Others	4	3

- Determine the effective *CPI*, MIPS rate, and execution time for each machine.
- Comment on the results.

SOLUTION:-

a)

$$CPI_A = \frac{\sum CPI_i \times I_i}{I_c} = \frac{(8 \times 1 + 4 \times 3 + 2 \times 4 + 4 \times 3) \times 10^6}{(8 + 4 + 2 + 4) \times 10^6} \approx 2.22$$

$$MIPS_A = \frac{f}{CPI_A \times 10^6} = \frac{200 \times 10^6}{2.22 \times 10^6} = 90$$

$$CPU_A = \frac{I_c \times CPI_A}{f} = \frac{18 \times 10^6 \times 2.2}{200 \times 10^6} = 0.2 \text{ s}$$

$$CPI_B = \frac{\sum CPI_i \times I_i}{I_c} = \frac{(10 \times 1 + 8 \times 2 + 2 \times 4 + 4 \times 3) \times 10^6}{(10 + 8 + 2 + 4) \times 10^6} \approx 1.92$$

$$MIPS_B = \frac{f}{CPI_B \times 10^6} = \frac{200 \times 10^6}{1.92 \times 10^6} = 104$$

$$CPU_B = \frac{I_c \times CPI_B}{f} = \frac{24 \times 10^6 \times 1.92}{200 \times 10^6} = 0.23 \text{ s}$$

- b) Even though, machine B has a higher MIPS than machine A, it needs a longer CPU time to execute the similar set of benchmark programs (instructions).

Question 3

[CLO 3]

The hypothetical machine of Figure 3.4 also has two I/O instructions:

0011 = Load AC from I/O

0111 = Store AC to I/O

In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 3.5) for the following program:

1. Load AC from device 5.
2. Add contents of memory location 940.
3. Store AC to device 6.

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SOLUTION :-

Assume that the next value retrieved from device 5 is 3 and that location 940 contains a value of 2.

STEP1 Memory

300	3 0 0 5
301	5 9 4 0
302	7 0 0 6
:	
940	0 0 0 2
941	

CPU Registers

3 0 0	PC
	AC
3 0 0 5	IR
I/O devices	
0 0 5	0 0 0 3
0 0 6	

STEP2 Memory

300	3 0 0 5
301	5 9 4 0
302	7 0 0 6
:	
940	0 0 0 2
941	

CPU Registers

3 0 1	PC
0 0 0 3	AC
3 0 0 5	IR
I/O devices	
0 0 5	0 0 0 3
0 0 6	

STEP3 Memory

300	3 0 0 5
301	5 9 4 0
302	7 0 0 6
:	
940	0 0 0 2
941	

CPU Registers

3 0 1	PC
0 0 0 3	AC
5 9 4 0	IR
I/O devices	
0 0 5	0 0 0 3
0 0 6	

STEP4 Memory

300	3 0 0 5
301	5 9 4 0
302	7 0 0 6
:	
940	0 0 0 2
941	

CPU Registers

3 0 2	PC
0 0 0 5	AC
5 9 4 0	IR
I/O devices	
0 0 5	0 0 0 3
0 0 6	

STEP5 Memory

300	3 0 0 5
301	5 9 4 0
302	7 0 0 6
:	
940	0 0 0 2
941	

CPU Registers

3 0 2	PC
0 0 0 5	AC
7 0 0 6	IR
I/O devices	
0 0 5	0 0 0 3
0 0 6	

STEP6 Memory

300	3 0 0 5
301	5 9 4 0
302	7 0 0 6
:	
940	0 0 0 2
941	

CPU Registers

3 0 3	PC
0 0 0 5	AC
7 0 0 6	IR
I/O devices	
0 0 5	0 0 0 3
0 0 6	0 0 0 5

Question 4

[CLO 3]

The program execution of Figure 3.5 is described in the text using six steps. Expand this description to show the use of the MAR and MBR.

SOLUTION :-

STEP 1:

- A) The PC contains 300, the address of the first instruction. This value is loaded in to the MAR.
- B) The value in location 300 is loaded into the MBR, and the PC is incremented. These two steps can be done in parallel.
- C) The value in the MBR is loaded into the IR.

STEP 2:

- A) The address portion of the IR (940) is loaded into the MAR.
- B) The value in location 840 is loaded into the MBR.
- C) The value in the MBR is loaded into the AC.

STEP 3:

- A) The value in the PC (301) is loaded in to the MAR.
- B) The value in location 301 is loaded into the MBR, and the PC is incremented.
- C) The value in the MBR is loaded into the IR.

STEP 4:

- A) The address portion of the IR (941) is loaded into the MAR.
- B) The value in location 941 is loaded into the MBR.
- C) The old value of the AC and the value of location MBR are added and the result is stored in the AC.

STEP 5:

- A) The value in the PC (302) is loaded into the MAR.
- B) The value in location 302 is loaded into the MBR, and the PC is incremented.
- C) The value in the MBR is loaded into the IR.

STEP 6:

- A) The address portion of the IR (941) is loaded into the MAR.
- B) The value in the AC is loaded into the MBR.
- C) The value in the MBR is stored in location 941.

Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.

- a. What is the maximum directly addressable memory capacity (in bytes)?
- b. Discuss the impact on the system speed if the microprocessor bus has:
 1. 32-bit local address bus and a 16-bit local data bus, or
 2. 16-bit local address bus and a 16-bit local data bus.
- c. How many bits are needed for the program counter and the instruction register?



(a) Instruction format



(b) Integer format

Program counter (PC) = Address of instruction
 Instruction register (IR) = Instruction being executed
 Accumulator (AC) = Temporary storage

(c) Internal CPU registers

0001 = Load AC from memory
 0010 = Store AC to memory
 0101 = Add to AC from memory

(d) Partial list of opcodes

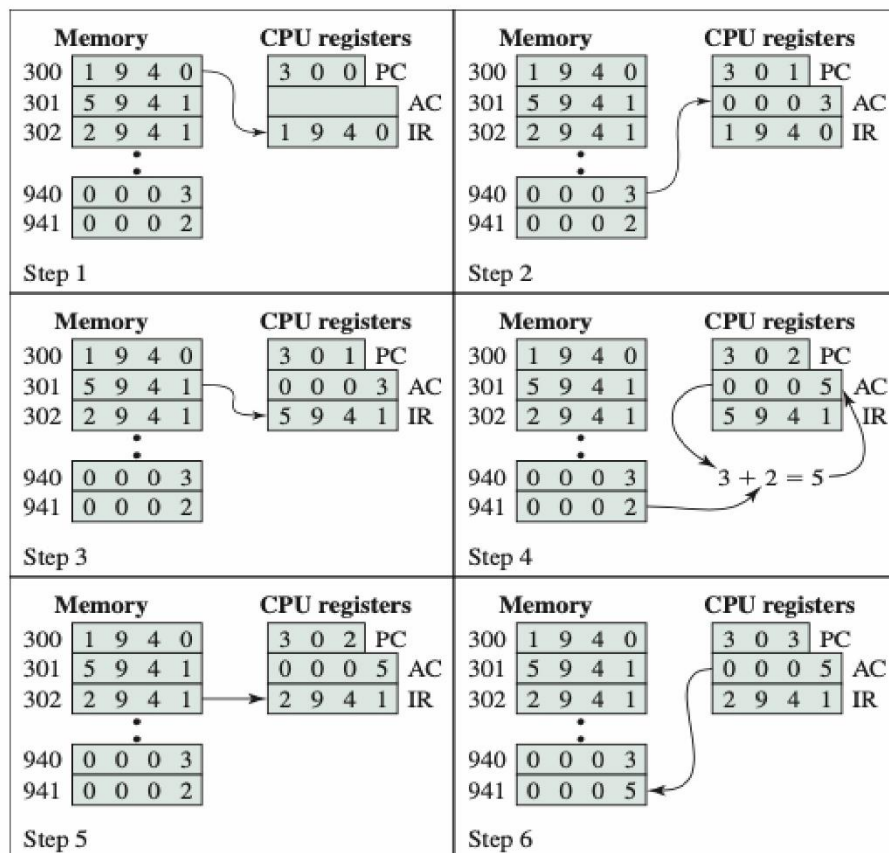


Figure 3.5 Example of Program Execution (contents of memory and registers in hexadecimal)

SOLUTION :-

a) $2^{(32-8)} = 2^{24} = 16,777,216 \text{ bytes} = 16 \text{ MB}$,(8 bits = 1 byte for the opcode).

b,1) A 32-bit local address bus and a 16-bit local data bus. Instruction and data transfers would take three bus cycles each, one for the address and two for the data. Since If the address bus is 32 bits, the whole address can be transferred to memory at once and decoded there; however, since the data bus is only 16 bits, it will require 2 bus cycles (accesses to memory) to fetch the 32-bit instruction or operand.

b,2) A 16-bit local address bus and a 16-bit local data bus. Instruction and data transfers would take four bus cycles each, two for the address and two for the data. Therefore, that will have the processor perform two transmissions in order to send to memory the whole 32-bit address; this will require more complex memory interface control to latch the two halves of the address before it performs an access to it. In addition to this two-step address issue, since the data bus is also 16 bits, the microprocessor will need 2 bus cycles to fetch the 32-bit instruction or operand.

c) For the PC needs 24 bits (24-bit addresses), and for the IR needs 32 bits (32-bit addresses).



THE END

