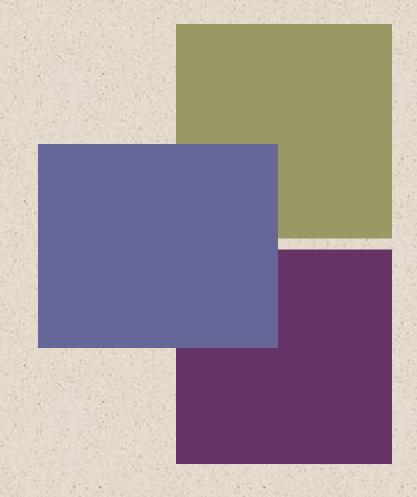


William Stallings
Computer Organization
and Architecture
10th Edition



₊ Chapter 3

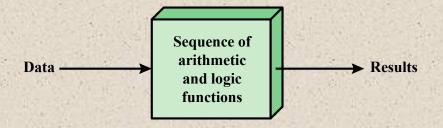
A Top-Level View of Computer Function and Interconnection

Computer Components

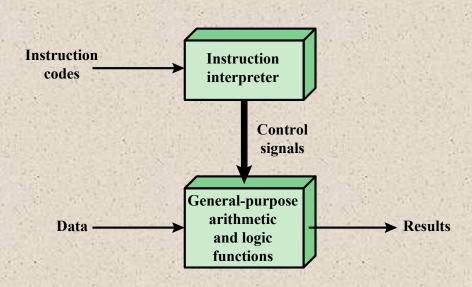
- Contemporary computer designs are based on concepts developed by John von Neumann at the Institute for Advanced Studies, Princeton
- Referred to as the *von Neumann architecture* and is based on three key concepts:
 - Data and instructions are stored in a single read-write memory
 - The contents of this memory are addressable by location, without regard to the type of data contained there
 - Execution occurs in a sequential fashion (unless explicitly modified) from one instruction to the next
- Hardwired program
 - The result of the process of connecting the various components in the desired configuration



Hardware and Software Approaches



(a) Programming in hardware



(b) Programming in software

Figure 3.1 Hardware and Software Approaches

Software

- A sequence of codes or instructions
- Part of the hardware interprets each instruction and generates control signals
- Provide a new sequence of codes for each new program instead of rewiring the hardware

Major components:

- CPU
 - Instruction interpreter
 - Module of general-purpose arithmetic and logic functions
- I/O Components
 - Input module
 - Contains basic components for accepting data and instructions and converting them into an internal form of signals usable by the system
 - Output module
 - Means of reporting results

Software

I/O Components



Memory address register (MAR)

 Specifies the address in memory for the next read or write

I/O address register (I/OAR)

Specifies a particular I/O device

Memory buffer register (MBR)

 Contains the data to be written into memory or receives the data read from memory

I/O buffer register (I/OBR)

 Used for the exchange of data between an I/O module and the CPU

MEMORY

MAR

MBR

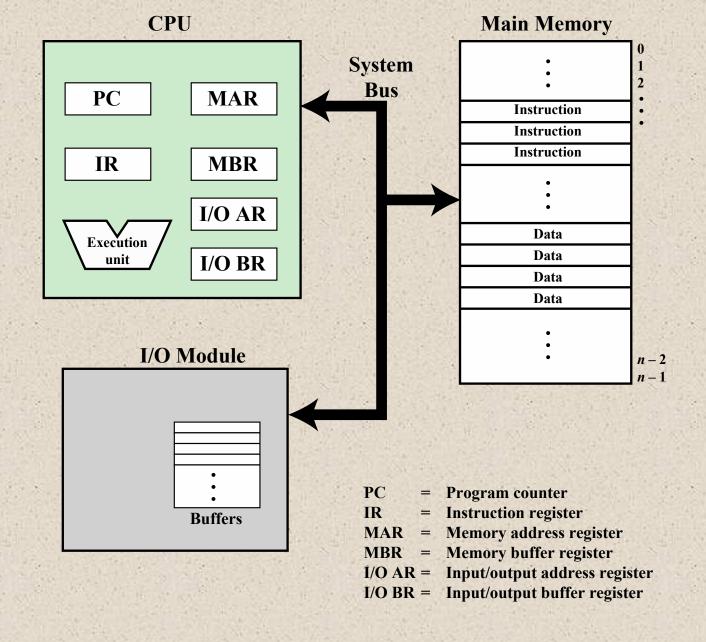


Figure 3.2 Computer Components: Top-Level View

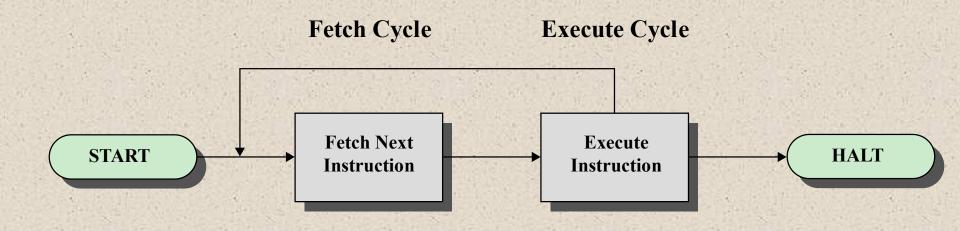


Figure 3.3 Basic Instruction Cycle

Fetch Cycle

- At the beginning of each instruction cycle the processor fetches an instruction from memory
- The program counter (PC) holds the address of the instruction to be fetched next
- The processor increments the PC after each instruction fetch so that it will fetch the next instruction in sequence
- The fetched instruction is loaded into the instruction register (IR)
- The processor interprets the instruction and performs the required action

Action Categories

