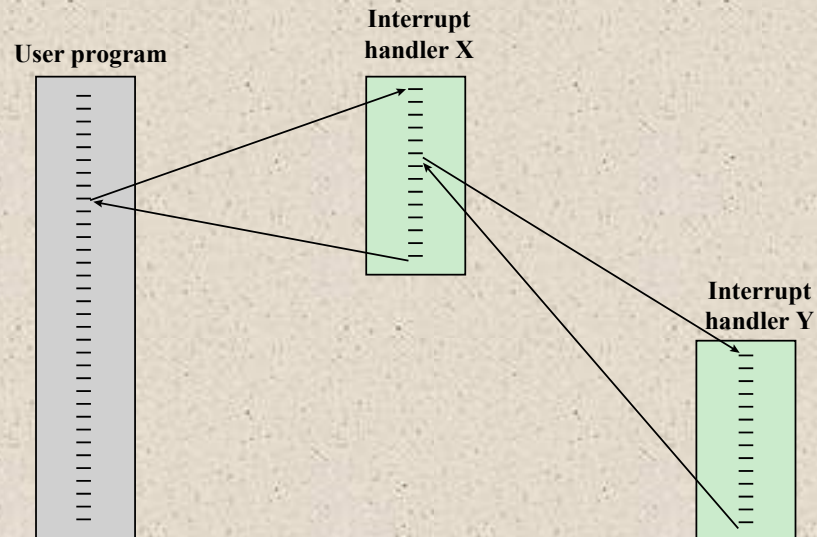**(a) Sequential interrupt processing**

**(b) Nested interrupt processing**

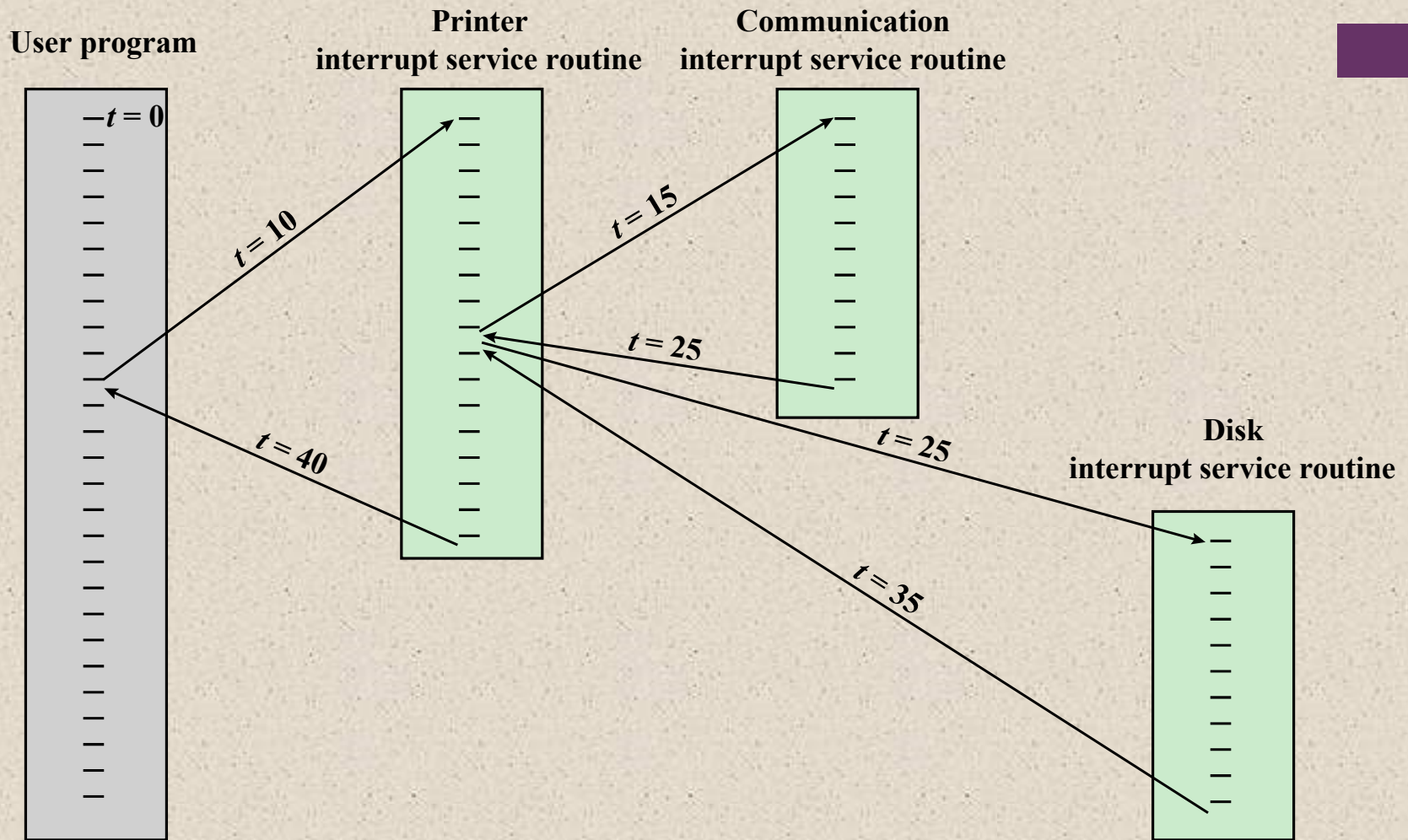**Figure 3.13  Transfer of Control with Multiple Interrupts**

**Figure 3.14  Example Time Sequence of Multiple Interrupts**

# I/O Function

- I/O module can exchange data directly with the processor

- Processor can read data from or write data to an I/O module
  - Processor identifies a specific device that is controlled by a particular I/O module
  - I/O instructions rather than memory referencing instructions

- In some cases it is desirable to allow I/O exchanges to occur directly with memory
  - The processor grants to an I/O module the authority to read from or write to memory so that the I/O memory transfer can occur without tying up the processor
  - The I/O module issues read or write commands to memory relieving the processor of responsibility for the exchange
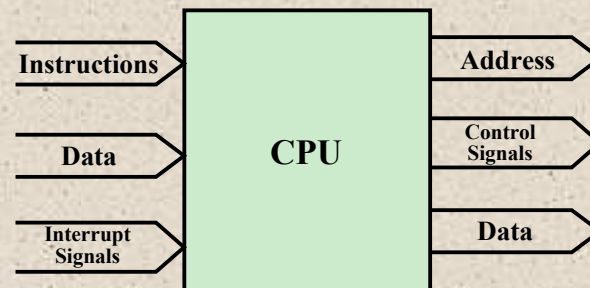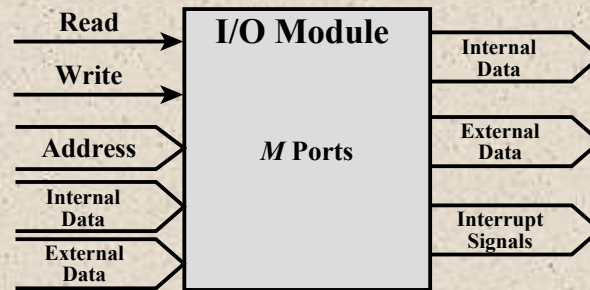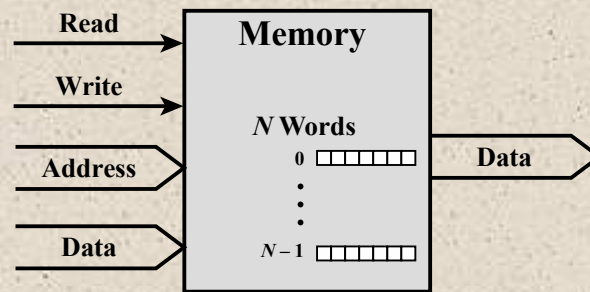  - This operation is known as direct memory access (DMA)

Read → **Memory**

Write →

*N* Words

Address → 0 ▭▭▭▭▭▭ → Data

⋮

Data → *N* − 1 ▭▭▭▭▭▭

---

Read → **I/O Module**

Write →

Internal Data →

Address → *M* Ports

External Data →

Internal Data →

External Data →

Interrupt Signals →

---

Instructions → Address →

Control Signals →

Data → **CPU**

Interrupt Signals → Data →

**Figure 3.15  Computer Modules**

# The interconnection structure must support the following types of transfers:

| Memory to processor | Processor to memory | I/O to processor | Processor to I/O | I/O to or from memory |
|---|---|---|---|---|
| Processor reads an instruction or a unit of data from memory | Processor writes a unit of data to memory | Processor reads data from an I/O device via an I/O module | Processor sends data to the I/O device | An I/O module is allowed to exchange data directly with memory without going through the processor using direct memory access |

**Bus Interconnection**

A communication pathway connecting two or more devices
- Key characteristic is that it is a shared transmission medium

Signals transmitted by any one device are available for reception by all other devices attached to the bus
- If two devices transmit during the same time period their signals will overlap and become garbled

Typically consists of multiple communication lines
- Each line is capable of transmitting signals representing binary 1 and binary 0

Computer systems contain a number of different buses that provide pathways between components at various levels of the computer system hierarchy

*System bus*
- A bus that connects major computer components (processor, memory, I/O)

The most common computer interconnection structures are based on the use of one or more system buses

# Data Bus

- Data lines that provide a path for moving data among system modules

- May consist of 32, 64, 128, or more separate lines

- The number of lines is referred to as the *width* of the data bus

- The number of lines determines how many bits can be transferred at a time

- The width of the data bus is a key factor in determining overall system performance
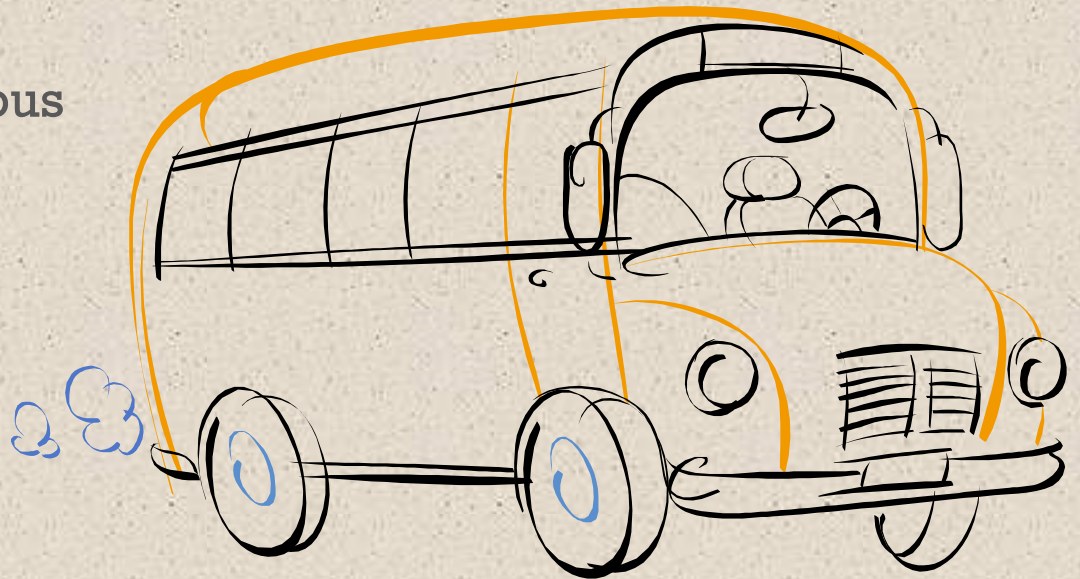
# Address Bus

# Control Bus
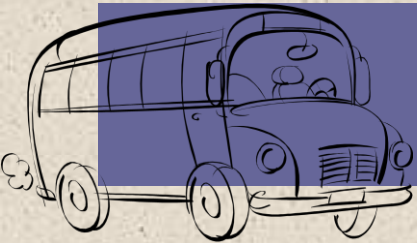
- Used to designate the source or destination of the data on the data bus
  - If the processor wishes to read a word of data from memory it puts the address of the desired word on the address lines

- Width determines the maximum possible memory capacity of the system

- Also used to address I/O ports
  - The higher order bits are used to select a particular module on the bus and the lower order bits select a memory location or I/O port within the module
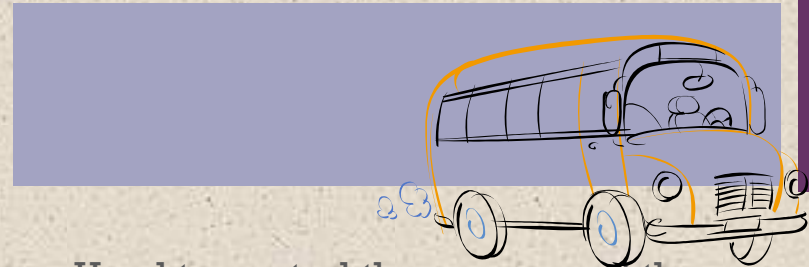
- Used to control the access and the use of the data and address lines

- Because the data and address lines are shared by all components there must be a means of controlling their use

- Control signals transmit both command and timing information among system modules

- Timing signals indicate the validity of data and address information
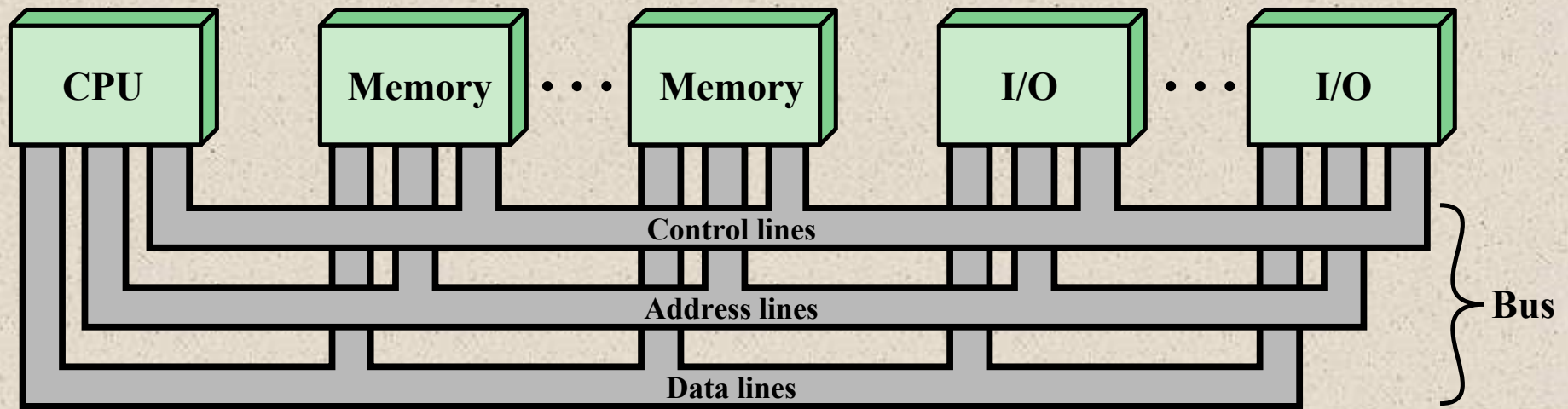
- Command signals specify operations to be performed

**Figure 3.16  Bus Interconnection Scheme**

+ # Summary

## Chapter 3

A Top-Level View of Computer Function and Interconnection

- Computer components
- Computer function
  - Instruction fetch and execute
  - Interrupts
  - I/O function
- Interconnection structures
- Bus interconnection