# **LAB 12**

**EXPOSURE OF DIFFERENT FLIP FLOPS**

##### EQUIPMENT: -

1. IC 7400, IC 7404, IC 7476.

2. NI Multisim

##### THEORY: -

SR flip-flop is al o called Synchronous flip-flop. That means that this flip-flop is concerned with time. Digital circuits can have a concept of time using a clock signal. The clock signal simply goes from low-to-high and

high-to-low in a short period of time.

|  |  |  |  |
| --- | --- | --- | --- |
| **C** | **S** | **R** | **Next Stage of Q** |
| 0 | x | x | No change |
| 1 | 0 | 0 | No change |
| 1 | 0 | 1 | Q = 0; Reset state |
| 1 | 1 | 0 | Q = 1; Set State |
| 1 | 1 | 1 | Indeterminate |

Figure 1: SR Flip Flop and its truth table

In case of D flip-flop, The Q output always takes on the state of the D input at the moment of a rising clock edge. (Or falling edge if the clock input is active low). It is called the D flip-flop for this reason, since the

output takes t e value of the D input or Data in ut, and Delays it by one clock counth. The D flip-flop can be interpreted as a primitive memory cell, zero-order hold, or delay line.

Figure 1: D Flip Flop and its truth table

|  |  |  |
| --- | --- | --- |
| **C** | **D** | **Next Stage of Q** |
| 0 | x | No change |
| 1 | 0 | Q = 0; Reset state |
| 0 | 1 | Q = 1; Set State |

84

In case of T flip-flop, if the T input is high, the T flip-flop changes state ("toggles") whenever the clock input is strobe. If the T input is low, the flip-flop holds the previous value. The truth table is as follows:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Characteristics Table** | | | | **Excitation Ta ble** | | | |
| **T** | **Q** | **Qnext** | **Comment** | **Q** | **Qnext** | **T** | **comment** |
| 0 | 0 | 0 | Hold on state (no clock) | 0 | 0 | 0 | No change |
| 0 | 1 | 1 | Hold on state (no clock) | 1 | 1 | 0 | No change |
| 1 | 0 | 1 | toggle | 0 | 1 | 1 | Complement |
| 1 | 1 | 0 | toggle | 1 | 0 | 1 | Complement |

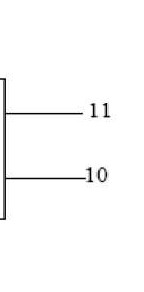
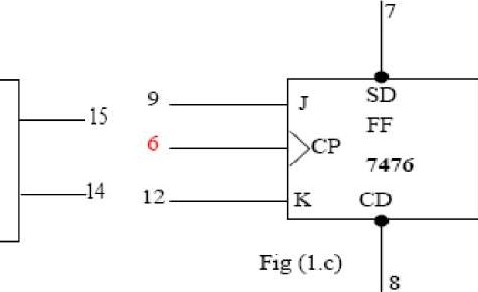
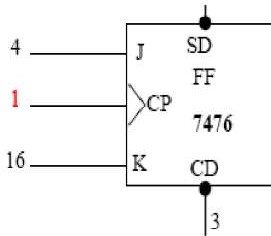
The JK flip-flop augments the behavior of the SR flip-flop (J=Set, K=Reset) by interpreting the S = R = 1 condition as a "flip" or toggle command. Specifically, the combination J = 1, K = 0 is a command to set the flip-flop; the combination

J = 0, K = 1 is a command to reset the flip-flop; and the combination J = K = 1 is

a command to complement of it

toggle the flip-flop, i.e., change its output to the logical current s value.

Figure: IC 7476 M/S JK flip-flop



86



|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **SD**  **Preset** | **SD**  **Clear** | **Clock** | **J** | **K** | **OUTPUST** | |
| **Q** | 𝐐¯ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H\* | H\* |
| H | H | ↓ | L | L | QO | ¯QO |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | TOGGLE | |
| H | H | H | X | X | QO | ¯QO |

Figure: Truth table for JK flip-flop (IC 7476)

**PROCEDURE:**

###### Make connections as shown in the diagrams.

* + Verify the truth tables for various combinations of inputs.

**QUESTIONS:**

1. What is the difference between Flip-Flop and latch?
2. What is the difference between synchronous and asynchronous inputs?
3. What are the applications of different Flip-Flops?
4. What is the difference of Edge triggering over level triggering?