

## Counters

- Based on clk signal, sequential ckt are classified as :-

↳ asynchronous sequential ckt

↳ synchronous sequential ckt

Asynchronous sequential ckt:-

External clock is not common in all the flip-flops.

Synchronous sequential ckt:- External clock is

common in all flip-flops.

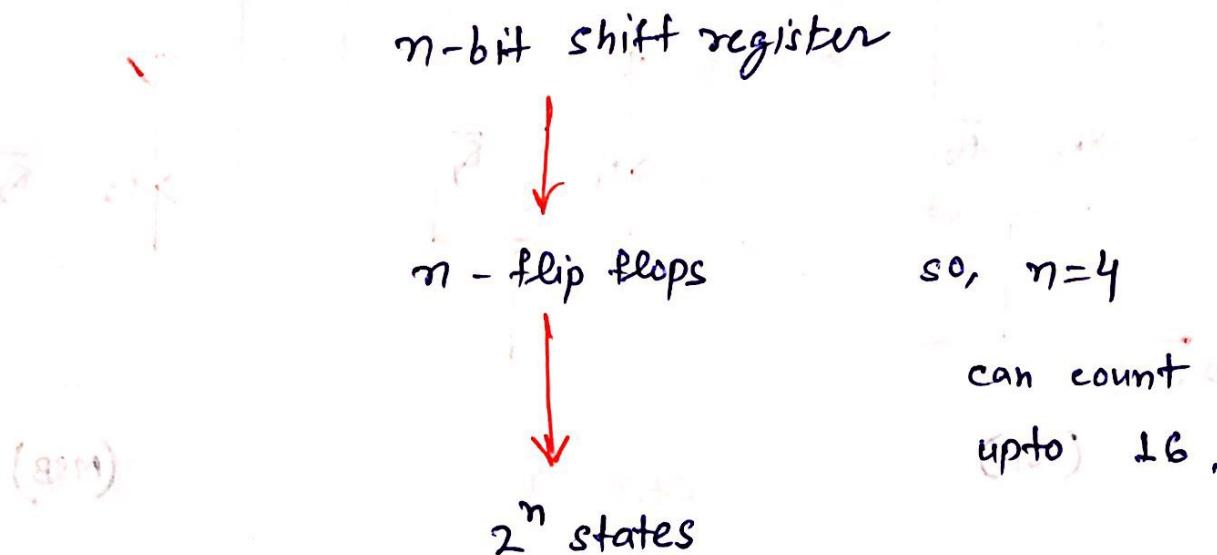
Having common clk signal to all the flip-flop give chance to change their value simultaneously.

while in asynchronous, there is no common clk signal due to which they <sup>(flip-flop)</sup> can't operate simultaneously.

Synchronous seq ckt → Fast

Asynchronous seq ckt → Slow

Counter is a special arrangement of combinational logic with register which makes it to count clock pulses.



### Types of counters

Asynchronous counter

Synchronous counter

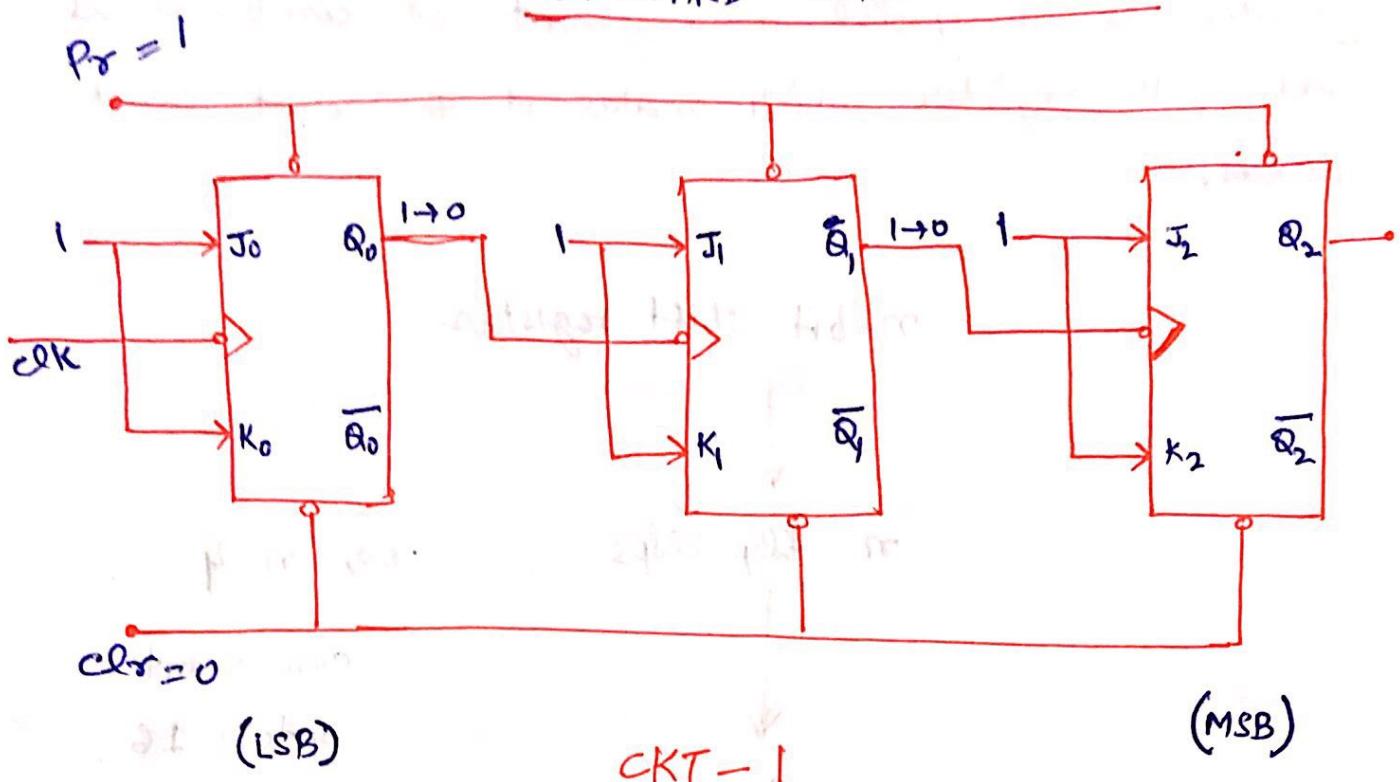
#### i) 3-bit Asynchronous counter :-

It contains 3 flip flops. ( $FF_0, FF_1, FF_2$ )

The o/p of first flip flop will be IIP  $\Leftrightarrow$  clk signal to next flip flop.

$Pr$  &  $Clr$  are shorted.  $Pr=0$  and  $Clr=1$  to make  $(Q_0, Q_1, Q_2 = 0)$ .

## STANDARD ASYNC COUNTER

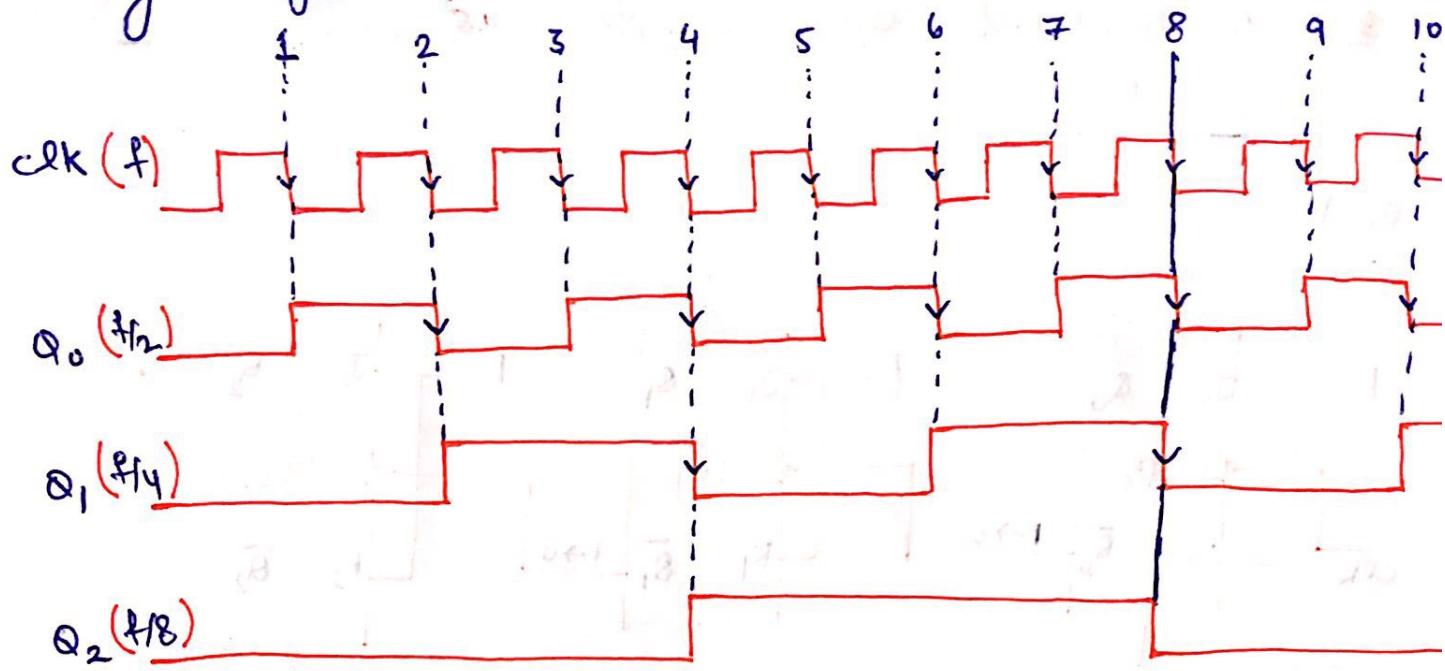


- All flip-flop work as T-ff. } standard Async.
- $O/P(FF_{i-1}) \rightarrow clk(FF_i)$  } counter

Mod 8 upcounter

clk	$Q_2$	$Q_1$	$Q_0$
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

## Timing Diagram :-



Q: If the clock Time period is  $T_c$ , then what is the freq. of  $Q_0, Q_1, Q_2$ .

$$f_c = \frac{1}{T_c} \quad \text{and } f_{Q_0} = \left(\frac{f_c}{2}\right)$$

$$f_{Q_1} = \frac{f_{Q_0}}{2} = \left(\frac{f_c}{4}\right)$$

$$f_{Q_2} = \frac{f_{Q_1}}{2} = \left(\frac{f_c}{8}\right)$$

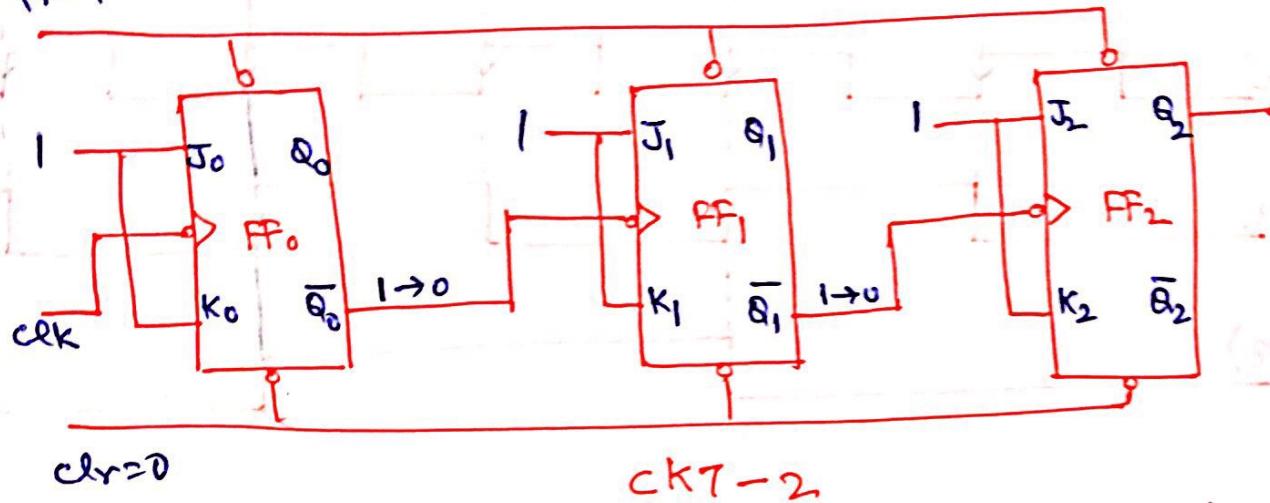
Q: If the propagation delay of each ff is  $T_{pd}$ , what is the maximum  $f_{\text{clk}}$  possible to apply in the standard Async Counter ckt.

$$f_{c \max} = \frac{1}{n T_{pd}}$$

NOTE:-

A standard async counter is named as Ripple counter.

$P_r=1$



$clr=0$

CKT-2

clk Pulse  $1 \rightarrow 0 \rightarrow$  FF<sub>0</sub> active

Q<sub>0</sub> 0 → 1 → FF<sub>1</sub> active

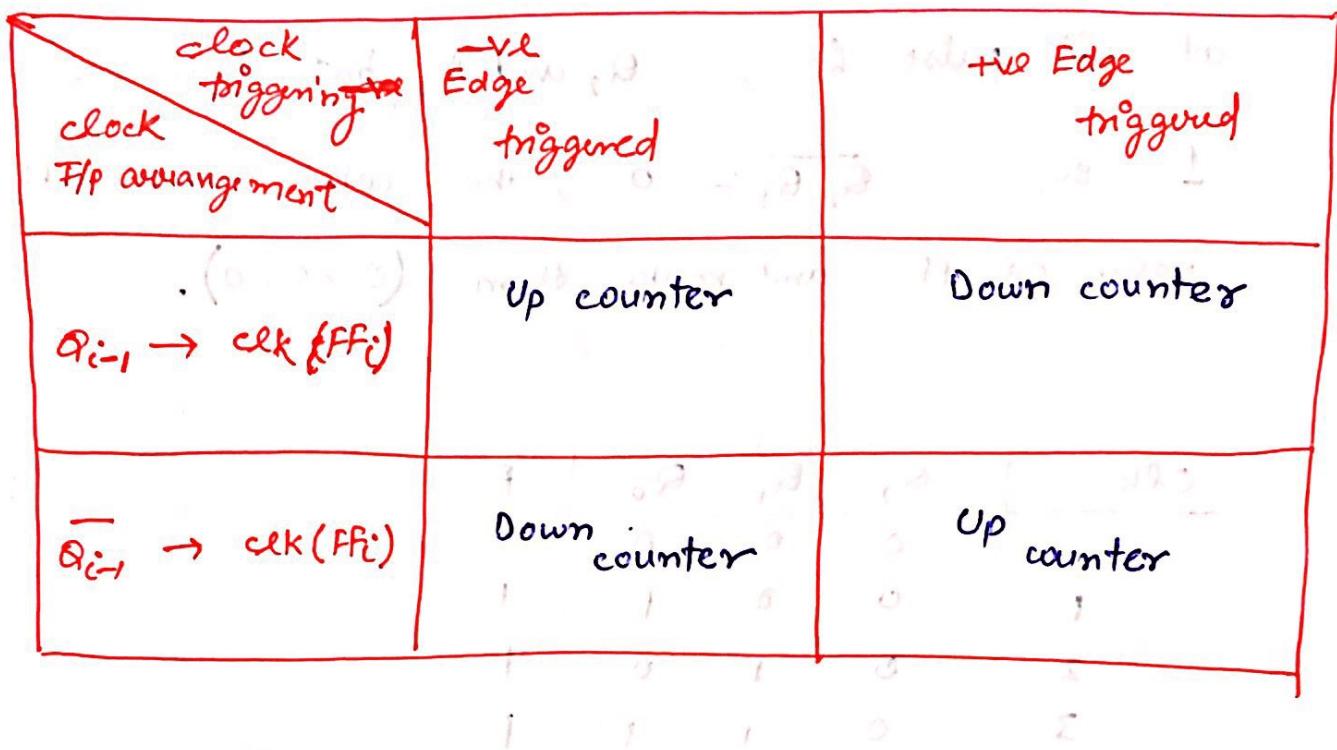
Q<sub>1</sub> 0 → 1 → FF<sub>2</sub> active

Mod 8 down counter

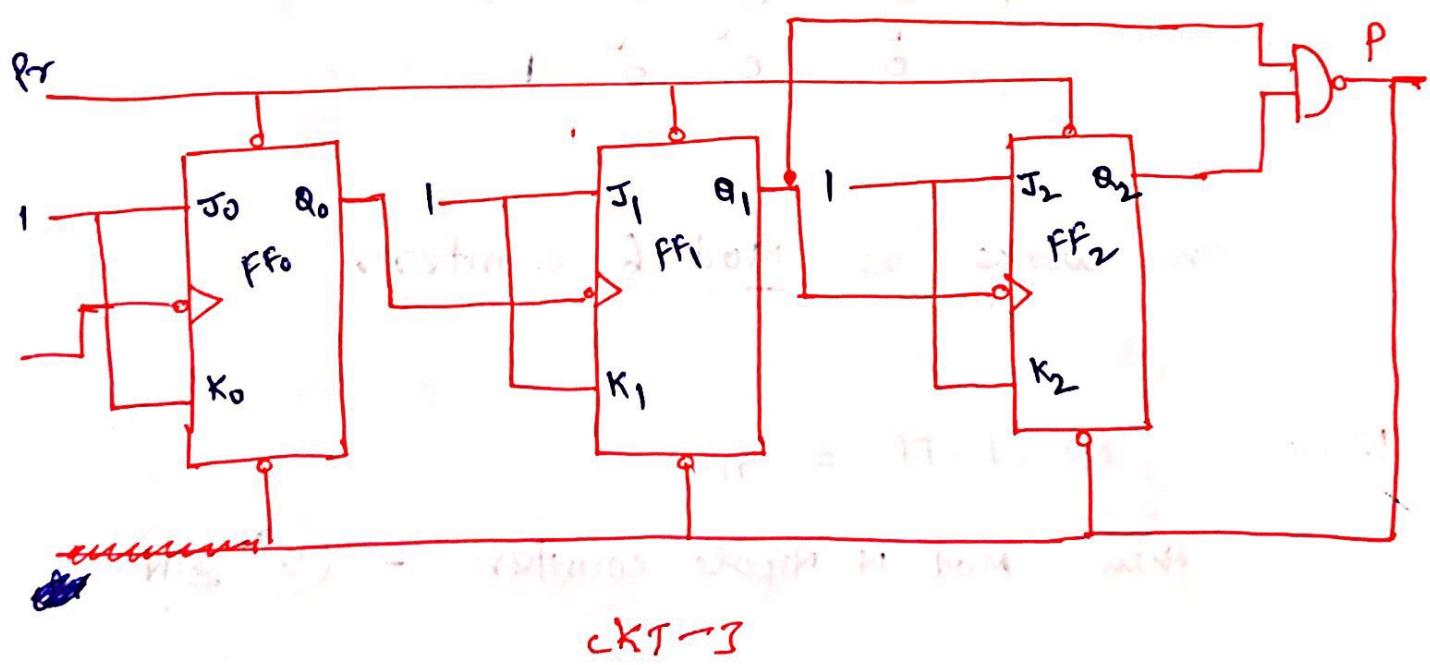
clk	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
1	0	0	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1
8	0	0	0

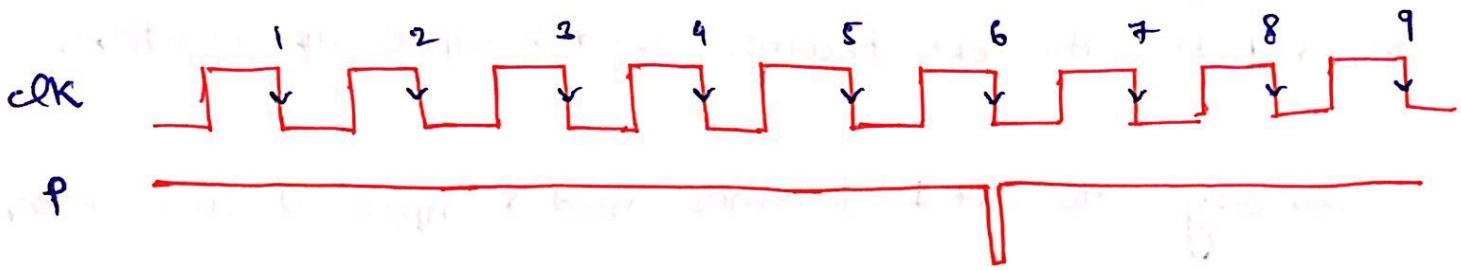
Counting sequence: 1, 2, 3, 4, 5, 6, 7, 8. The sequence is shown with arrows indicating the transition from one state to the next. The states are represented as (Q<sub>2</sub>, Q<sub>1</sub>, Q<sub>0</sub>).

- In ckt 2 while replace all the FF with the edge triggered FF the ckt becomes mod 8 ripple up counter.
- Similarly the ckt 1 becomes mod 8 ripple down counter.



Q. Draw the wave form to the O/P of the NAND gate P.





at  $\text{clk}$  pulse 6,  $Q_2$  and  $Q_1$  both becomes 1 so,  $\overline{Q_2 \cdot Q_1} = 0$ , this will clear all value of FF and make them  $(0, 0, 0)$ .

<u>clk</u>	$Q_2$	$Q_1$	$Q_0$	<u>P</u>
	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	0	1	0	0
	0	0	0	1

] fraction of time-pulse

This works as Mod 6 counter.

NOTE:- No. of FF =  $n$

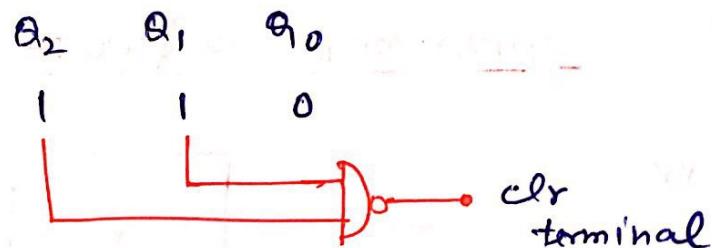
then Mod N Ripple counter -  $(2^n \geq N)$

NOTE:- To realize ( $\text{Mod } N$  where  $2^n > N$ ) ripple counter, take the input of FF to the NAND gate which has value 1 at  $N^{\text{th}}$  clock pulse, And the Op of NAND gates is connected to clear terminals of each FF.

eg:- for Mod 6 -

$$2^n > 6 \quad \text{so, } n = 3$$

Now at  $\text{clk} = 6$

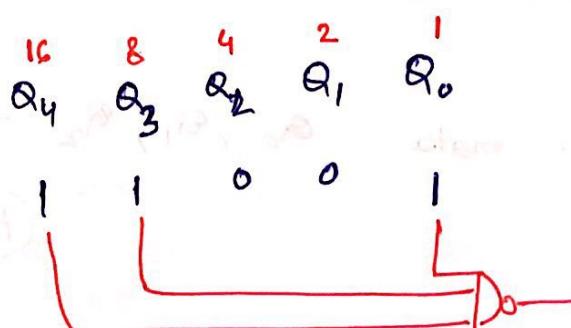


$$\text{so, clr terminal of each FF} = \overline{Q_2 \cdot Q_1}$$

eg:- for Mod 25 -

$$2^n > 25 \quad \text{so, } n = 5$$

Now at  $\text{clk} = 25$

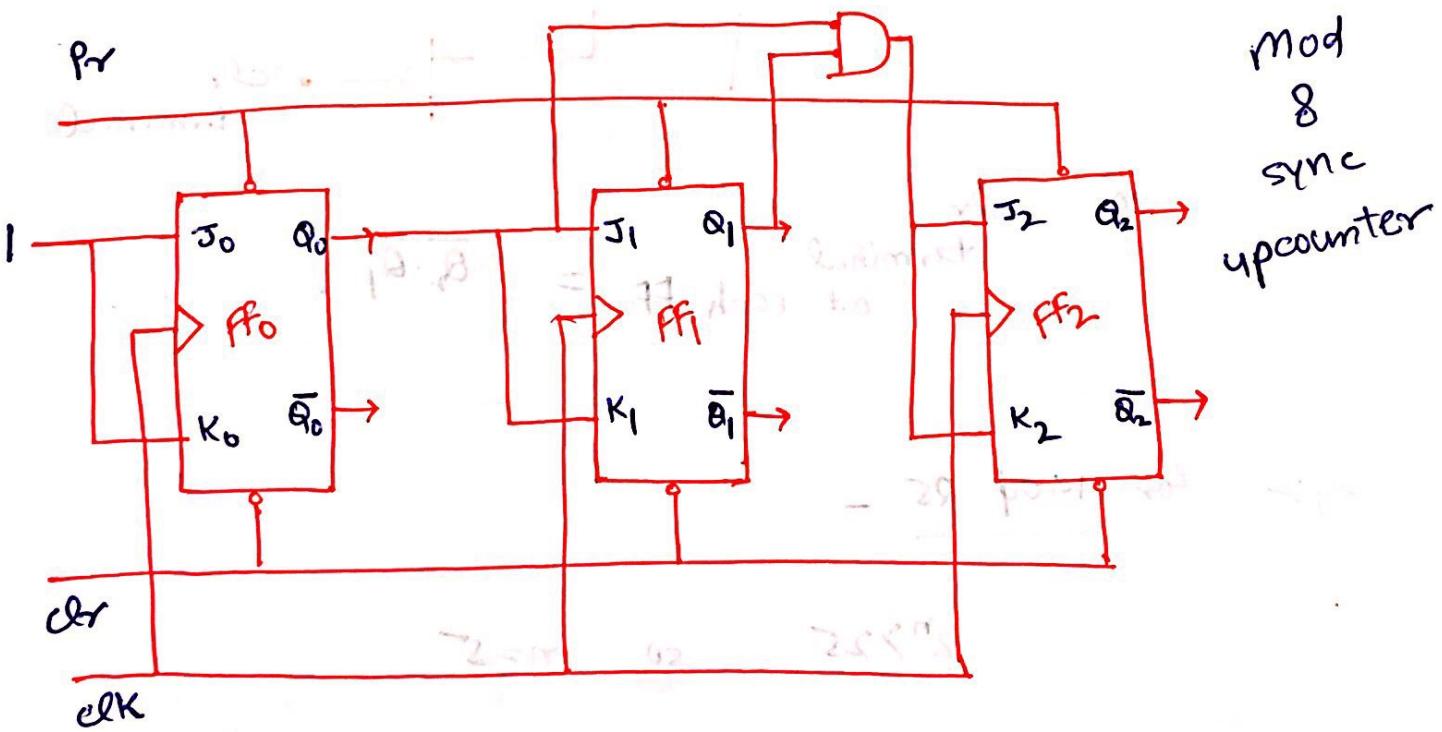


$$\text{clr} = \overline{Q_4 \cdot Q_3 \cdot Q_2}$$

Q. In the figt 3, the propagation delay of each FF is  $T_F$  and propagation delay of NAND gate is  $T_N$ . What is the maximum clock frequency possible to apply to counter circuit.

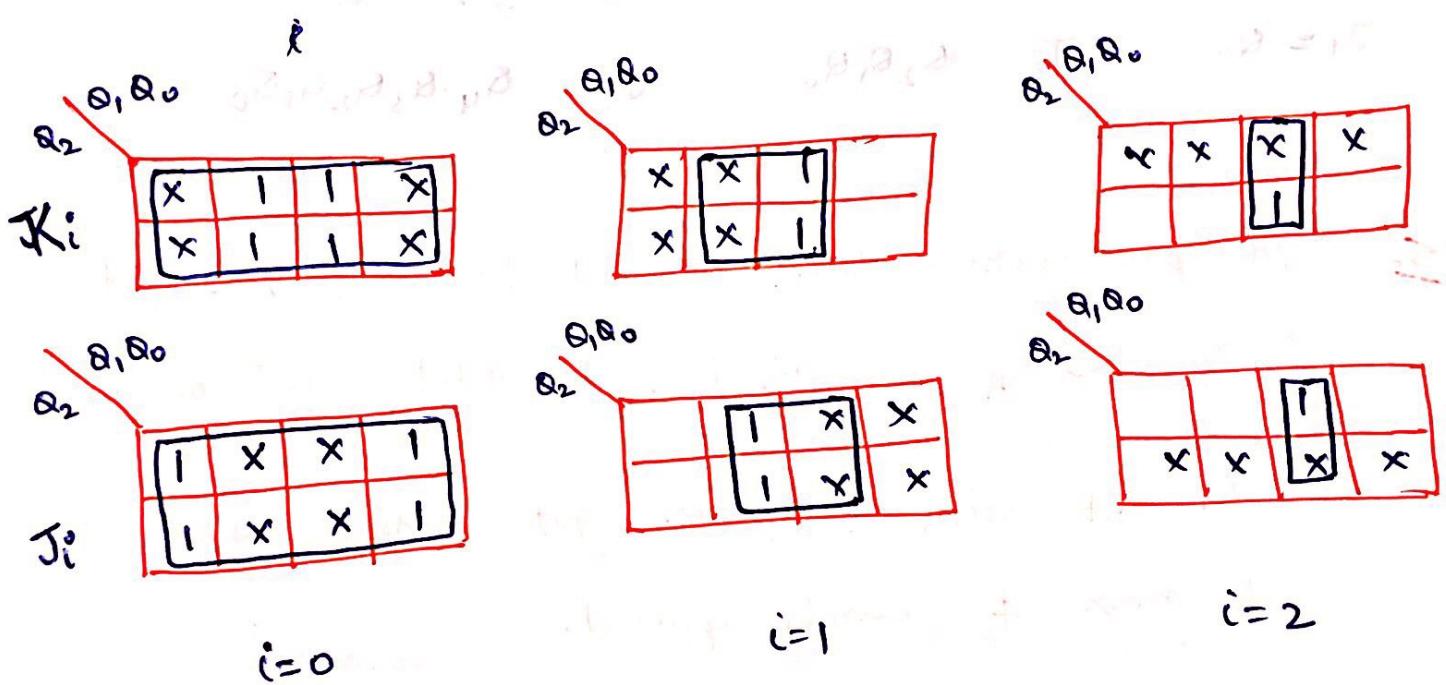
$$f_c = \frac{1}{3T_F + T_N}$$

### (ii) Synchronous counter :-



for make  $Q_0, Q_1, Q_2 \rightarrow (0, 0, 0, 0)$  make  
 $(P_r = 1 \text{ and } C_{lr} = 0)$

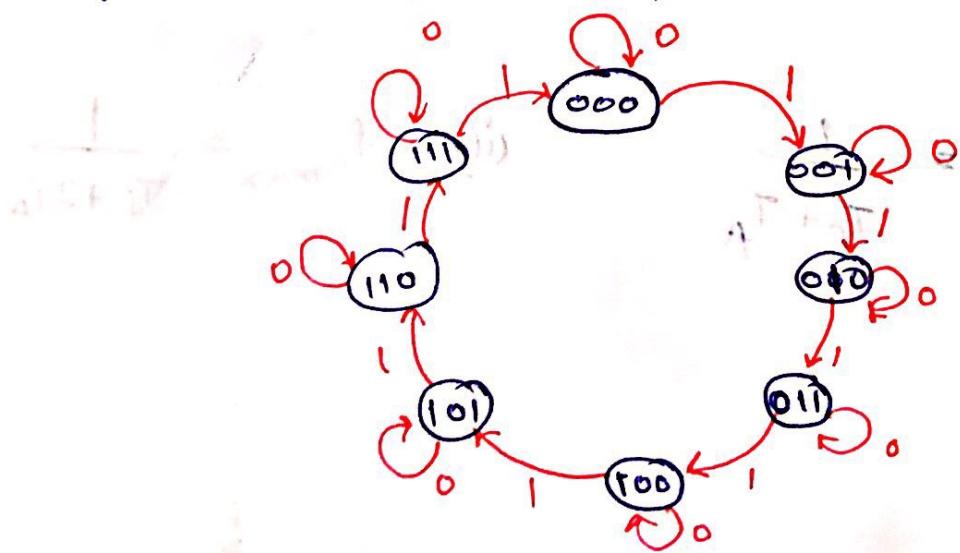
$clk$	$Q_2$	$Q_1$	$Q_0$	$J_0$	$K_0$	$J_1$	$K_1$	$J_2$	$K_2$
1	0	0	0	1	x	0	x	0	x
2	0	0	1	x	1	1	x	0	x
3	0	1	0	1	x	x	0	0	x
4	0	1	1	x	1	x	0	x	0
5	1	0	0	1	x	1	x	x	0
6	1	0	1	x	1	x	0	x	0
7	1	1	1	x	1	x	1	x	1
8	0	0	0	0	0	0	0	0	0



$$\begin{cases} J_0 = 1 \\ K_0 = 1 \end{cases}$$

$$\begin{cases} J_1 = Q_0 \\ K_1 = Q_0 \end{cases}$$

$$\begin{cases} J_2 = Q_1, Q_0 \\ K_2 = Q_1, Q_0 \end{cases}$$



STATE  
DIAGRAM

NOTE :- If we replace the FF with -ve edge triggered FF, there will not be any change in the behaviour of counter.

for N-bit counter :-

$$J_{n-1} = Q_{n-2} \cdot Q_{n-3} \cdot \dots \cdot Q_0 \cdot 1$$

$$J_0 = 1, \quad J_2 = Q_1 Q_0, \quad J_4 = Q_3 Q_2 Q_1 Q_0$$

$$J_1 = Q_0, \quad J_3 = Q_2 Q_1 Q_0, \quad J_5 = Q_4 \cdot Q_3 Q_2 Q_1 Q_0$$

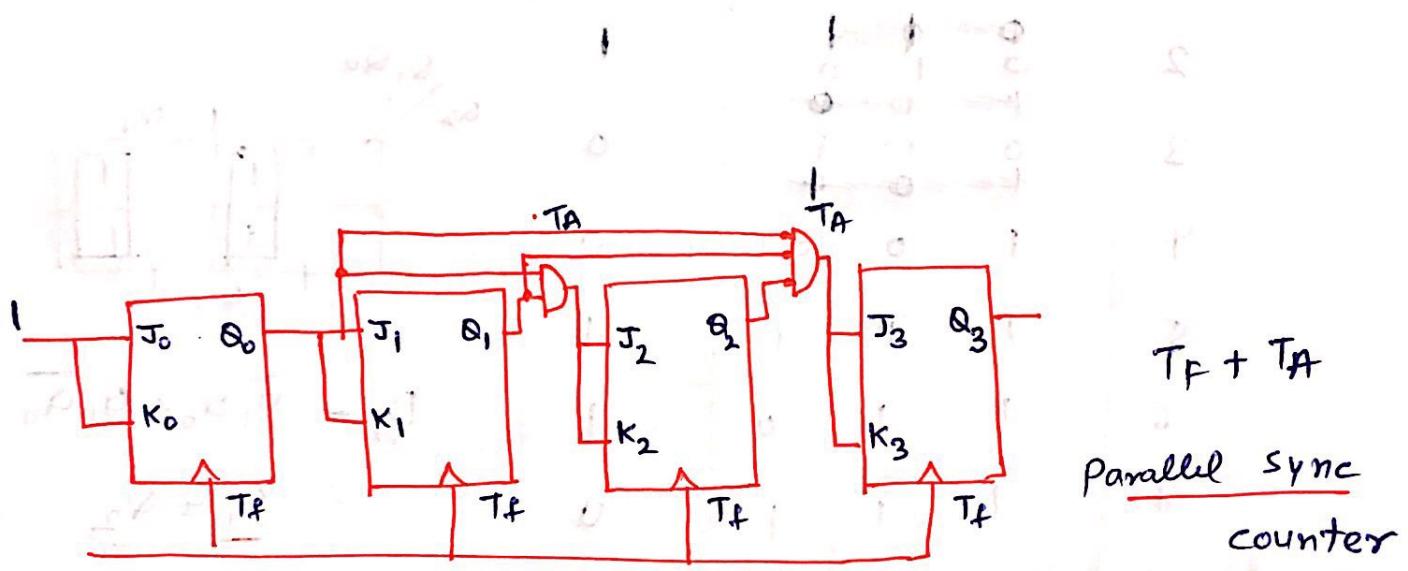
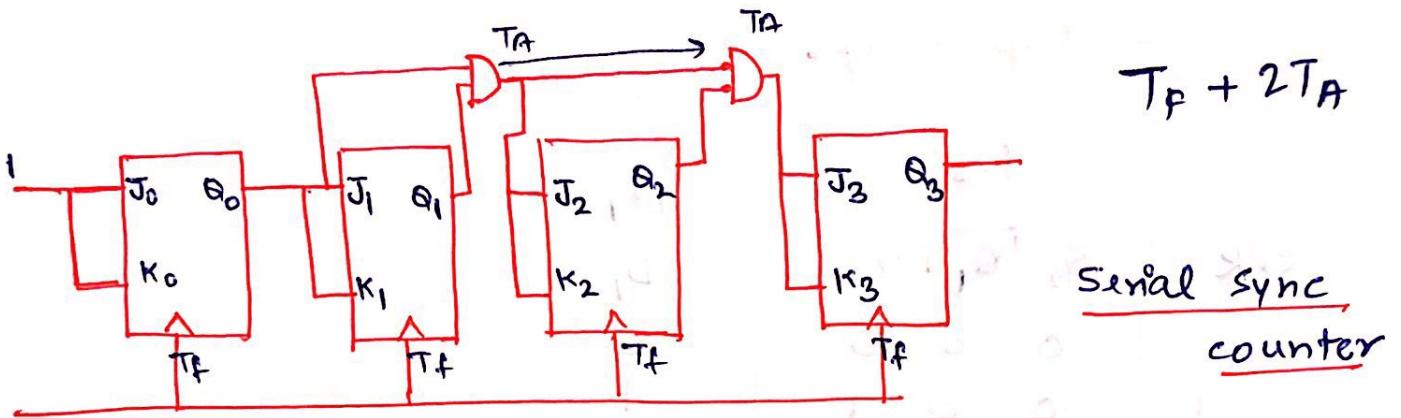
Q. The propagation delay of each FF and AND gate is  $T_f$  and  $T_A$  respectively. A 4-bit sync counter

(i) In ckt with 2-I/p AND gate is used, what is the max  $f_c$  can be applied.

(ii) If ckt with n-I/p AND gate is used, what is the max  $f_c$  can be applied.

$$(i) f_{c\max} = \frac{1}{T_f + T_A}$$

$$(ii) f_{c\max} = \frac{1}{T_f + 2T_A}$$

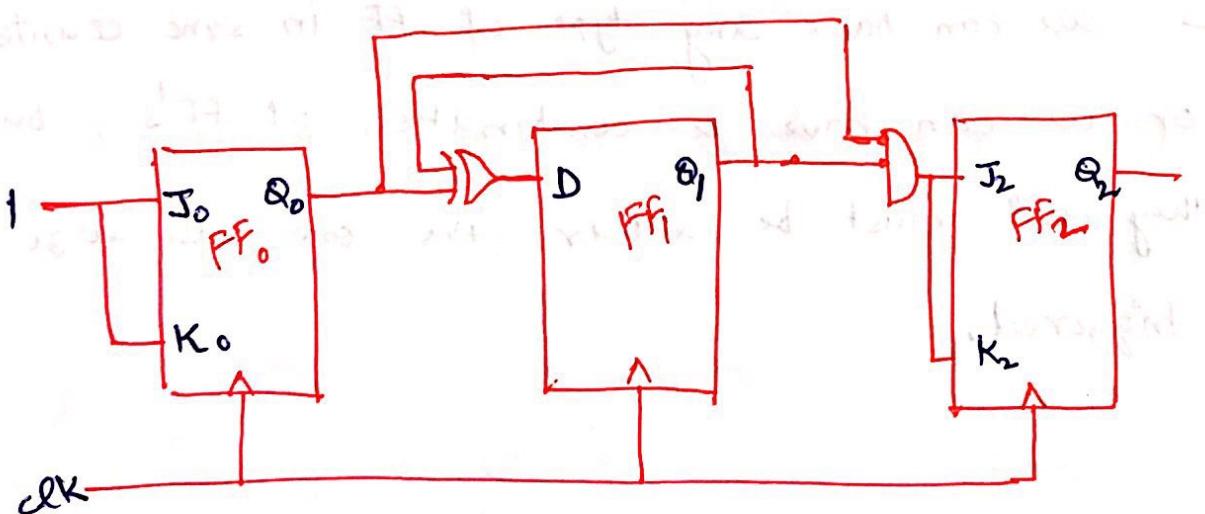


NOTE:- We can have any type of FF in sync counter,  
or we can have a combination of FF's, but  
they all must be either +ve or -ve edge  
triggered.

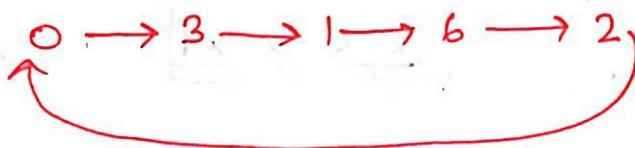
Q. In clk of 3-bit sync counter, if  $\overline{P\&S}$  is to be replaced with D-FF. what is the I/p to D flip-flop.

P-S			FF <sub>1</sub>
clk	Q <sub>2</sub>	Q <sub>1</sub>	D <sub>1</sub>
	0	0	0
1	0	0	1
2	0	1	1
3	0	1	0
4	1	0	0
5	1	0	1
6	1	1	1
7	1	1	0
8	0	0	0

$D_1 = \overline{Q_1}Q_0 + Q_1\overline{Q_0}$   
 $= Q_1 \oplus Q_0$



Q. In sync. counter <sup>for</sup> with the following sequence  
using :



MOD 5  
counter

(a) M/S JK Flip flop

(b) D flip flop

(c) T flip flop.

As we have 6 as the highest state, so we need  $2^n \geq 6$ , ( $n=3$ )

So, we need 3 FF's.

As, 4, 5 and 7 are unused combination so they will be don't care for all the FF's.

m	P.S $Q_2 Q_1 Q_0$	N.S $Q_2 Q_1 Q_0$	$J_0$	$K_0$	$J_1$	$K_1$	$J_2$	$K_2$
0	0 0 0	0 1 1	1	x	1	x	0	x
1	0 0 1	1 1 0	x	1	1	x	1	x
2	0 1 0	0 0 0	0	x	x	1	0	x
3	0 1 1	0 0 1	x	0	x	1	0	x
4	1 0 0	—	x	x	x	x	x	x
5	1 0 1	—	x	x	x	x	x	x
6	1 1 0	0 1 0	0	x	x	0	x	1
7	1 1 1	—	x	x	x	x	x	x

$Q_2$	$Q_1, Q_0$						
	<table border="1"> <tr> <td>1</td><td>X</td><td>X</td></tr> <tr> <td>X</td><td>X</td><td>X</td></tr> </table>	1	X	X	X	X	X
1	X	X					
X	X	X					

$$J_0 = \bar{Q}_1$$

$Q_2$	$Q_1, Q_0$								
	<table border="1"> <tr> <td>1</td><td>1</td><td>X</td><td>X</td></tr> <tr> <td>X</td><td>X</td><td>X</td><td>X</td></tr> </table>	1	1	X	X	X	X	X	X
1	1	X	X						
X	X	X	X						

$$J_1 = 1$$

$Q_2$	$Q_1, Q_0$								
	<table border="1"> <tr> <td></td><td>1</td><td></td><td></td></tr> <tr> <td>X</td><td>X</td><td>X</td><td>X</td></tr> </table>		1			X	X	X	X
	1								
X	X	X	X						

$$J_2 = \bar{Q}_1 Q_0$$

$Q_2$	$Q_1, Q_0$								
	<table border="1"> <tr> <td>X</td><td>1</td><td></td><td>X</td></tr> <tr> <td>X</td><td>X</td><td>X</td><td>X</td></tr> </table>	X	1		X	X	X	X	X
X	1		X						
X	X	X	X						

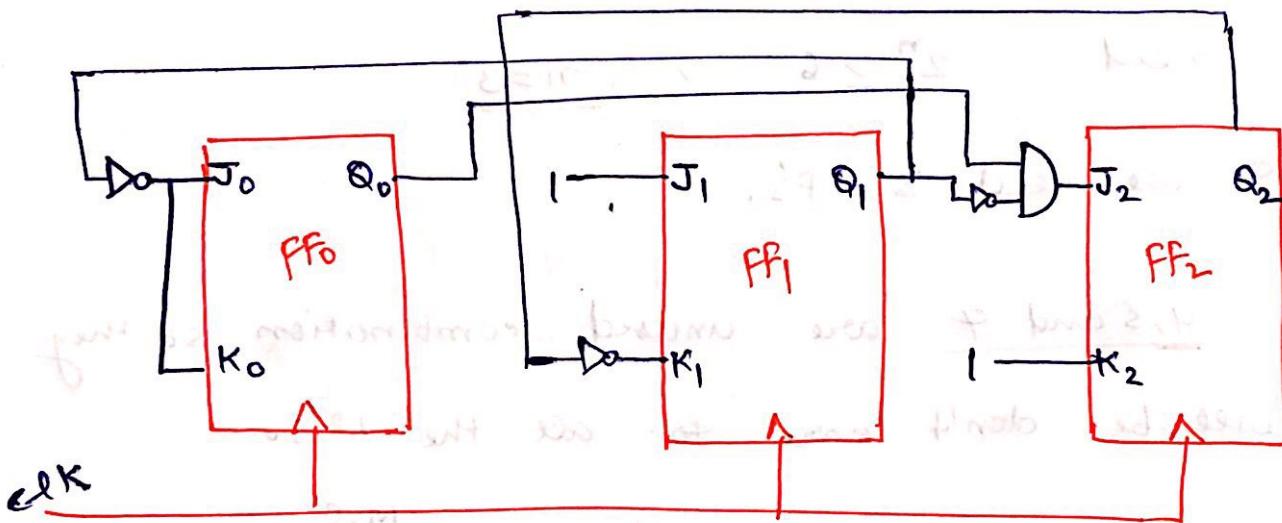
$$K_0 = \bar{Q}_1$$

$Q_2$	$Q_1, Q_0$								
	<table border="1"> <tr> <td>X</td><td>X</td><td>1</td><td>1</td></tr> <tr> <td>X</td><td>X</td><td>X</td><td>X</td></tr> </table>	X	X	1	1	X	X	X	X
X	X	1	1						
X	X	X	X						

$$K_1 = \bar{Q}_2$$

$Q_2$	$Q_1, Q_0$								
	<table border="1"> <tr> <td>X</td><td>X</td><td>X</td><td>X</td></tr> <tr> <td>X</td><td>X</td><td>X</td><td>1</td></tr> </table>	X	X	X	X	X	X	X	1
X	X	X	X						
X	X	X	1						

$$K_2 = 1$$



(a) A counter circuit is shown, what is mod value of the given counter.

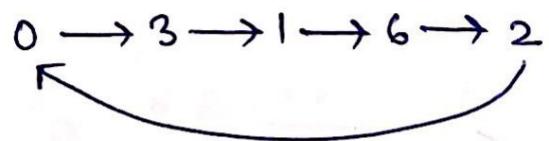
(b) If P.S of counter is 001, what is state after 3 clock pulse.

(c) If P.S of counter is 110, what is state after 48 clock pulse.

(a) clk

	$Q_2\ Q_1\ Q_0$	$FF_2$	$FF_1$	$FF_0$
		$J_2 = K_2$	$J_1 = K_1$	$J_0 = K_0$
	0 0 0	0 1	1 1	1 1
1	0 1 1	0 1	1 1	0 0
2	0 0 1	1 1	1 1	1 1
3	1 1 0	0 1	1 0	0 0
4	0 1 0	0 1	1 1	0 0
5	0 0 0			

MOD 5 counter :



(b) 000 (0)

(c) 0 1 1 (3)

NOTE:-

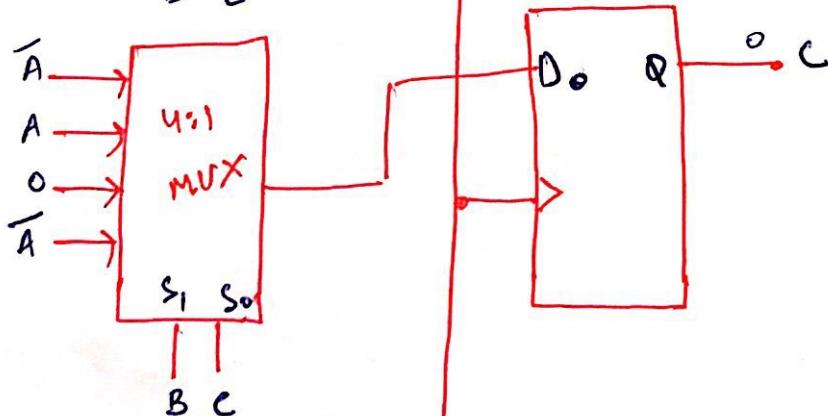
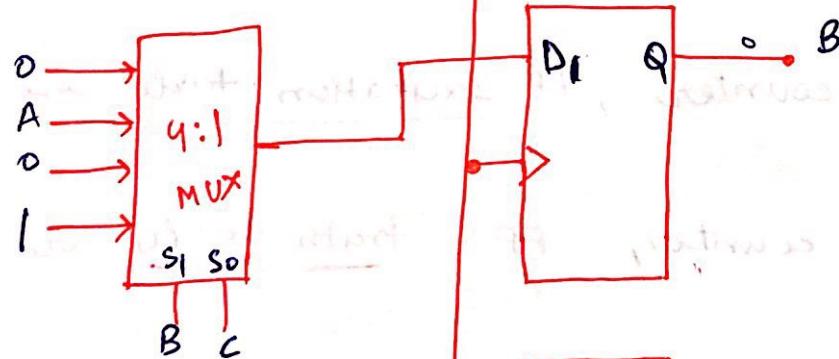
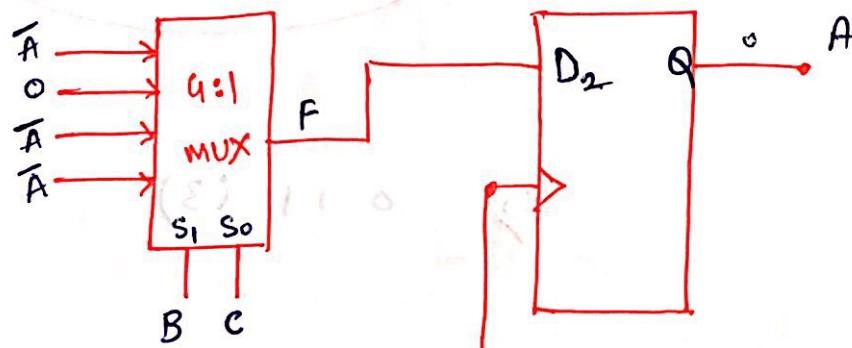
- To design the sync counter, FF excitation table are used,
- To analyze sync counter, FF truth tables are used.

Q. A Finite state machine is switching in following sequence -

ABC

$000 \rightarrow 101 \rightarrow 011 \rightarrow 111 \rightarrow 010 \rightarrow 100$

One of the possible D-FF implementation is shown below, identify what I/P need to applied to each one of 4:1 MUX.

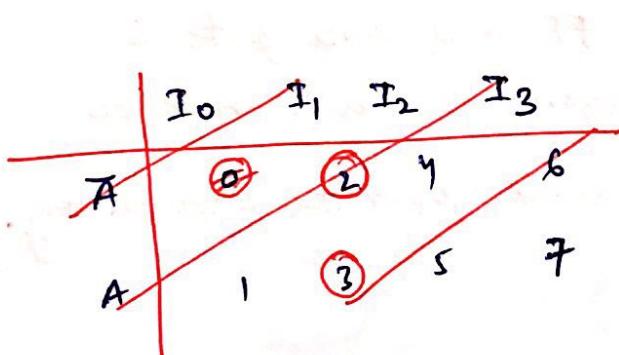


P.S A B C	N.S A B C	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0 0 0	1 0 1	1	0	1
0 0 1		x	x	x
0 1 0	1 0 0	1	0	0
0 1 1	1 1 1	1	1	1
1 0 0	0 0 0	0	0	0
1 0 1	0 1 1	0	1	1
1 1 0		x	x	x
1 1 1	0 1 0	0	1	0

$$D_2 = \Sigma m(0, 2, 3)$$

$$D_0 = \Phi \Sigma m(0, 3, 5)$$

$$D_1 = \Sigma m(3, 5, 7)$$

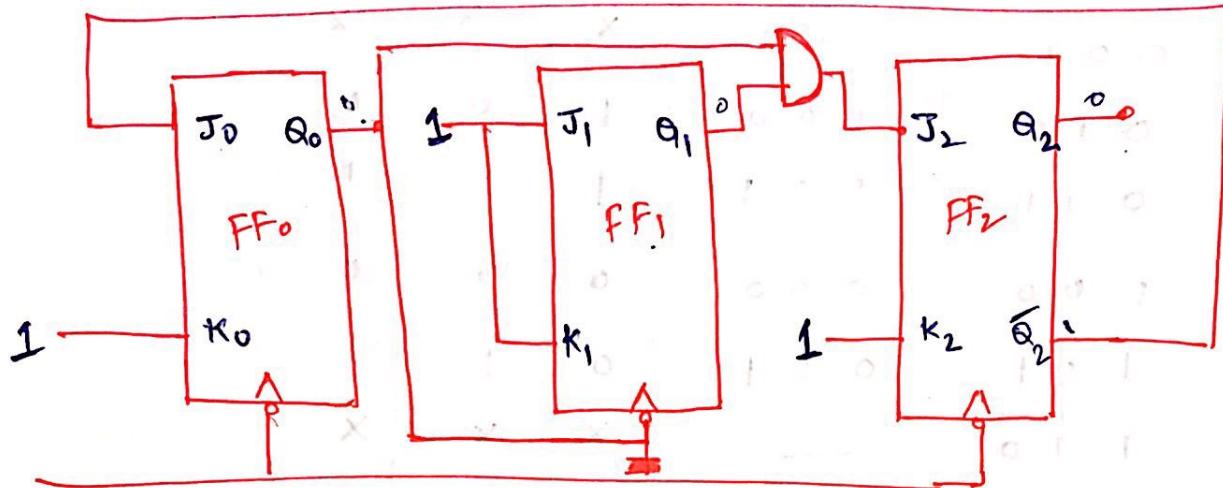


	I <sub>0</sub> $\bar{B}\bar{C}$	I <sub>1</sub> $\bar{B}C$	I <sub>2</sub> $B\bar{C}$	I <sub>3</sub> $BC$
$\bar{A}$	0	1	2	3
A	4	5	6	7
	$\bar{A}$	0	$\bar{A}$	$\bar{A}$

D <sub>1</sub>	I <sub>0</sub>	I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>
$\bar{A}$	0	1	2	3
A	4	5	6	7

D <sub>0</sub>	I <sub>0</sub>	I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>
$\bar{A}$	0	1	2	3
A	4	5	6	7

Q. what is the  $(a)_{mod}$  value of the given counter:



(b) if counter is entering in any one of the unusual state. check whether it is Lock-in or Lock-out.

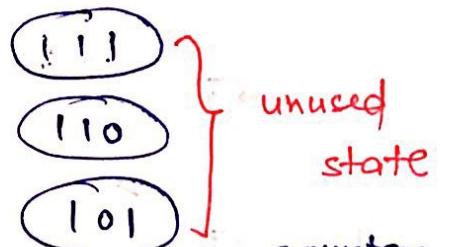
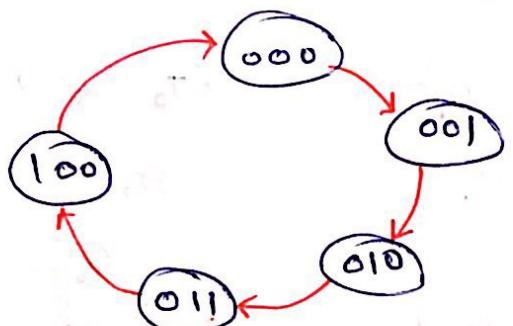
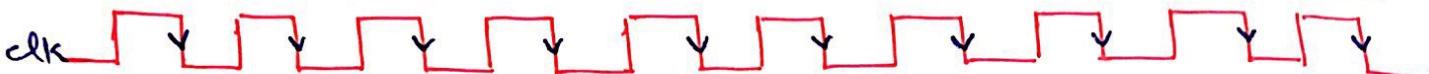
(c)

The propagation delay of FF and AND gate is  $T_F$  &  $T_A$ . what is the maximum clock rate to apply, so that counter will operate satisfactorily.

clk	$Q_2$	$Q_1$	$Q_0$
1	0	0	0
2	0	1	0
3	0	1	1
4	1	0	0

so, MOD 5 counter

5	1	0	0	0
---	---	---	---	---



counter  
is  
lock out  
state

NOTE:- while applying the clk signal, if the counter is coming from unused state to one of the used state then the counter is said to be in "Lock-in" other wise counter is "Lock-out".



LOCK-IN



LOCK-IN



LOCK-IN

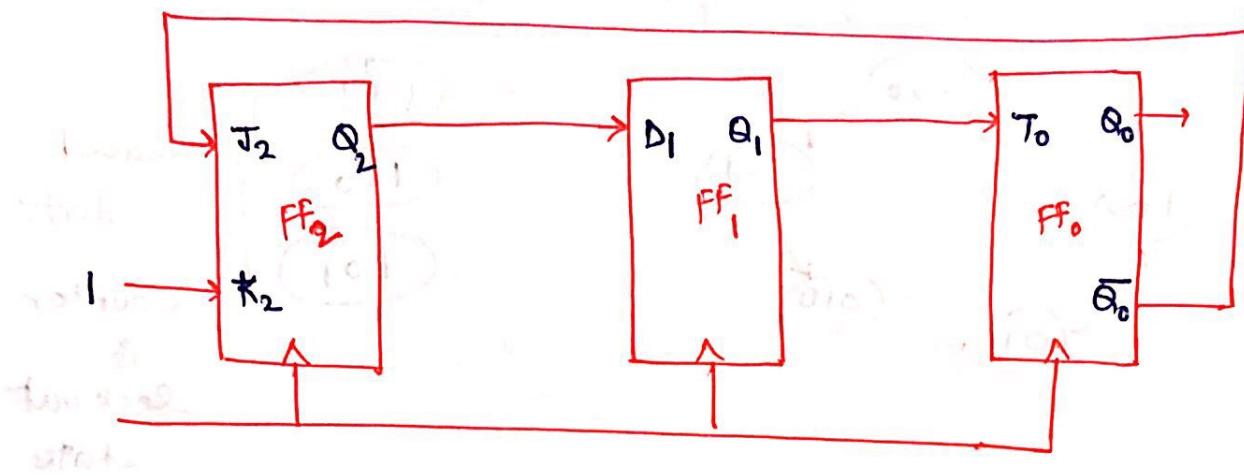
(c)

$$f_{C\max} = \frac{1}{2T_F + T_A}$$

Q.

what is the mod value of the given counter:

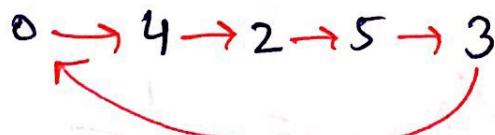
Ans: 8 + 8 + 8 = 24 bits



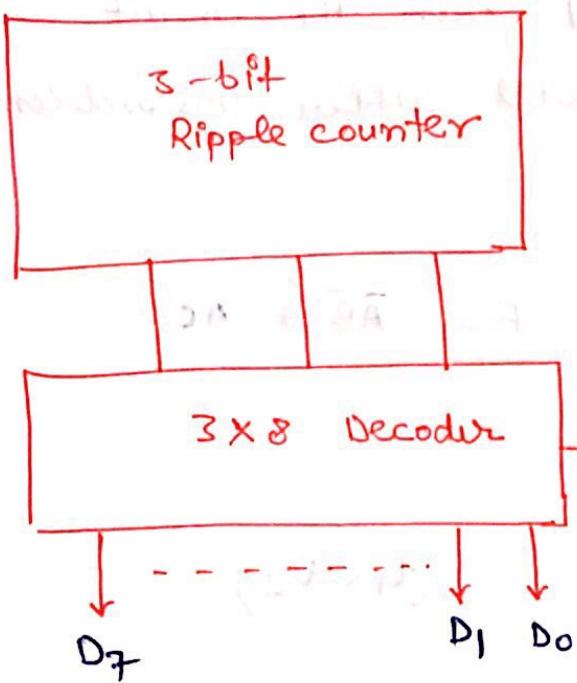
It increases just by double the bits with previous state

clk	state $Q_2\ Q_1\ Q_0$	FF <sub>2</sub> state $J_2\ \bar{Q}_0$	FF <sub>1</sub> state $K_2\ D_1\ Q_2$	FF <sub>0</sub> state $T_0\ Q_1$
0	0 0 0	1	1	0
1	1 0 0	1	1	0
2	1 0 1	1	0	1
3	1 0 1	0	1	0
4	0 1 1	0	0	1
5	0 0 0			

MOD 5



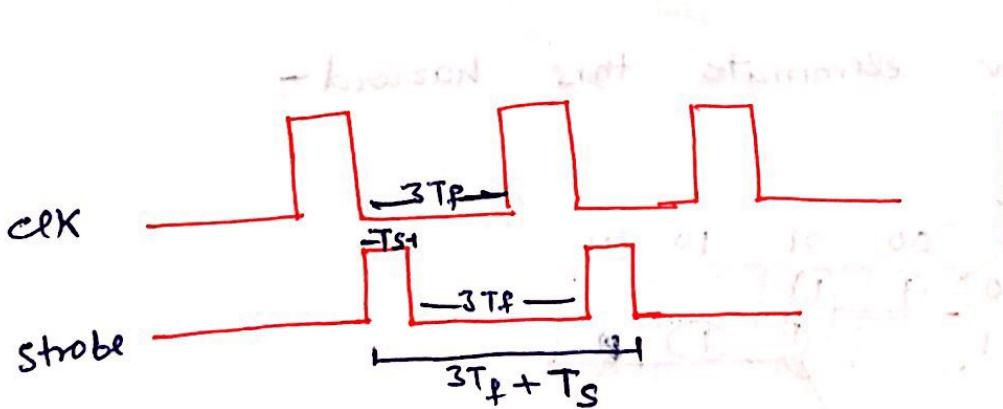
## Glitch in Ripple counter :-



clk	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	
	1	1	1	
unwanted	1	1	0	D <sub>6</sub>
010	1	0	0	D <sub>4</sub>
	1	0	0	D <sub>0</sub>

strobe

In ripple counter, after applying the clk signal before coming to steady state value the counter is switching to unwanted states. This problem in the ripple counter is named as decoding error or glitches.



T<sub>s</sub> is time period  
pulse width of  
strobe.

so, the new clock freq

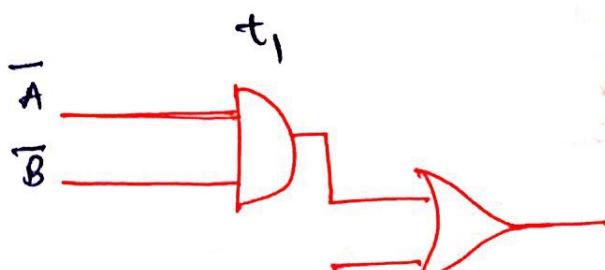
$$f_c' = \frac{1}{3T_f + T_s}$$

## Static 1 Hazard :-

In the minimal expression, taking two adjacent cell product is not covered then the circuit will suffer this problem.

A	B	C	00	01	10	11
0	0	0	1	1	0	0
1	1	1	1	0	1	0

$$F = \overline{AB} + AC$$



$$(t_1 < t_2)$$

now,

A	B	C	f
0	0	1	1
1	0	1	0 $t_1$ X
1	1	0	1 $t_2$

To remove or eliminate this hazard -

A	B	C	00	01	10	11
0	0	0	1	1	0	0
1	1	1	1	0	1	0

Add this also

$$F = \overline{AB} + AC + \overline{BC}$$