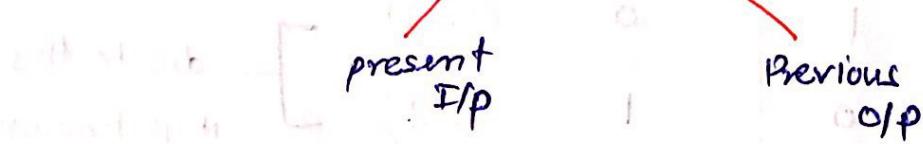


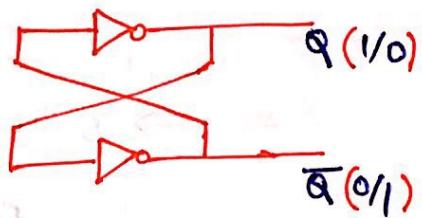
(Sequential circuit)

$$\text{Output} = f(\underbrace{x(t)}_{\text{present I/p}}, \underbrace{\text{Prev. state}}_{\text{Previous O/p}})$$



Memory Elements
(Flip-Flops)

Binary latch:-



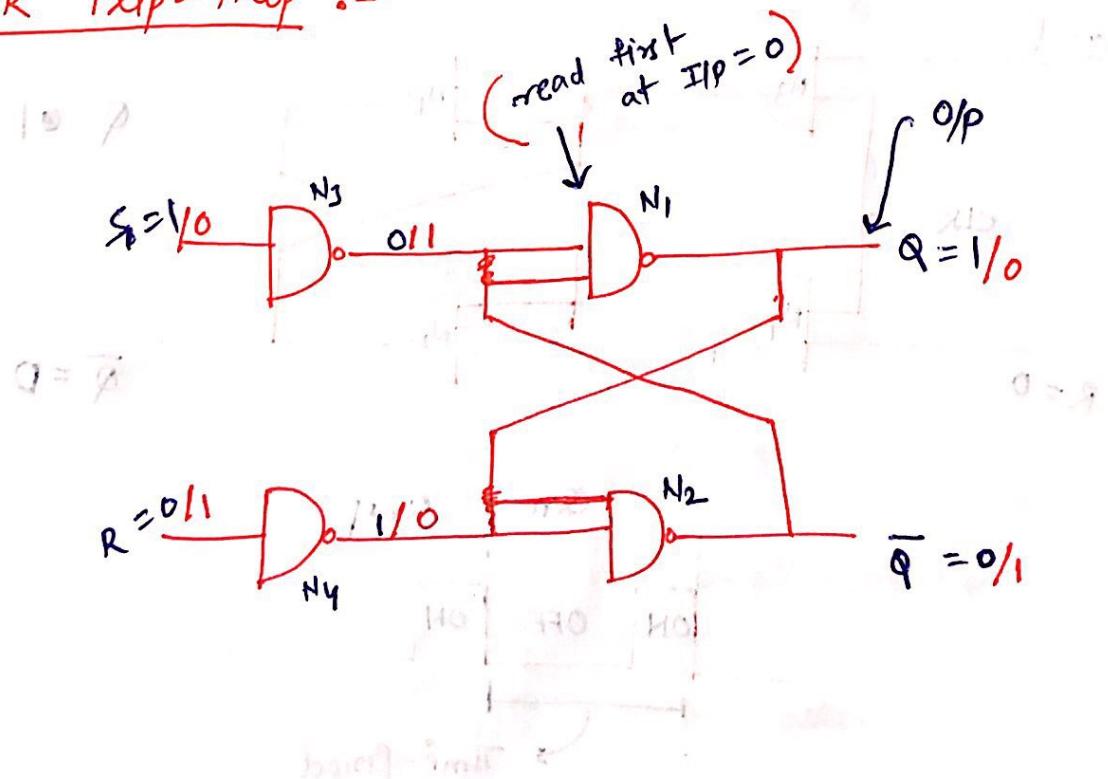
- S-R FF
- J-K FF
- D FF
- T FF

* If has no user inputs

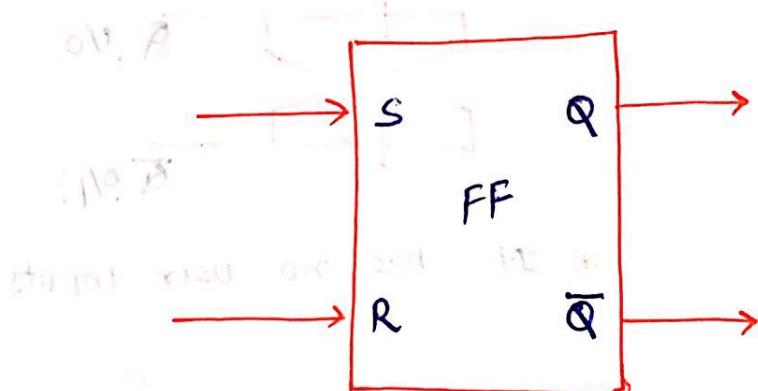
* Flip-Flop consist H/W for user I/p.

Ans

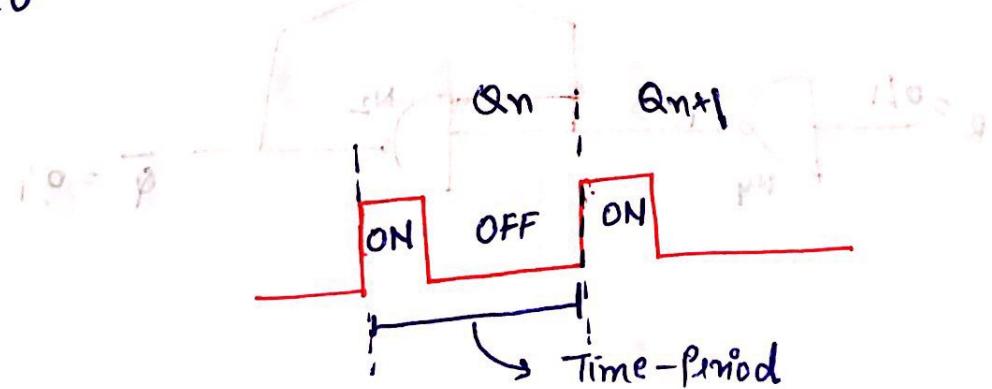
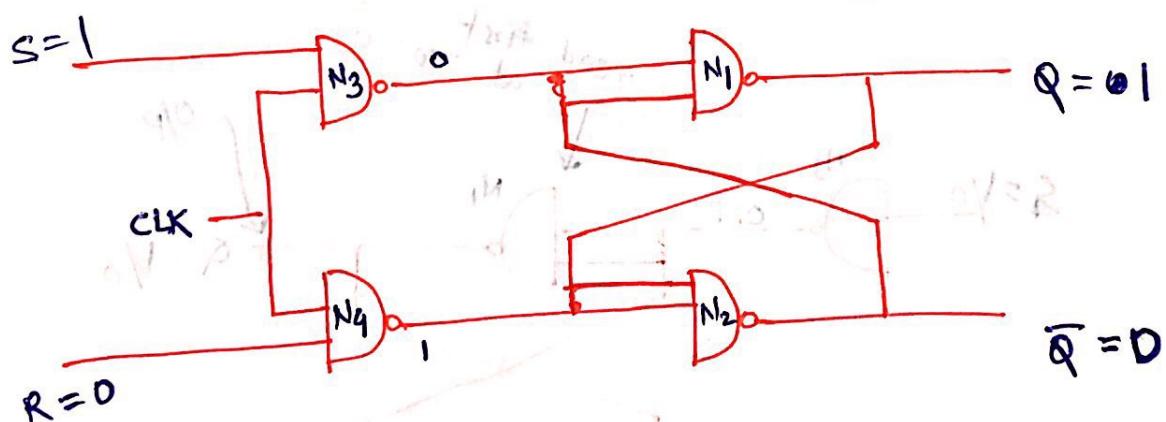
S-R Flip-Flop :-



S	R	O/p (Q)
0	0	Previous state
0	1	0 (Reset)] due to this
1	0	1 (set) it is known
1	1	Not allowed as <u>Set-Reset</u> <u>Flip Flop</u>

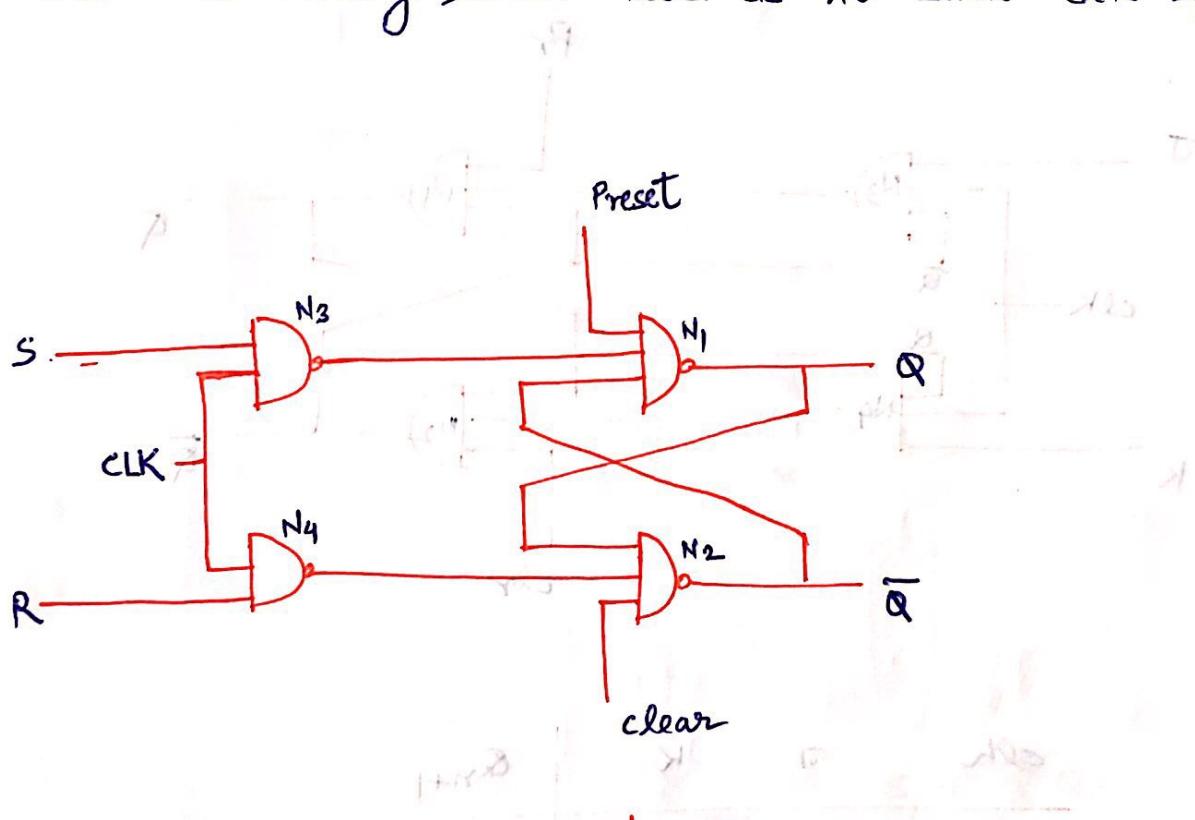


Clocked S-R Flip-Flop :-

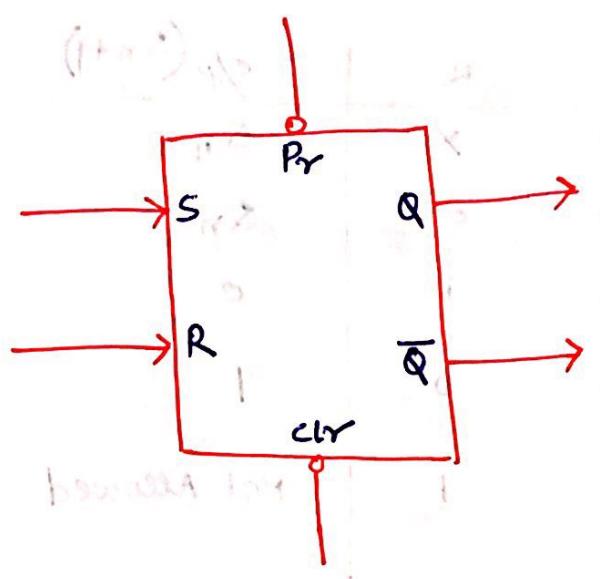


<u>CLK</u>	<u>S</u>	<u>R</u>	<u>O/p (Q_{n+1})</u>
0	x	x	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Not Allowed

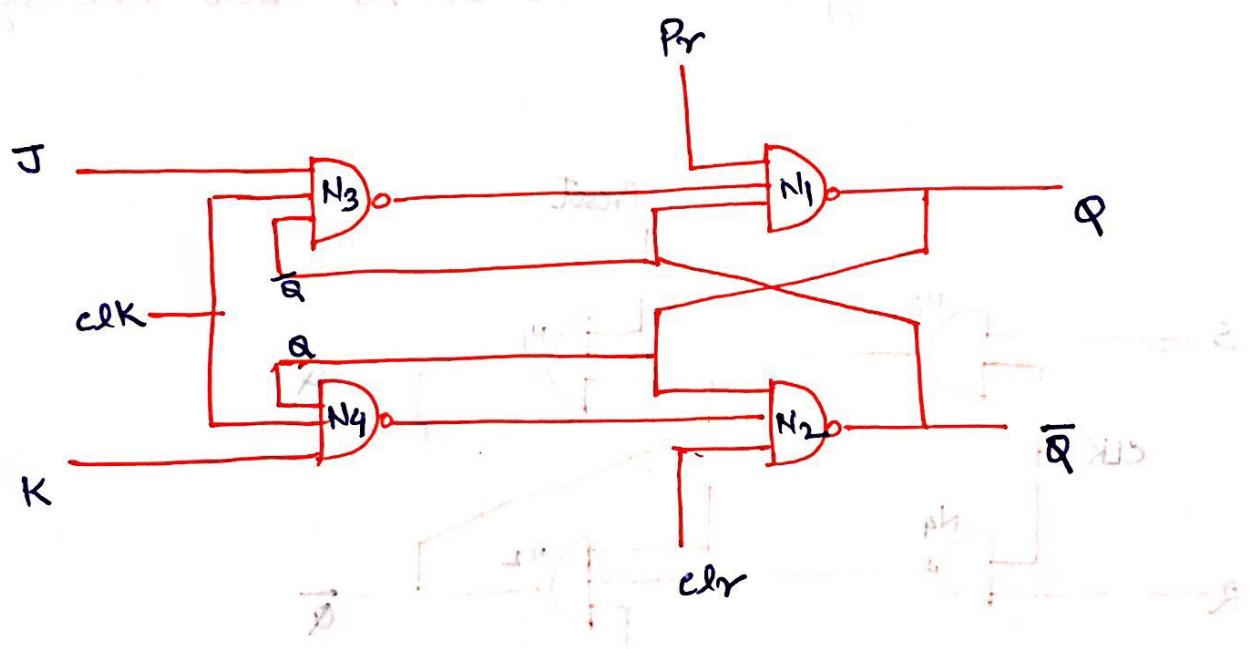
- * Flip-Flop opⁿ are always controlled by clocked signal whereas in Binary latch there is no such clk signal.



<u>CLK</u>	<u>Pr</u>	<u>Clr</u>	<u>Q</u>
0	0	1	1 ← PRESET
0	1	0	0 ← CLEAR
1	1	1	Normal operation
0	0	1	Not allowed



Logic symbols and block diagrams explain the logic with flip-flops
J-K Flip-Flop :-
 Logic symbol with state diagram for explanation



clk	J	K	Q_{n+1}
0	x	x	Q_n
1	0	0	?
1	0	1	0
1	1	0	1
1	1	1	\bar{Q}_n

characteristic Equation:- It is a mathematical eq.

which described behaviour of sequential circuit.

$$Q_{n+1}(\text{Input}, Q_n)$$

(i) S-R flip-flop:-

S	R	Q_n	Q_{n+1}
0	0	0	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

S	R	Q_n	Q_{n+1}
0	0	0	0
0	1	0	1

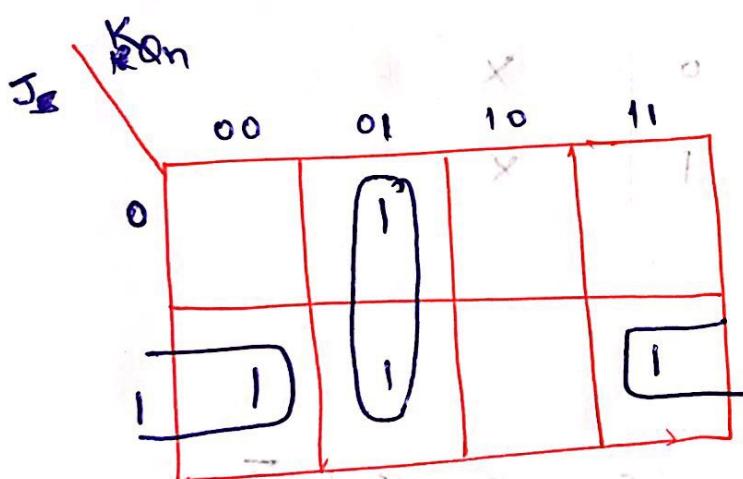


$$Q_{n+1} = S + \bar{R} Q_n$$

(ii) for J-K flip-flop :-

state differences to be examined by means of truth table

<u>J</u>	<u>K</u>	<u>Q_n</u>	<u>Q_{n+1}</u>
0	0	0	0] <u>Q_n</u>
0	0	1	1]
0	1	0	- <u>Q_{n+1}</u> (1)
0	1	1	0
1	0	0	1] <u>Q_{n+1}</u>
1	0	1	0]
1	0	1	1]
1	1	0	1] <u>Q_{n+1}</u>
1	1	1	0]



$$(Q_{n+1}) = J\bar{Q}_n + \bar{K}Q_n$$

Excitation Table :- It shows the transition of Q_n to Q_{n+1} for set of inputs.

Q_n	$\rightarrow Q_{n+1}$	Inputs
-------	-----------------------	--------

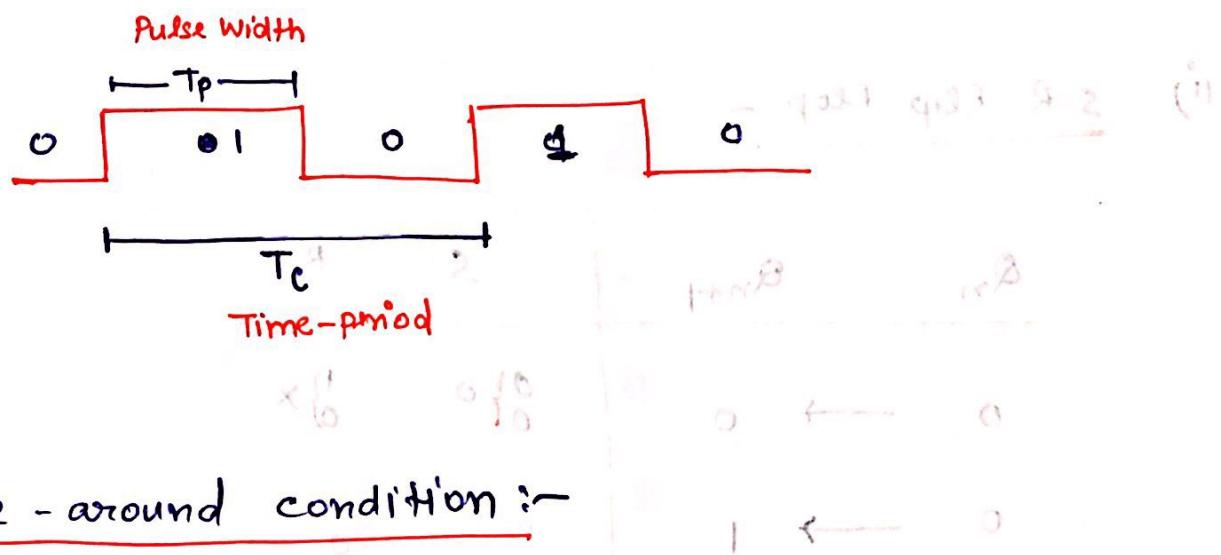
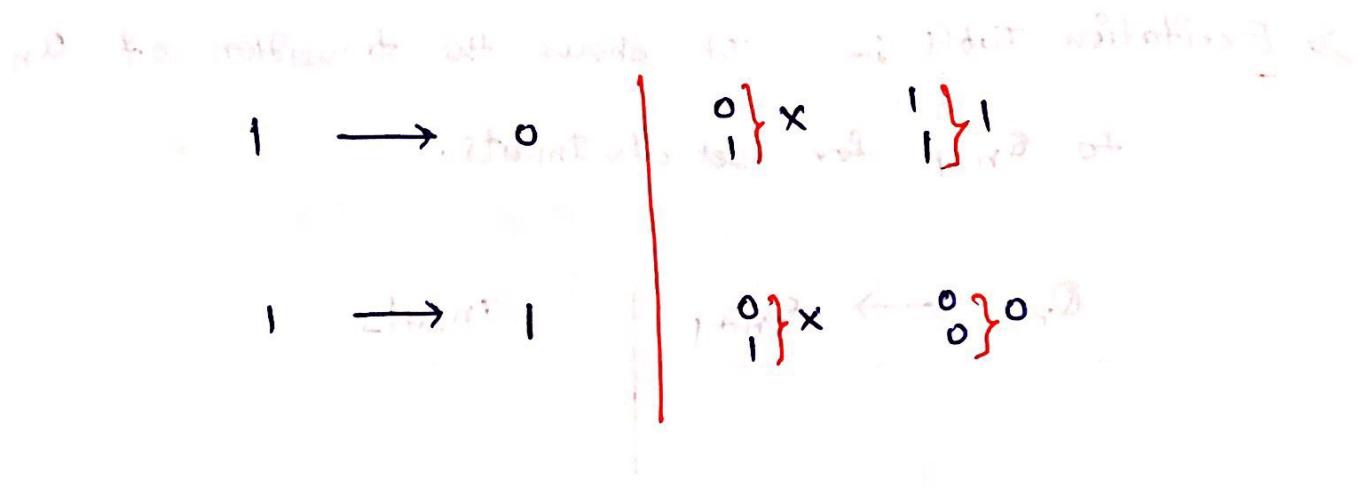
(i) S-R flip Flop :-

Q_n	Q_{n+1}	S	R
0 \rightarrow 0	0 { 0	0 { X	0 { 0
0 \rightarrow 1	1 { 0	1 { 0	0 { 0
1 \rightarrow 0	0 { 0	0 { 1	1 { 0
1 \rightarrow 1	1 { X	1 { 0	0 { 0

* E.T are useful in synchronous sequential circuit.

(ii) J-K Flip-Flop :-

Q_n	Q_{n+1}	J	K
0 \rightarrow 0	0 { 0	0 { 0	0 { X
0 \rightarrow 1	1 { 1	1 { 1	0 { X



Race-around condition :-

Let in J-K flip-flop $\Rightarrow J=1, K=1$

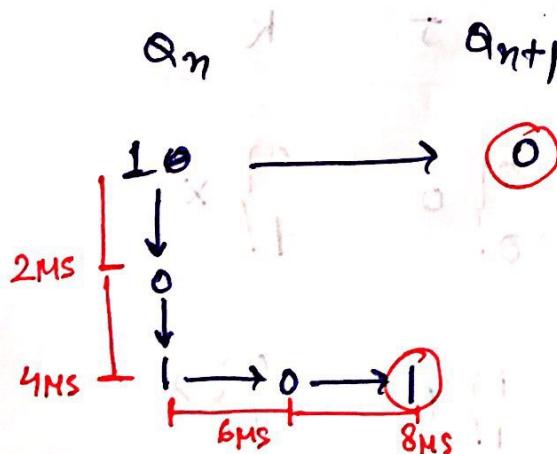
$$(Q_{n+1} \overline{Q_n})$$

$$\text{Let } T_p = 8\text{ ms}$$

$$T_{pd} = 2\text{ ms}$$

After 1 8ms o/p is 1

whereas expected o/p is 0



so, this condition

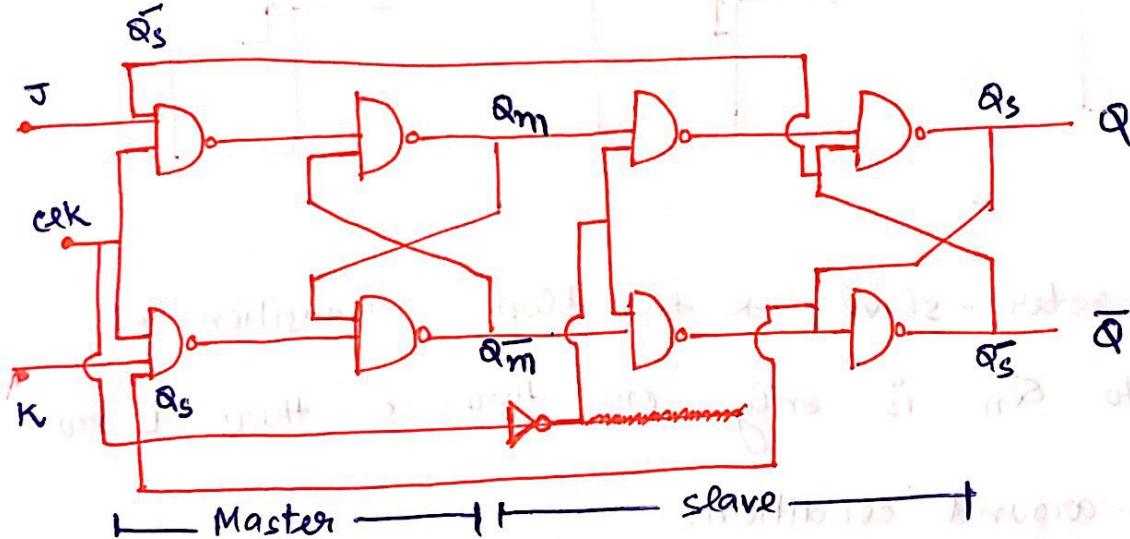
is known as race-around condition.

* To eliminate Race-around condition:

$$(T_p \leq T_{pd} < T_c)$$

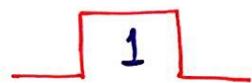
But sometime due to change in temperature and pressure condition in environment, electrical properties of clk like (resistance, Inductance) changes which can alter this condition, so this is not a rugged solution.

To completely solve this problem we use master slave J & K flip flop.

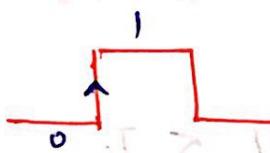


- Due to inverted CLK signal only one of the master and slave circuit will be enabled,
- thus when change takes place in master ckt, the change can't be transferred to slave ckt until pulse of CLK ^{will} be changed.

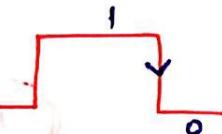
Right edge triggered and left edge triggered



level triggered



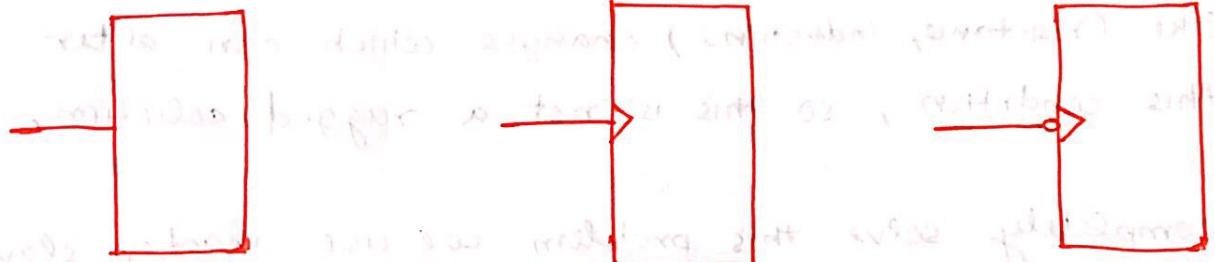
+ve Edge triggered



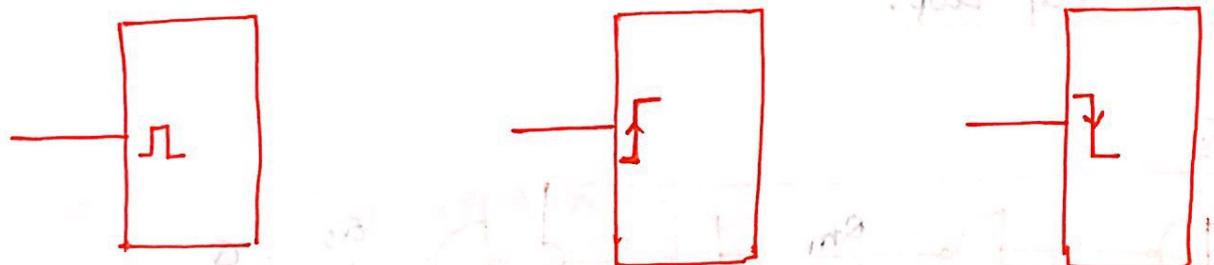
-ve edge triggered

Transition time depends on number of stages in sequence

Also as number of stages increases, transition time will increase



transition time depends on number of stages in sequence

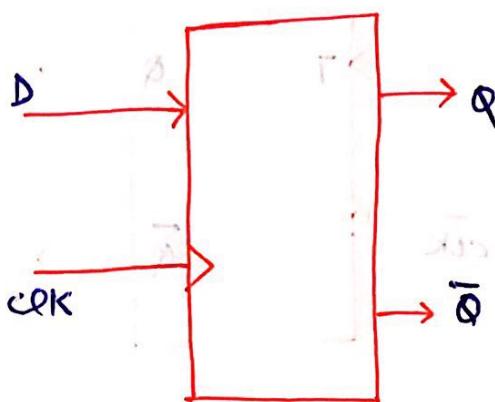


clock pulse

- In master-slave J-K flip flop, transition of Q_n to \bar{Q}_n is only one time, so there is no race-around condition.

- ~~Also~~ characteristic eq. and truth table are same as JK flip flop.
- Edge triggered clocks are used for synchronous sequential circuits.

D-Flip-flop :- (delay flip flop)



clk	D	Q_{n+1}
0	X	Q_n
0	0	0
0	1	0
1	0	1
1	1	1

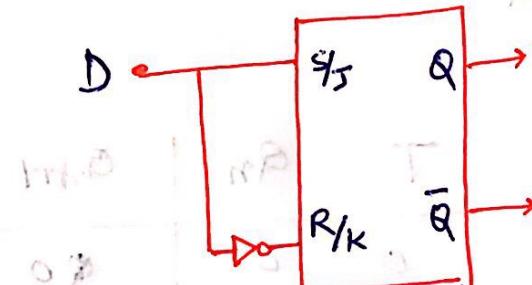
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$$Q_{n+1}(D, Q_n) = D$$

↳ characteristic eq.

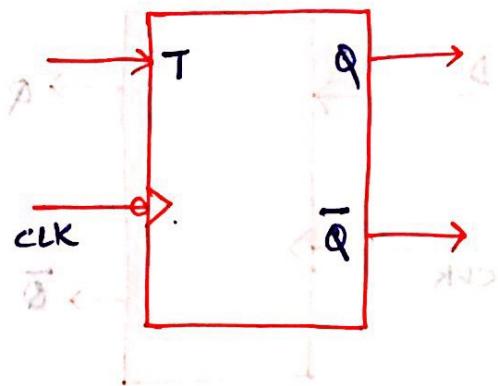
Q_n	\rightarrow	Q_{n+1}	D
0		0	0
0		1	1
1		0	0
1		1	1

Excitation table

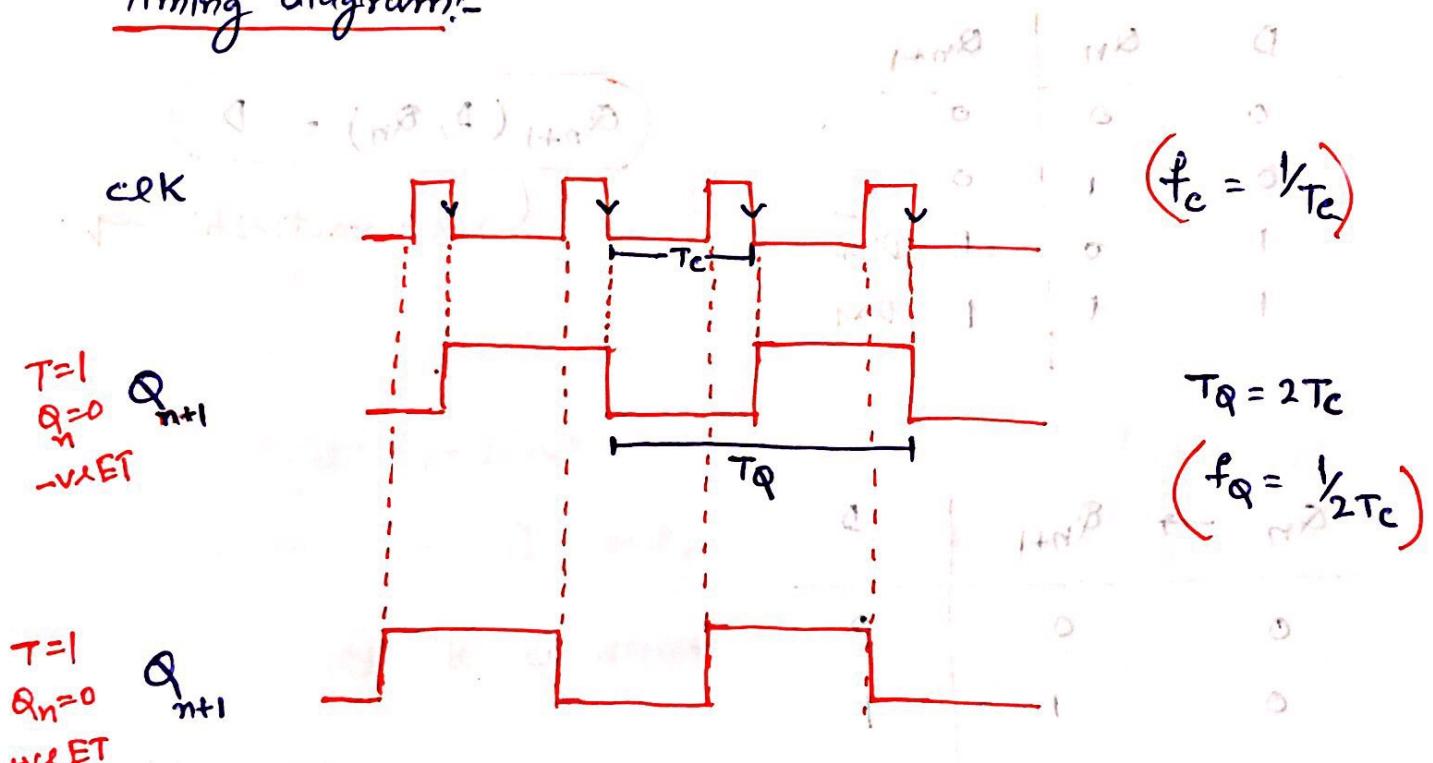


T-flip flop :- (Toggle flip flop)

clk	T	Q_{n+1}
0	X	Q_n
0	0	\bar{Q}_n
1	1	\bar{Q}_n



Timing diagram:-

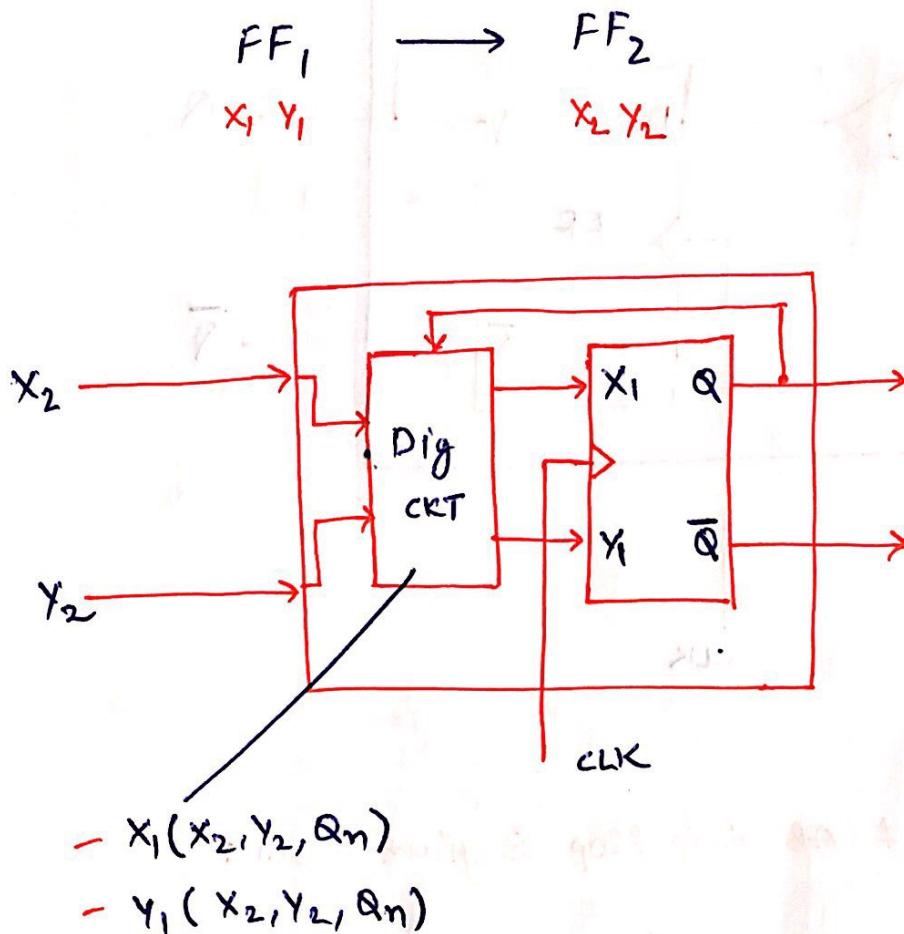


T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$$Q_{n+1} = \bar{T}Q_n + TQ_n$$

$$Q_{n+1} = T \oplus Q_n$$

Conversion's of FF₁ to FF₂ :-

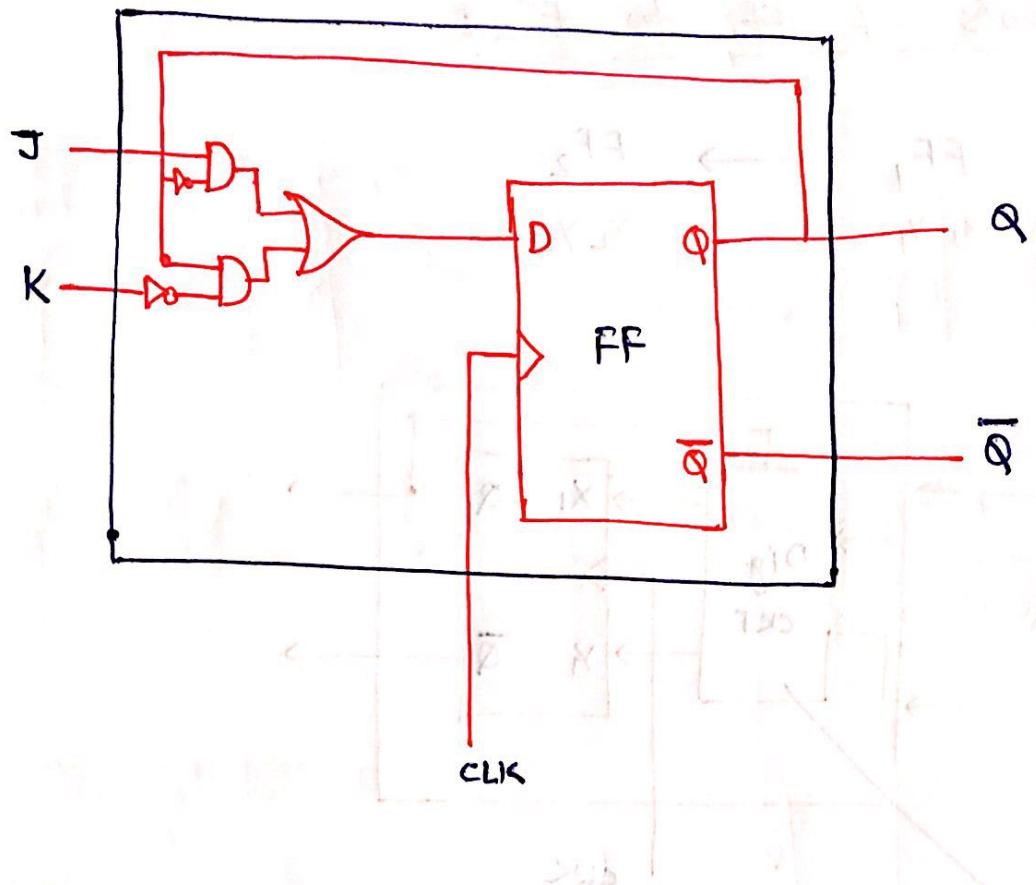


* To convert the FF₁ as FF₂, read the FF₁ I/p's as a func'n of FF₂ I/p's and Q_n.

Q. Convert D-Flip flop to J-K flip flop.

J	K	Q _n	Q _{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

$D(J, K, Q_n) \propto$
 $= J\bar{Q}_n + \bar{K}Q_n$



Q. The TT of AB flip flop is given below:

A	B	Q_{n+1}
0	0	1
0	1	Q_n
1	0	0
1	1	Q_n

(a) Develop characteristic eq. & E.T.

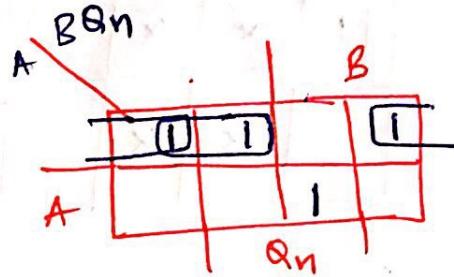
(b) Convert JK to AB flip flop

Convert D to T

T to U

(a)

A	B	Q_n	Q_{n+1}
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



$$Q_{n+1} = \overline{A}\overline{B} + \overline{A}Q_n + ABQ_n$$

Q_n	Q_{n+1}	A	B
0	0	1	x
0	1	0	x
1	0	x	x
1	1	x	x

(b)

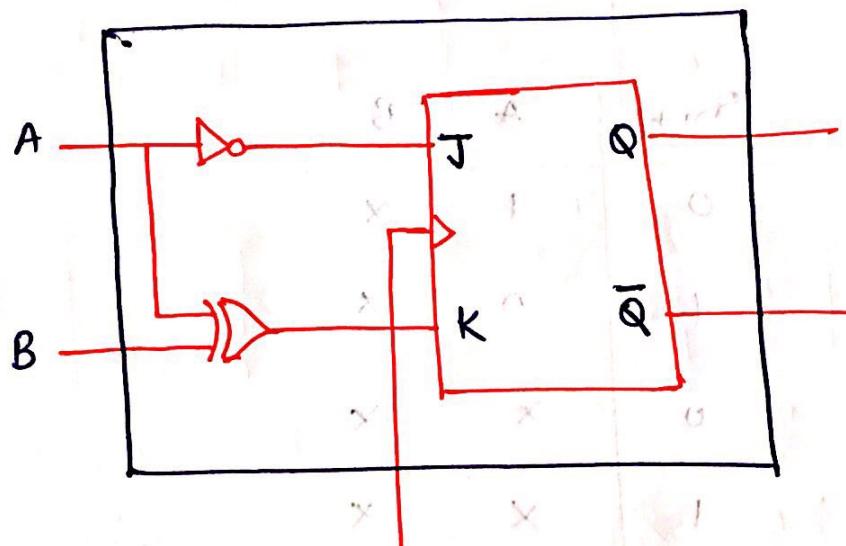
JK to AB :- $J(A, B, Q_n), K(A, B, Q_n)$

A	B	Q_n	Q_{n+1}	AJ	BK
0	0	0	1	1	x
0	0	1	1	x	0
0	1	0	1	1	x
0	1	1	0	x	1
1	0	0	0	0	x
1	0	1	0	x	1
1	1	0	0	0	x
1	1	1	1	x	0

J	K
BQ_n	BQ_{n+1}
$\begin{matrix} 1 & X & X & 1 \\ X & X \end{matrix}$	$\begin{matrix} X & & 1 & X \\ X & 1 & & X \end{matrix}$

$$(J = \bar{A})$$

$$\begin{aligned} K &= A\bar{B} + \bar{A}B \\ &= (A \oplus B) \end{aligned}$$



D to AB :-

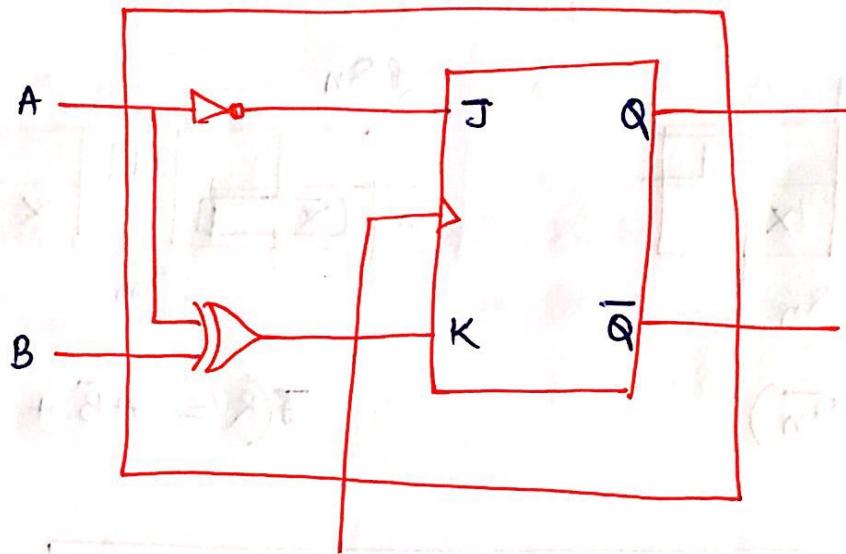
A	B	Q_n	Q_{n+1}	D	A
0	0	0	1	0	1
0	0	1	1	0	1
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	0	0	1
1	1	0	0	0	1
1	1	1	1	1	1

$$D = \overline{A}\overline{B}\overline{Q_n} + \overline{A}\overline{B}Q_n + \overline{A}B\overline{Q_n} + ABQ_n$$

T to AB flip-flop:-

- Q. A JK flip flop is converted to AB flip flop as shown in circuit. Identify characteristic eq. and excitation table.

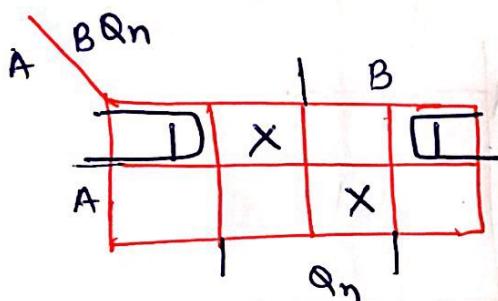
Convert SR flip flop to AB.



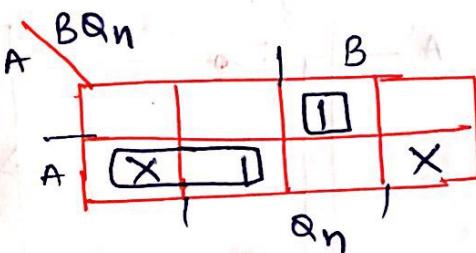
A	B	Q_n	Q_{n+1}	\overline{A}	J	K	$A \oplus B$
0	0	0	1	1	1	0	0
0	0	1	1	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1
1	0	0	0	0	0	1	1
1	0	1	0	0	0	1	1
1	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0

SR ff to AB ff

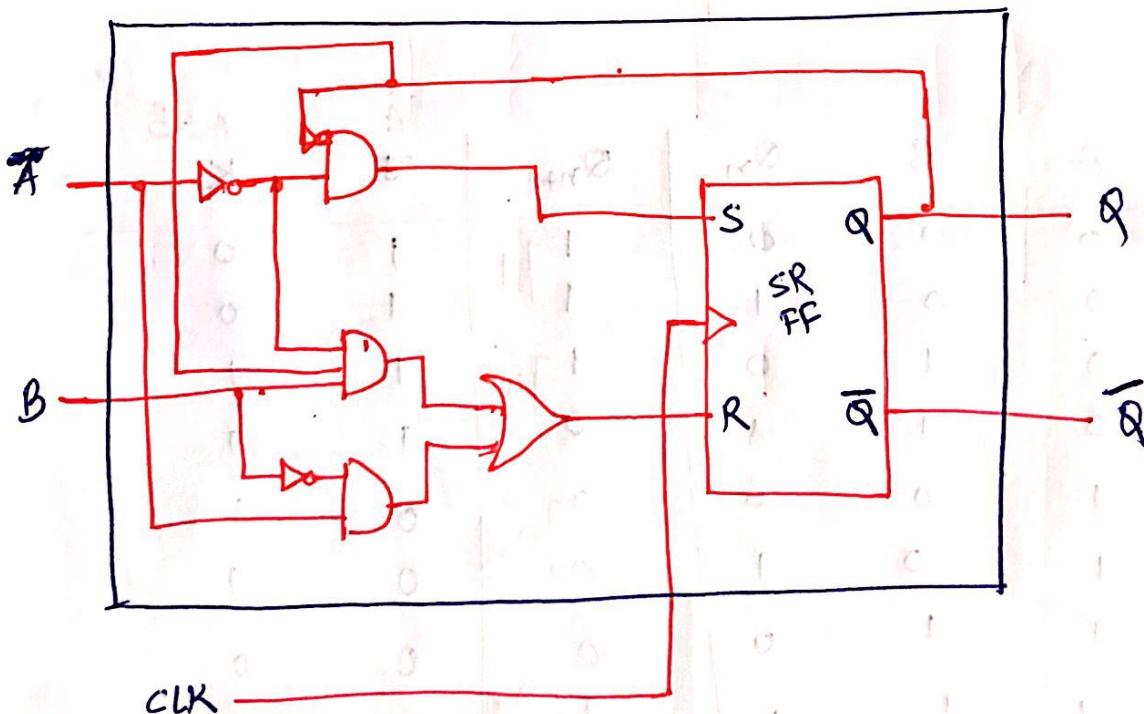
A	B	Q_n	Q_{n+1}	S	R
0	0	0	1	1	0
0	0	1	1	x	0
0	1	0	1	1	0
0	1	1	0	0	1
1	0	0	0	0	x
1	0	1	0	0	1
1	1	0	0	0	x
1	1	1	1	x	0



$$(S = \overline{A}Q_n)$$



$$J(R = A\bar{B} + \bar{A}BQ_n)$$



Register :-

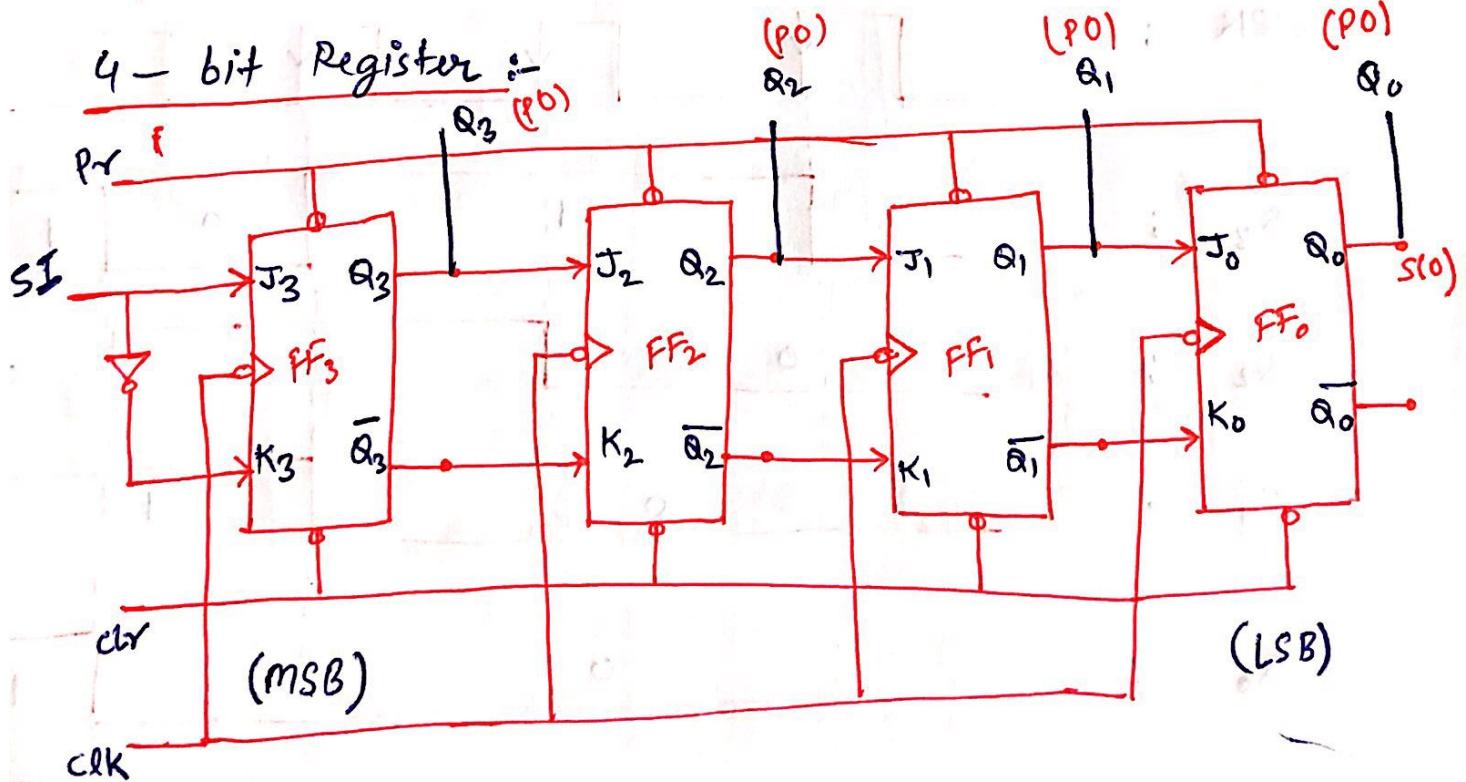
n -bit word \rightarrow ' n ' no. of FF

WRITER op n - [Serial I/p (counting 1-bit at a time)]
 Parallel I/p (writing all bit at a time)

READ op n - [serial O/p (Read 1-bit at a time)
 Parallel O/p (Read all-bit ")

- (i) SISO
 - (ii) SIPO
 - (iii) PISO
 - (iv) PIPO
- } Universal shift registers ↗ Rightshift ($L \rightarrow R$)
 } ↗ left shift ($R \rightarrow L$)

4-bit Register :-



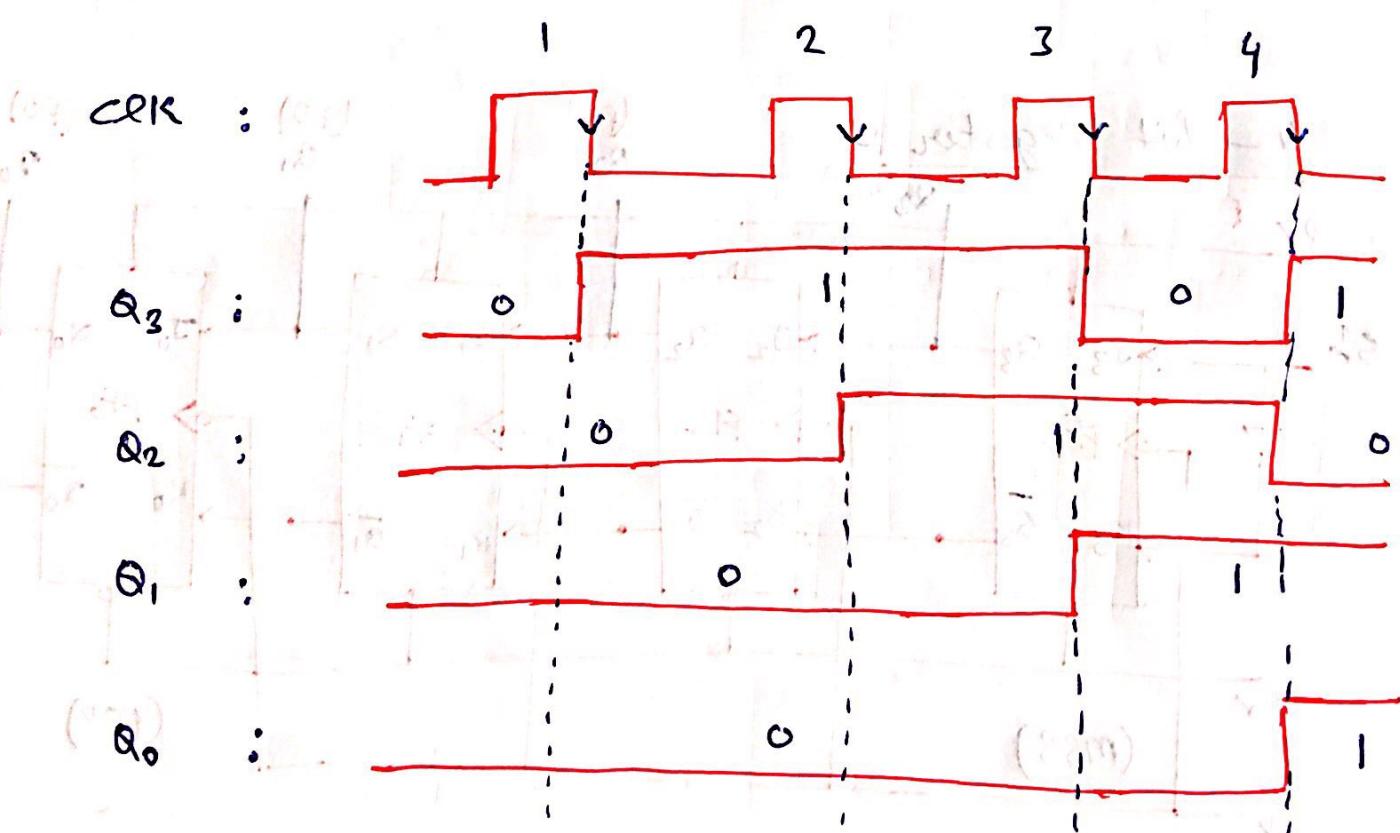
for clearing the FF load $P_r = 1$ and $Clr = 0$,

after clearing $P_r = Clr = 1$.

Let $SI = 1011$ Serial Input

<u>Clk</u>	<u>SI</u>	Q_3	Q_2	Q_1	Q_0
		0	0	0	0
1	$b_0(1)$	$1b_0$	0	0	0
2	$b_1(1)$	$1b_1$	$1b_0$	0	0
3	$b_2(0)$	$0b_2$	$1b_1$	$1b_0$	0
4	$b_3(1)$	$1b_3$	$0b_2$	$1b_1$	$1b_0$

Timing diagram :-



Parallel O/p :-

After 4 clk cycle Q_0, Q_1, Q_2, Q_3 all available in FF so we can access them simultaneously.

	$n=4$	n
SI	1	1
PO	0	0

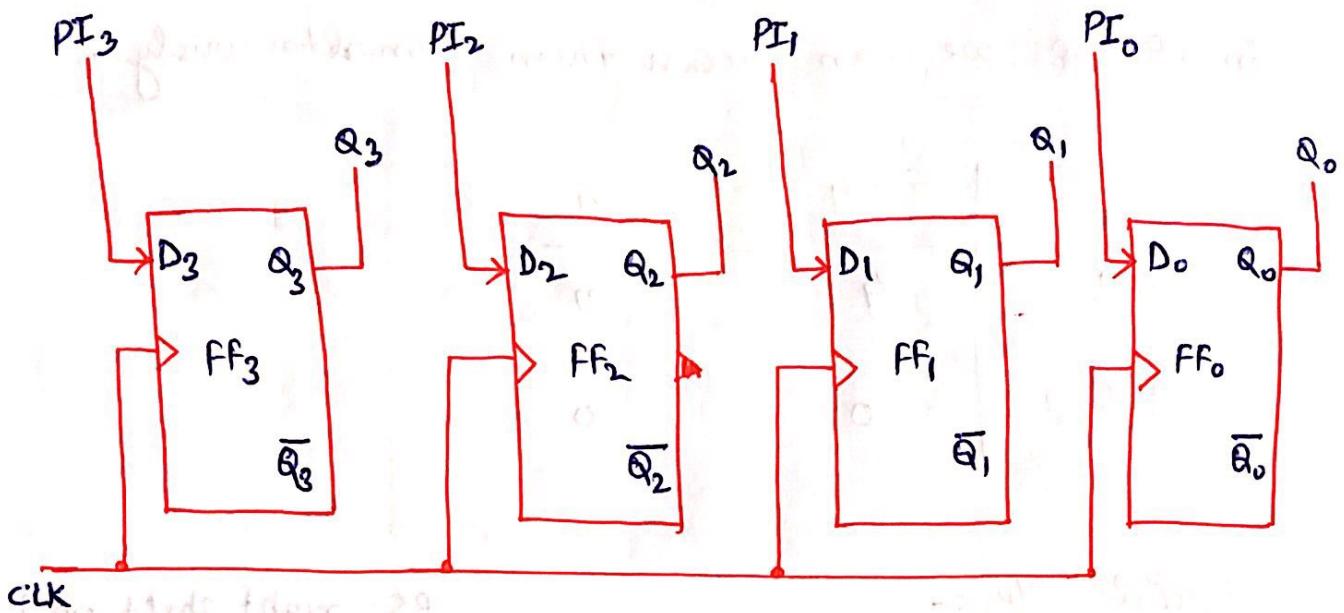
Serial O/p :-

RS: right shift op n

	clk	SI	Q_3	Q_2	Q_1	Q_0	$b_0 b_1 b_2 b_3$
(RS)	1	0	1	0	1	0	1 1
(RS)	2	0	0	0	0	1	0 0
(RS)	3	0	0	0	0	0	1 1
	4	0	0	0	0	0	0 0 0 0
			$n=4$	n			
		SO	3	$n-1$			

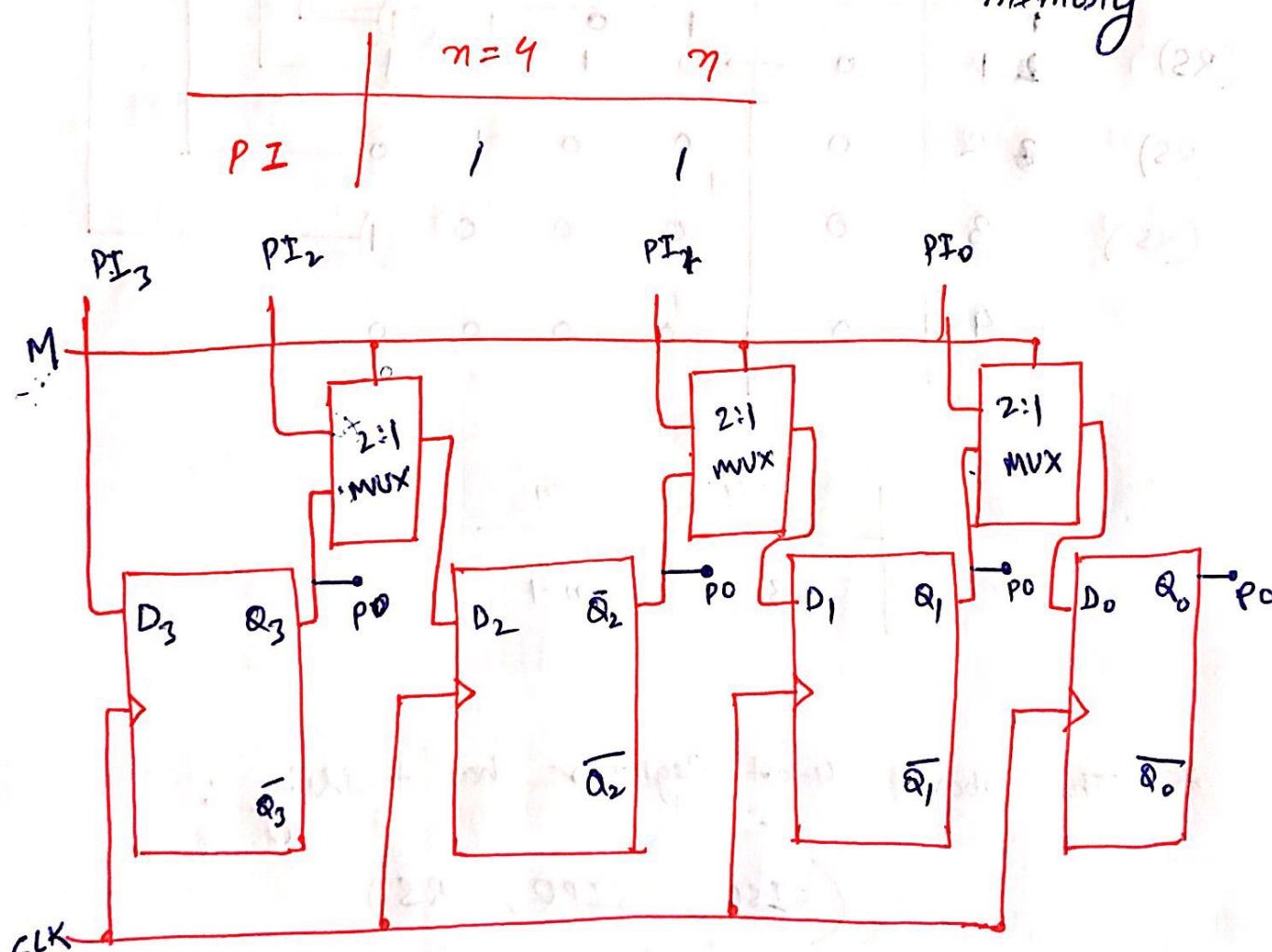
* The above 4-bit Register has facility :

(SISO, SIPO, RS)



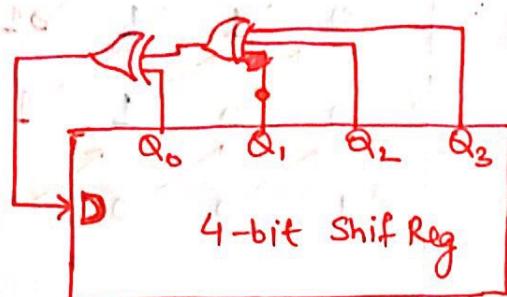
PIPO (Data Register)

↳ used in cache memory



$M = 0 \rightarrow \text{PIPO, PISO}$
 $M = 1 \rightarrow \text{SIPD, SISO}$

Q. A- 4-bit Right Shift Register shifting the data bit at each clock pulse. The serial I/p derive from Ex-OR as shown in figure.



After how many clock pulse, ckt is back to initial state, if initial content of the puls is

- (a) 1000 $Q_0 \ Q_1 \ Q_2 \ Q_3$

After 3 clock pulse content is

- (b) 1001 $Q_0 \ Q_1 \ Q_2 \ Q_3$

What is initial content of register.

(a)

clk	D	Q_3	Q_2	Q_1	Q_0
		0	0	0	1
1	1 \rightarrow	1	0	0	0
2	1 \rightarrow	1	1	0	0
3	0 \rightarrow	0	1	1	0
4	0 \rightarrow	0	0	1	1
5	0 \rightarrow	0	1	0	1
6	0 \rightarrow	0	0	1	0
7	0 \rightarrow	0	0	0	1

Ans = 7

(b)

clk	D	Q ₃	Q ₂	Q ₁	Q ₀
1	0	1	1	1	0
2	0	0	1	1	01
3	1	1	0	1	1

So, Initial content : 1 + 1 0

NOTE:-

SISO	No. of clk pulse
SIP0	2n-1
PISO	n
PIPO	1

⇒ Application of shift register :-

- It is possible to use to convert serial data to parallel form with SIP0 opⁿ.

- It is possible to use to convert parallel data to serial form by using PISO opⁿ.

- It is possible to use as a delay ckt.

- It is possible to use as divided by two ckt with right shift opⁿ.

$$\begin{array}{r} \text{MSB} & \text{LSB} \\ \hline Q_3 & Q_2 & Q_1 & Q_0 & \text{decimal} \\ \hline 1 & 0 & 1 & 0 & \rightarrow 10 \\ 0 & 1 & 0 & 1 & \rightarrow 5 & \text{RS op}^n \\ \hline & 1 & 0 & 1 & 1 & \rightarrow 11 \\ 0 & 1 & 0 & 1 & \rightarrow 5 & \text{RS op}^n \end{array}$$

If (LSB = 0) then it is a true division

else it is with error of 0.5 (floor division).

(LSB=1)

- It is possible to use as multiply by 2 ckt with left shift opⁿ (LS).

$$\begin{array}{r} \text{Q}_3 & \text{Q}_2 & \text{Q}_1 & \text{Q}_0 & \text{decimal} \\ \hline 0 & 0 & 1 & 0 & 5 \\ \hline 1 & 0 & 1 & 0 & 10 & \text{LS op}^n \end{array}$$

True MUL

at state 01001 two of 13 division by 2
 $1 \quad 0 \quad 1 \quad 0 \quad \underline{-} \quad 10$
 False MUL
 error of

the period is 2ⁿ of division by 2ⁿ = 24
 $13 \times 2 = 26$
 $= 16$

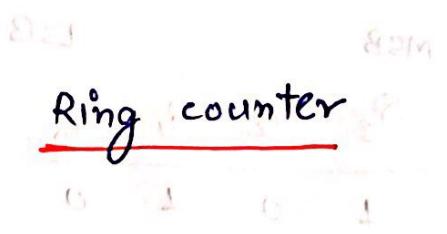
After this point of period in case of division by 2

It is possible to use it as a counter.

(a)

$Q_0 \Rightarrow SI$

Ring counter



(b)

$\overline{Q_0} \Rightarrow SI$

Twisted Ring counter
or

Johnson counter

Moebious counter

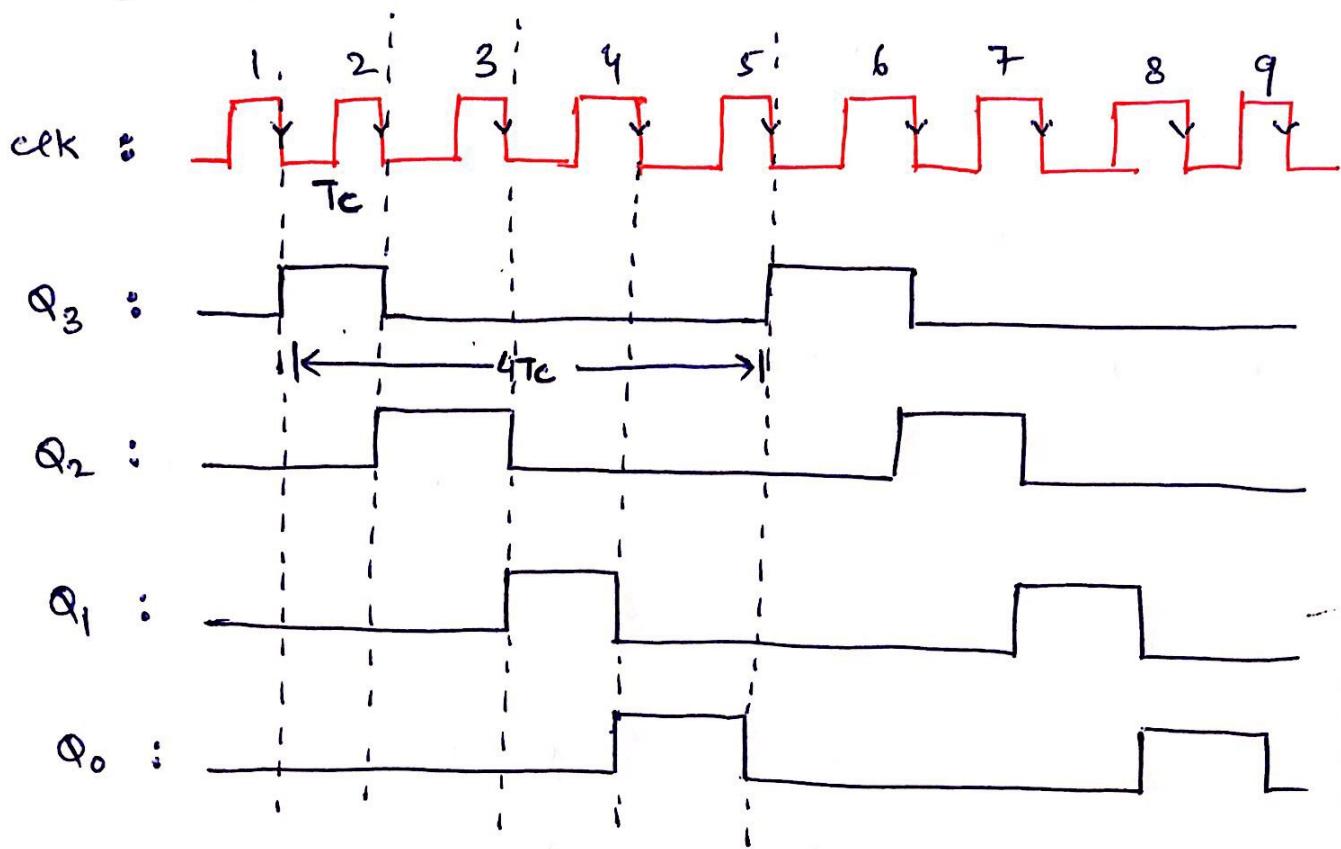
NOTE:-

The best way to use register as counter is

one of the bit = 1 and remaining must be 0.

CLK	SI	$Q_3 \quad Q_2 \quad Q_1 \quad Q_0$	Mod K counter
		0 0 0 1	
1	1	1 0 0 0	
2	0	0 1 0 0	$K = 4$
3	01	0 0 1 0	
4	0	0 0 0 1	

Timing diagram :-



$$f_{Q_3, Q_2, Q_1, Q_0} = \frac{1}{4T_c} = \frac{f_{clk}}{4}$$

$K = 8$

clk	$S \swarrow \bar{Q}_0$	Q_3	Q_2	Q_1	Q_0
1	0	0	0	0	1
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	0	1	1	1
7	0	0	0	1	1
8	0	0	0	0	1