UNIT 3 - IMPORTANT QUESTIONS Date.....

Q1. What is an instruction in the context of computer organization? Explain the purpose of the various elements of an instruction with the help of a simple instruction format.

Q2 Evaluate the arithmetic statement $X = (A+B) * (C+D)$ using a general register computer with three address, two address and one address instruction format a program to evaluate the expression.
[AKTU-2018-19] [AKTU- 2014-15]

Q3 Explain all the phases of instruction cycle.
[AKTU - 2018-19]

Q4 Write the steps in fetching a word from memory. Differentiate between a branch instruction and call subroutine instruction.
[AKTU-2014-15]

Q5. In an instruction format, there are 16 bits in an instruction word. Bit 0 and 11 convey the address of the memory location for memory related instructions. For non memory instructions these bits convey various register or I/O operations. Bits 12 to 14 show the various basic memory operations such as ADD, AND, LDA etc. Bit 15 shows if the memory is accessed directly or indirectly. For such an instruction format draw block diagram of the control unit of a computer and briefly explain how an instruction will be decoded and executed, by this control unit.
[AKTU - 2016-17]

Q6 List and explain different types of shift micro operation.
[AKTU - 2016-17]

Spiral

Date.....

Q7 What are the different categories of micro operations that may be carried out by CPU? Explain each category of micro-operations giving one example for each. [2014-15]

Q8 What is CISC? Explain its characteristics. [2015-16]

Q9 What is RISC? Explain its various characteristics. [2015-16]

Q10 Give the detailed comparison between RISC and CISC [2018-19] [2015-16]

Q11 Write a short note on pipelining.

Q12 Explain the basic concept of hardwired and Software control unit with neat diagrams. [2014-15] [2015-16] [2018-19]

Q13 What is micro-programmed control unit? Give the basic structure of micro-programmed control unit. Also discuss the micro-instruction format and the control unit organization for a typical micro programmed controllers using suitable diagram. [2017-18]

Q14 Write a short note on micro program sequencer for control memory.

Q15 Briefly define the following terms. [2016-17] [2018-19] [2014-15]

(i) Micro operation
(ii) Micro instruction
(iii) Micro program.
(iv) Micro-code.
(v) Control memory.

Spiral

Date.....

Q16. Write an assembly level program for the following pseudo code.

```
SUM = 0
SUM = SUM + A + B
DIF = DIF - C
SUM = SUM + DIF
```

Q17. Explain 4-bit incrementer with a necessary diagram.

Q18. Write a program loop using a pointer and a counter to clear the contents of hex locations 500 to 5FF with 0.

Q19. Demonstrate the process of second pass of assembler using a suitable diagram.

———.———

UNIT-4 IMPORTANT QUESTIONS Date.....

Questions are from "2014-15" "2015-16", "2016-17", "2017-18" & "2018-19".

Q1 Give the structure of commercial 8M x 8 bit DRAM chip.

Q2 A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts an indirect bit, an operation code, a register code part to specify one of 64 register and an address part.

(i) How many bits are there in the operation code, the register code part and the address part?

(ii) Draw the instruction word format and indicate the number of bits in each part.

(iii) How many bits are there in the data and address inputs of the memory?

Q3 Consider a cache uses a direct mapping scheme. The size of main memory is 4K bytes and word size of cache is 2 bytes. The size of cache is memory is 128 bytes. Find the following:

(i) The size of main memory address (assume each bytes of main memory has an address)

(ii) Address of cache block.

(iii) How many memory location address will be translated to cache address/ block/ location.

(iv) How can it be determined if the content of specified main memory address in cache?

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Date.....

Q4 A computer uses RAM chips of 1024*1 capacity.
(i) How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024*8?
(ii) How many chips are needed to provide a memory capacity of 16KB? Explain in words how the chips are to be connected to the address bus.

Q5 What do you mean by locality of reference? Explain with suitable example.

Q6 Explain the following memory schemes discussing why needed the:
(i) Interleaved memory. (ii) Associative memory.

Q7 Discuss the various types of address mapping using in cache memory.

Q8 Write short note on organization of 2D and 2.5D memory organization.

Q9 A ROM chip of 1024*8 has four select inputs & operates from a 5 volt power supply. How many pins are needed for the IC package? Draw a block diagram and label all input and output terminals in the ROM.

Q10 How main memory is useful in computer system? Explain the memory address map of RAM and ROM.

Date.....

Q11 What is associative memory? Explain with the help of a block diagram. Also mention the situation in which associative memory can be effective utilized.

Q12 A two way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from memory. The main memory size is 128K X 32.

(i) Formulate all pertinent information required to construct the cache memory.

(ii) What is the size of cache memory?

Q13 Write a short note on virtual memory?

Q14 What do you mean by CAM? Explain its major characteristics.

Q15 What is the distinction between spatial locality and temporal locality?

Q16 A moving arm disc storage device has the following specifications:

Number of tracks per recording surface = 200

Disc rotation speed = 2400 revolution / minute

Track - storage capacity = 62500 bits

Estimate the average latency and data transfer rate of this device.

Ajay Kumar Garg Engineering College, Ghaziabad
Department of Computer Science and Engineering

2nd III Sem Year Time Table Template

Day/Time	9:30-10:30	10:30-11:00	11:00-12:00
Monday	Lecture	BREAK	Lecture
Tuesday	Lecture		Lecture
Wednesday	Lecture		Lecture
Thursday	Lecture		Lecture
Friday	Lecture		Lecture

3rd V Sem Year Time Table Template

Day/Time	9:30-11:00	11:00-11:30	11:30-1:00
Monday	Lecture	BREAK	Lecture
Tuesday	Lecture		Lecture
Wednesday	Lecture		Lecture
Thursday	Lecture		Lecture
Friday	Lecture		Lecture

4th VII Sem Year Time Table Template

Day/Time	9:30-11:00	11:00-11:30	11:30-1:00
Monday	Lecture	BREAK	Lecture
Tuesday	Lecture		Lecture
Wednesday	Lecture		Lecture
Thursday	Lecture		Lecture
Friday	Lecture		Lecture

Ajay Kumar Garg Engineering College, Ghaziabad

Department of Computer Science and Engineering

2nd Year III SemCalender

Dec-20						
Mon	**Tue**	**Wed**	**Thur**	**Fri**	**Sat**	**Sun**
	1	**2**	**3**	**4**	**5**	**6**
	Revision Class for KCS-303				Preparatory off	Preparatory off
7	**8**	**9**	**10**	**11**	**12**	**13**
Revision Class for KCS-303					Preparatory off	Preparatory off
14	**15**	**16**	**17**	**18**	**19**	**20**
PUT (KCS-303)	Revision Class for KNC-301				Preparatory off	Preparatory off
21	**22**	**23**	**24**	**25**	**26**	**27**
Revision Class for KNC-301				Holiday (X'mas)	Preparatory off	Preparatory off
28	**29**	**30**	**31**			
PUT(KNC-301)	Revision Class for KCS-302					

Jan-21						
Mon	**Tue**	**Wed**	**Thur**	**Fri**	**Sat**	**Sun**
				1	**2**	**3**
				RC for Subject KCS-302	Preparatory off	Preparatory off
4	**5**	**6**	**7**	**8**	**9**	**10**
Revision Class for KCS-302					Preparatory off	Preparatory off
11	**12**	**13**	**14**	**15**	**16**	**17**
PUT (KCS-302)	Revision Class for KCS-301				Preparatory off	Preparatory off
18	**19**	**20**	**21**	**22**	**23**	**24**
Revision Class for KCS-301					Preparatory off	Preparatory off
25	**26**	**27**	**28**	**29**	**30**	**31**
PUT (KCS-301)	Rebublic Day	Revision Class for KAS-301			Preparatory off	Preparatory off

Feb-21						
Mon	**Tue**	**Wed**	**Thur**	**Fri**	**Sat**	**Sun**
1	**2**	**3**	**4**	**5**	**6**	**7**
Revision Class for KAS-301					Preparatory off	Preparatory off
8	**9**	**10**	**11**	**12**	**13**	**14**
PUT (KAS-301)	Revision Class for OE				Preparatory off	Preparatory off
15	**16**	**17**	**18**	**19**	**20**	**21**
Revision Class for OE					Preparatory off	Preparatory off
22	**23**	**24**	**25**	**26**	**27**	**28**
PUT (OE)						
25	**26**	**27**	**28**	**29**	**30**	

Ajay Kumar Garg Engineering College, Ghaziabad

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3rd Year V Sem Calender

Dec-20						
Mon	**Tue**	**Wed**	**Thur**	**Fri**	**Sat**	**Sun**
	1	**2**	**3**	**4**	**5**	**6**
	Revision Class for KCS-051				Preparatory off	Preparatory off
7	**8**	**9**	**10**	**11**	**12**	**13**
PUT (KCS-051)	Revision Class for KCS-503				Preparatory off	Preparatory off
14	**15**	**16**	**17**	**18**	**19**	**20**
PUT (KCS-503)	Revision Class for KCS-055				Preparatory off	Preparatory off
21	**22**	**23**	**24**	**25**	**26**	**27**
PUT (KCS-055)	Revision Class for KNC-501			Holiday (X'mas)	Preparatory off	Preparatory off
28	**29**	**30**	**31**			
PUT (KNC-501)	Revision Class for KCS-502					

Jan-21						
Mon	**Tue**	**Wed**	**Thur**	**Fri**	**Sat**	**Sun**
				1	**2**	**3**
				Revision Class for KCS-502	Preparatory off	Preparatory off
4	**5**	**6**	**7**	**8**	**9**	**10**
PUT (KCS-502)	Revision Class for KCS-501				Preparatory off	Preparatory off
11	**12**	**13**	**14**	**15**	**16**	**17**
PUT (KCS-501)						
18	**19**	**20**	**21**	**22**	**23**	**24**
25	**26**	**27**	**28**	**29**	**30**	**31**

Ajay Kumar Garg Engineering College, Ghaziabad

Department of Computer Science and Engineering

3rd Year Re-admit V Sem Calender

Dec-20						
Mon	**Tue**	**Wed**	**Thur**	**Fri**	**Sat**	**Sun**
	1	**2**	**3**	**4**	**5**	**6**
	Revision Class for RAS-501				Preparatory off	Preparatory off
7	**8**	**9**	**10**	**11**	**12**	**13**
PUT (RAS-501)	Revision Class for RCS-502				Preparatory off	Preparatory off
14	**15**	**16**	**17**	**18**	**19**	**20**
PUT (RCS-502)	Revision Class for RCS-503				Preparatory off	Preparatory off
21	**22**	**23**	**24**	**25**	**26**	**27**
PUT (RCS-503)	Revision Class for RUC-501			Holiday (X'mas)	Preparatory off	Preparatory off
28	**29**	**30**	**31**			
PUT (RUC-501)	Revision Class for RCS-052					

Jan-21						
Mon	**Tue**	**Wed**	**Thur**	**Fri**	**Sat**	**Sun**
				1	**2**	**3**
				Revision Class for RCS-052	Preparatory off	Preparatory off
4	**5**	**6**	**7**	**8**	**9**	**10**
PUT (RCS-052)	Revision Class for RCS-501				Preparatory off	Preparatory off
11	**12**	**13**	**14**	**15**	**16**	**17**
PUT (RCS-501)						
18	**19**	**20**	**21**	**22**	**23**	**24**
25	**26**	**27**	**28**	**29**	**30**	**31**

Ajay Kumar Garg Engineering College, Ghaziabad

Department of Computer Science and Engineering

4th Year VII Sem Calender

Dec-20						
Mon	**Tue**	**Wed**	**Thur**	**Fri**	**Sat**	**Sun**
	1	**2**	**3**	**4**	**5**	**6**
	Revision Class for RCS-702				Preparatory off	Preparatory off
7	**8**	**9**	**10**	**11**	**12**	**13**
PUT (RCS-702)	Revision Class for RCS-073				Preparatory off	Preparatory off
14	**15**	**16**	**17**	**18**	**19**	**20**
PUT (RCS-073)	Revision Class for RCS-701				Preparatory off	Preparatory off
21	**22**	**23**	**24**	**25**	**26**	**27**
PUT (RCS-701)	Revision Class for OE			Holiday (X'mas)	Preparatory off	Preparatory off
28	**29**	**30**	**31**			
PUT (OE)	Revision Class for RCS-075					

Jan-21						
Mon	**Tue**	**Wed**	**Thur**	**Fri**	**Sat**	**Sun**
				1	**2**	**3**
				Revision Class for RCS-075	Preparatory off	Preparatory off
4	**5**	**6**	**7**	**8**	**9**	**10**
PUT (RCS-075)	**Project PPT**				Preparatory off	Preparatory off
11	**12**	**13**	**14**	**15**	**16**	**17**
Project PPT						
18	**19**	**20**	**21**	**22**	**23**	**24**
25	**26**	**27**	**28**	**29**	**30**	**31**

Ajay Kumar Garg Engineering College, Ghaziabad

PUT Proposed Schedule

Department of Computer Science and Engineering

3rd & 4th Year PUT Schedule

Timing: 10:00AM to 1:00 PM

Branch/Date	07-Dec-20		14-Dec-20		21-Dec-20		28-Dec-20		04-Jan-21		11-Jan-21
Year	III	IV	III	IV	III	IV	III	IV	III	IV	III
CSE	KCS-051	RCS-702	KCS-503	RCS-073	KCS-055	RCS-701	KNC-501	OE	KCS-502	RCS-075	KCS-501

2nd Year PUT Schedule

Timing: 10:00AM to 1:00 PM

Branch/Date	14-Dec-20	28-Dec-20	11-Jan-21	25-Jan-21	08-Feb-21	22-Feb-21
Year	II	II	II	II	II	II
CSE	KCS-303	KNC-301	KCS-302	KCS-301	KAS-301	OE
CS	KCS-303	KNC-301	KCS-302	KCS-301	KAS-301	OE

3rd Year Readmitted PUT Schedule

Timing: 10:00AM to 1:00 PM

Branch/Date	07-Dec-20	14-Dec-20	21-Dec-20	28-Dec-20	04-Jan-21	11-Jan-21
Year	II	II	II	II	II	II
CSE	RAS-501	RCS-502	RCS-503	RUC-501	RCS-052	RCS-501

Highlighted subjects are common between branch(s).