COMPUTER ORGANIZATION AND ARCHITECTURE (COA)

EET 2211
4TH SEMESTER – CSE & CSIT
CHAPTER 5, LECTURE 20

CHAPTER 5
INTERNAL MEMORY

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TOPICS TO BE COVERED

- Semiconductor Main Memory
- Error Correction

LEARNING OBJECTIVES

After studying this chapter you should be able to:

- Present an overview on the principle types of semiconductor main memory.
- Understand the operation of a basic code that can detect and correct single-bit errors in 8-bit words.

INTRODUCTION

✓In earlier computers the most common form of random-access storage for computer main memory employed an array of doughnut-shaped ferromagnetic loops known as CORES.

✓In this chapter we will be studying semiconductor main memory subsystems including ROM, DRAM and SRAM memories.

✓Also error control techniques used to enhance memory reliability.

SEMICONDUCTOR MAIN MEMORY

ORGANIZATION

✓The basic element of a semiconductor memory is the memory cell.

✓All semiconductor memory cells share certain properties:

i. They exhibit two stable states which can be used to represent binary 1 and 0.

ii. They are capable of being written into to set the state.

iii. They are capable of being read to sense the state.

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- ✓The cell has 3 functional terminals capable of carrying an electrical signal.
- ✓The selected terminal selects a memory cell for read or write operation.
- ✓The control terminal indicates read or write.

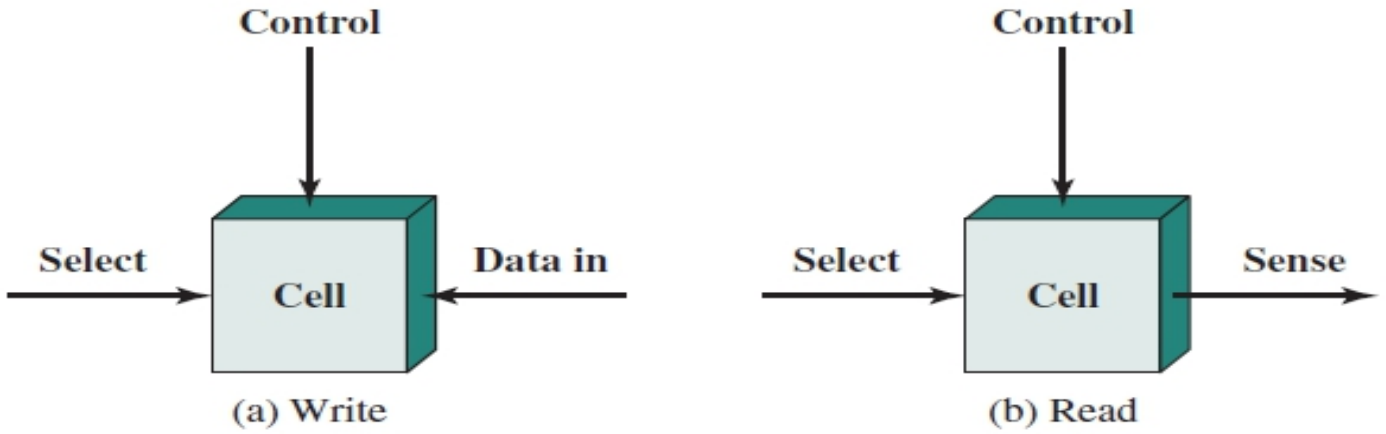

Fig.1: Memory cell operation [Source: Computer Organization and Architecture by William Stallings]

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RAM

- ✓ The most common is RAM (Random access memory).
- ✓ It reads data from memory and to write new data into the memory easily and rapidly.
- ✓ Both reading and writing is accomplished through the use of electrical signals.
- ✓ It is volatile in nature.
- ✓ It must be provided with constant power supply.
- ✓ RAM acts as a temporary data storage.
- ✓ Two forms are DRAM and SRAM.

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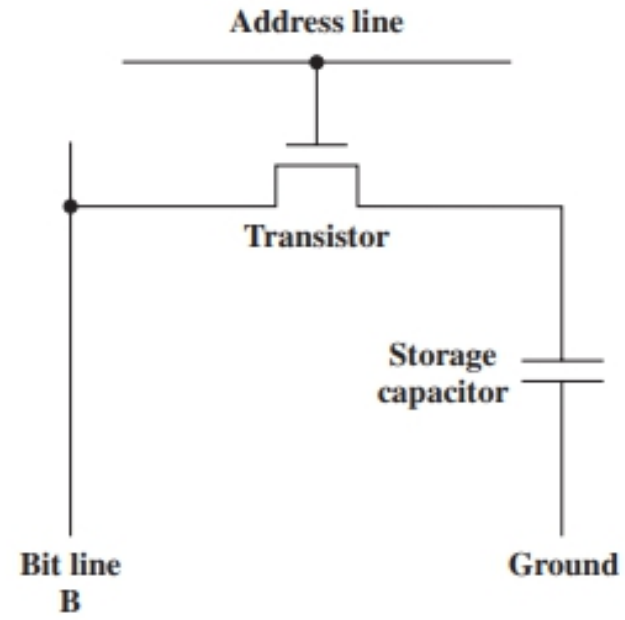
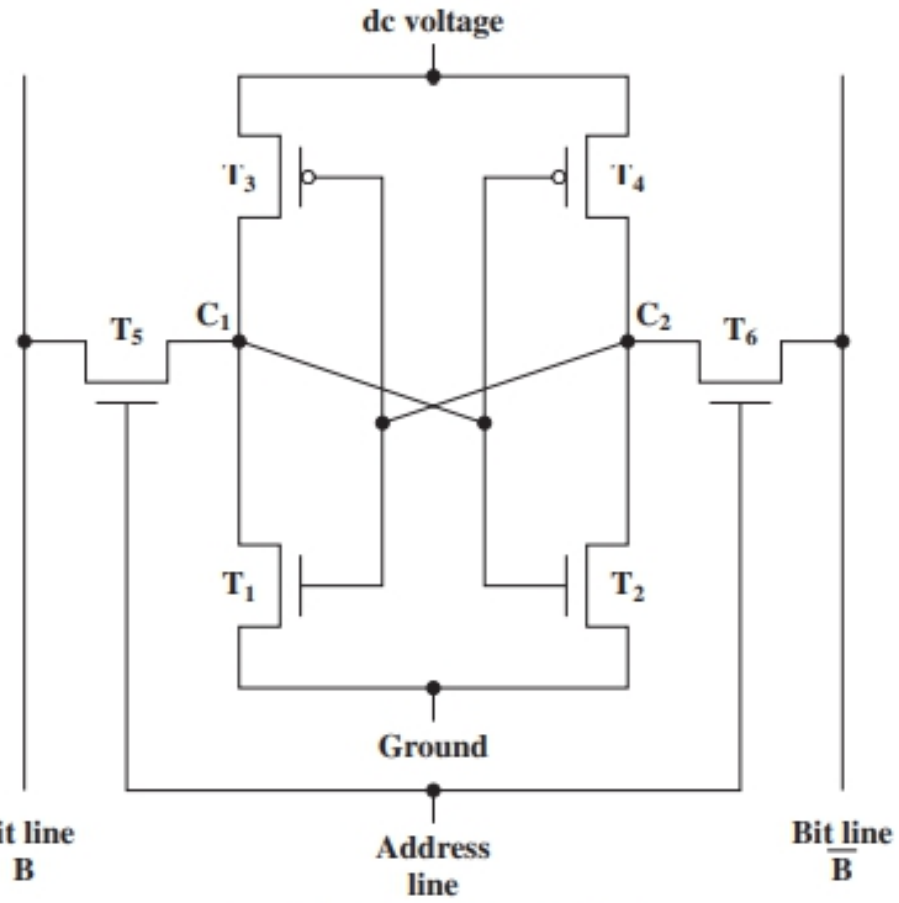
DRAM and SRAM

- ✓ DRAM is made with cells that store data as charge on capacitors.
- ✓ The presence or absence of charge in a capacitor is interpreted as a binary 1 or 0.
- ✓ As capacitors have a natural tendency to discharge, it requires periodic charge refreshing to maintain data storage.
- ✓ SRAM is a digital device that uses the same logic elements used in processor.
- ✓ In SRAM binary values are stored using traditional flip-flop logic-gate configurations.
- ✓ A SRAM will hold its data as long as power is supplied to it.

DRAM and SRAM



(a) Dynamic RAM (DRAM) cell



(b) Static RAM (SRAM) cell

SEMICONDUCTOR MEMORY TYPES

Memory Type	Category	Erasure	Write Mechanism	Volatility
Random-access memory (RAM)	Read-write memory	Electrically, byte-level	Electrically	Volatile
Read-only memory (ROM)	Read-only memory	Not possible	Masks	Nonvolatile
Programmable ROM (PROM)			Electrically	
Erasable PROM (EPROM)	Read-mostly memory	UV light, chip-level		
Electrically Erasable PROM (EEPROM)		Electrically, byte-level		
Flash memory		Electrically, block-level		

ERROR CORRECTION

A semiconductor memory is subject to errors. They can be categorized into:

(i) Hard Failure

(ii) Soft errors

- ✓A hard failure is a permanent physical defect so that the memory cell or cells affected cannot reliably store data but become stuck at 0 or 1 or switch erratically between 0 and 1.

- ✓`A soft error is a random, non-destructive event that alters the contents of one or more memory cells without damaging the memory.

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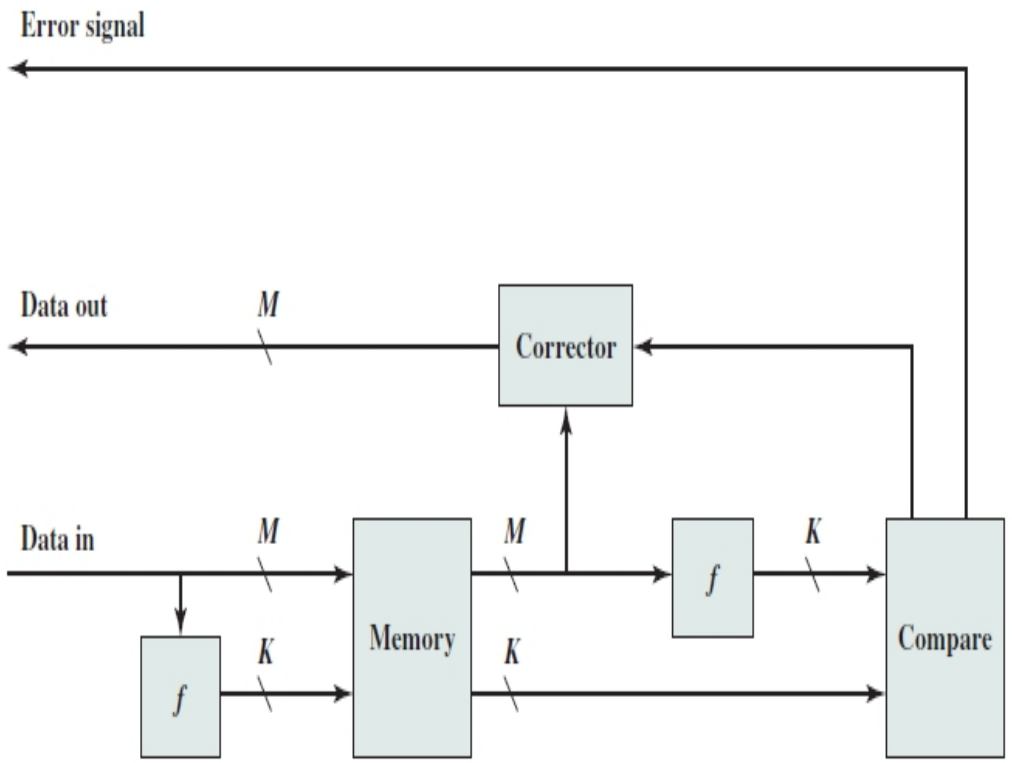
- Hard Failure
  - Permanent physical defect.
  - Memory cells affected cannot reliably store data.
  - Caused due to harsh environmental abuse, manufacturing defects and wear etc.
- Soft errors
  - Random and non-destructive events.
  - It alters the content of one or more memory cells without damaging the memory.
  - Caused due to power supply or alpha particles.

Error-Correcting Code Function

- When data are to be written into memory, a calculation (f) is performed on the data to produce a code.
- If an M-bit word of data is to be stored and the code is of length K bits, then the actual size of the stored word is M+K bits.
- When the previously stored word is read out, the code is used to detect and possibly correct errors.

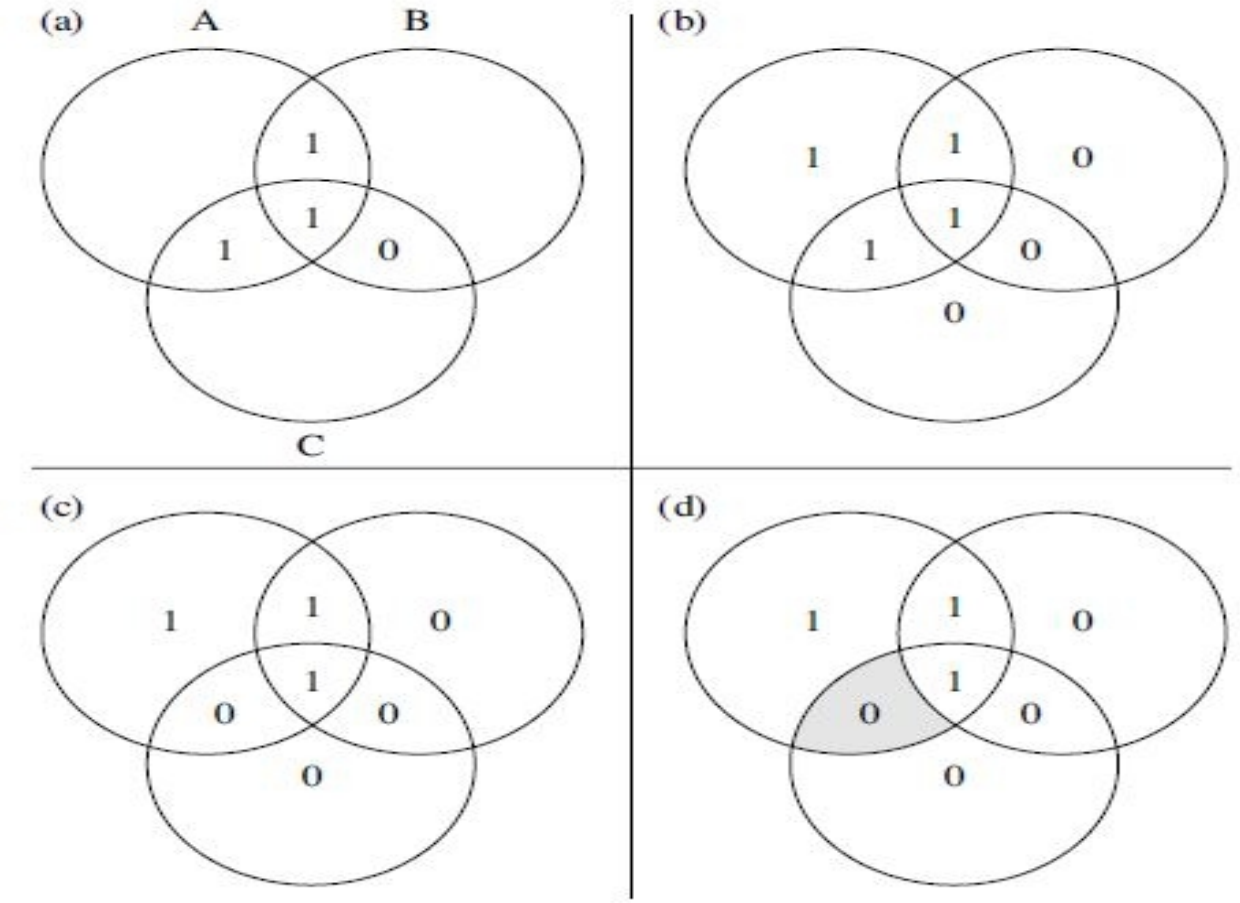


Error-correcting code function

- Prior to storing data a code is generated from the bits in the word.
- Code is stored along with the word in memory.
- Code used to identify and correct errors.
- When the word is fetched a new code is generated and compared to the stored code.
  - No errors detected.
  - An error is detected and it is possible to correct the error.
  - An error is detected, but it is not possible to correct it.

Hamming Error correcting code

- It is the simplest of all error correction codes.
- The figure uses Venn diagrams to illustrate the use of this code on 4-bit words (M=4).
- With 3 intersecting circles there are seven compartments.
- We assign the 4 data bits to the inner compartments. (a)



Contd.

- The remaining compartments are filled with parity bits.
- Each parity bit is chosen so that the total number of 1s in the circle is even. (b)
- Because circle A contains 3 data 1s, the parity bit in the circle is set to 1.
- Now if error changes one of the data bits (c), it is easily found.
- By checking the parity bits, discrepancies are found in circle A and circle C but not in circle B. Only one of the seven compartments is in A and C but not B. (d)
- The error can therefore be corrected by changing that bit.

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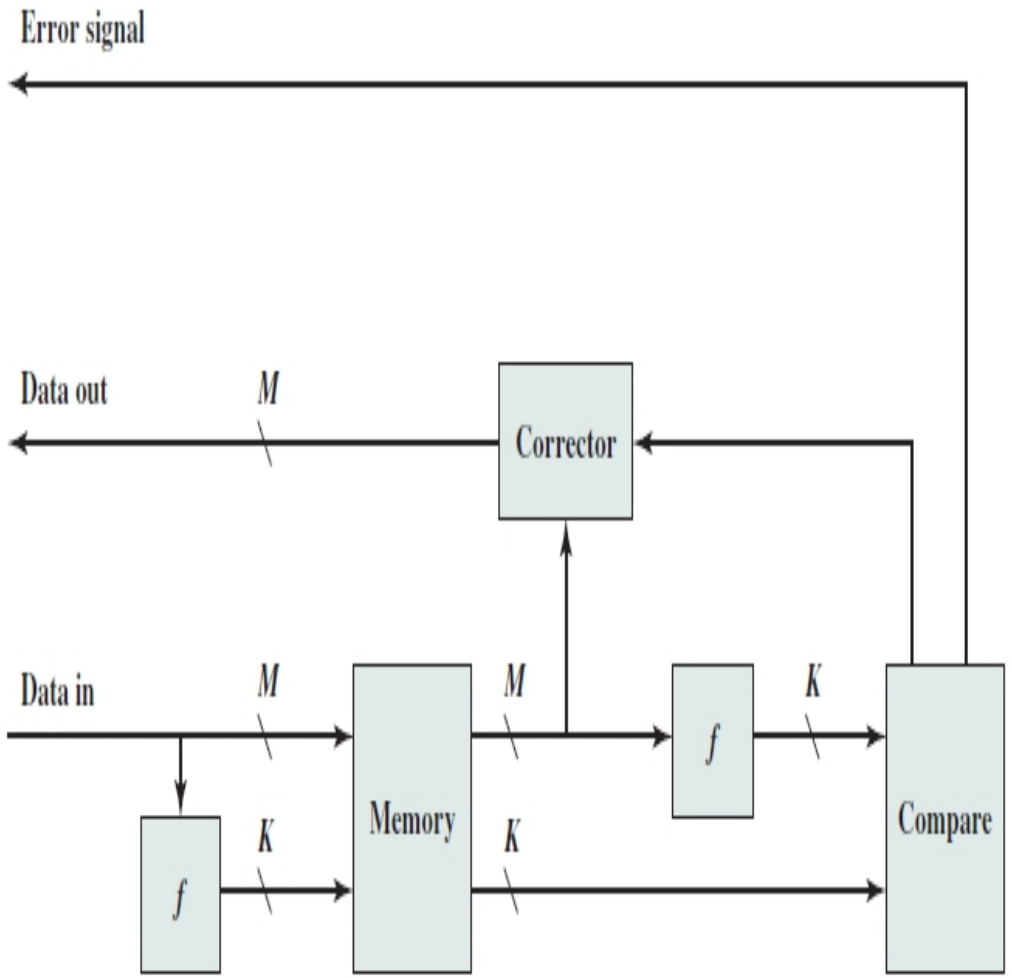
- The comparison logic receives as input two K-bit values.
- A bit-by-bit comparison is done by taking the exclusive-OR of the two inputs.
- The result is called the syndrome word.
- Thus, each bit of the syndrome is 0 or 1 according to if there is or is not a match in that bit position for the two inputs.
- The syndrome word is therefore K bits wide and has a range between 0 and (2^k-1).
- Now because an error could occur on any of the M data bits or K check bits, we must have

$$2^k - 1 \geq M + K$$



Data bits and check bits

- Data bits and check bits

Data Bits	Check Bits
8	4
16	5
32	6
64	7
128	8
256	9

M=8,K=3,K=4
$2^k-1 \geq M+K$
$2^3-1 < 8+3$
$2^4-1 > 8+4$

THANK YOU