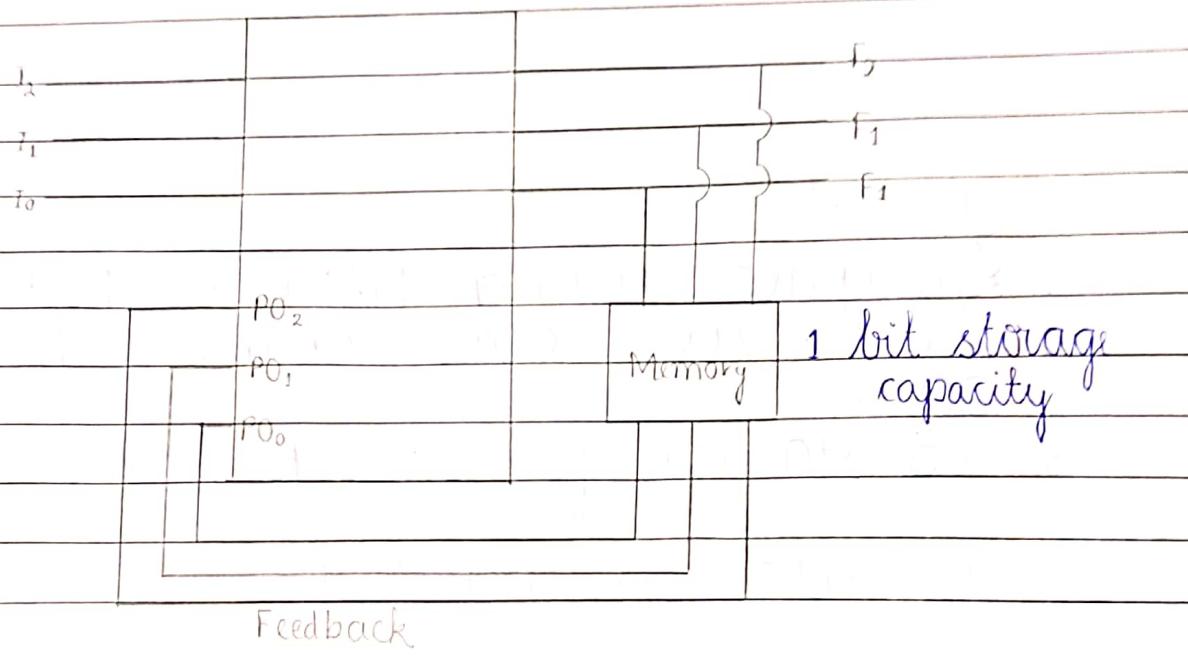


Sequential Circuit

- * flip-flops
- * counters
- * registers

Sequential circuit is a circuit where present output depends on present input as well as past outputs.

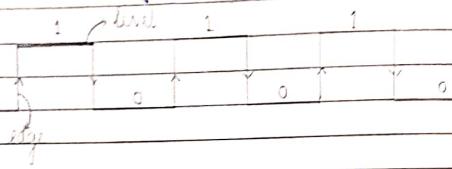


* Combinational + memory = sequential

latch and flip flop

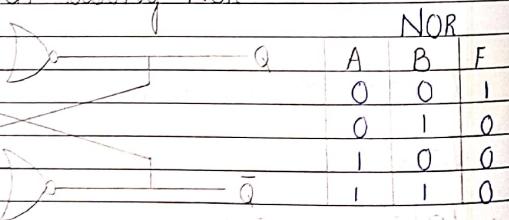
1. Latch is the basic storage element.
2. It stores only a single bit.
3. A storage element in digital circuit can maintain a binary state indefinitely until either power off or directed by input to change / switch off state.

- SR is a level sensitive circuit whereas flip-flops are edge sensitive
- (+ve or -ve edge)
- Storage element that operates with signal value on latch whereas controlled by clock transition is flip-flop



- SR latch
- 1. Designed using NAND or NOR gates
- 2. Needs two cross-coupled NAND/NOR gates
- 3. S stands for set, R for reset

SR latch using NOR



Case -1 : $R = 1, S = 0$

$$Q = 0, \bar{Q} = 1$$

Next instance : $R = 0, S = 0$ } memory
 $Q = 0, \bar{Q} = 1$

* prev output = new output. Behaves as memory

Case 2 : $R = 0, S = 1$

$$Q = 1, \bar{Q} = 0$$

Next instance : $R = 0, S = 0$
 $Q = 1, \bar{Q} = 0$

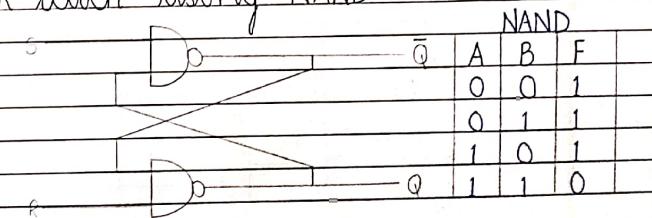
Case 3 : $R = 1, S = 1$

$$Q = 0, \bar{Q} = 0 \rightarrow \text{not possible}$$

Next instance : $R = 0, S = 0$ } doesn't work as memory
 $Q = 1, \bar{Q} = 1$

S	R	Q	\bar{Q}
0	0	Prev Q	Prev \bar{Q}
0	1	0	1
1	0	1	0
1	1	-	-

SR latch using NAND



Case 1 : $R = 1, S = 0$

$$Q = 1, \bar{Q} = 0$$

Next instance : $R = 1, S = 1$
 $Q = 1, \bar{Q} = 0$

Case 2 : $S = 1, R = 0$

$$\bar{Q} = 0, Q = 1$$

Next instance : $S = 1, R = 1$

$$Q = 0, \bar{Q} = 1$$

Case 3 : $S = 0, R = 0$

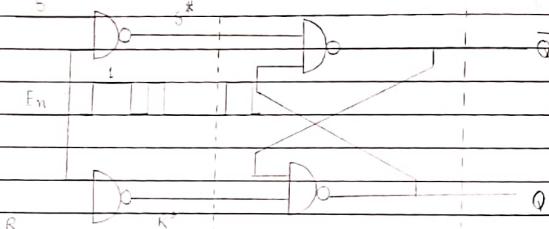
$$Q = 1, \bar{Q} = 1$$

- not possible
Next instance : $S = 1, R = 1$ → indeterminate
not used / forbidden

S	R	Q	\bar{Q}
0	0	-	-
0	1	0	1
1	0	1	0
1	1	Prev	Prev

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SR latch with control (enable input)



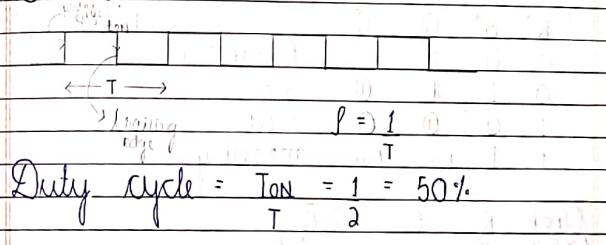
S*	R*	Q	\bar{Q}
0	0	-	-
0	1	0	1
1	0	1	0
1	1	Prev	Prev

En	S	R	O/P
0	x	x	no change
1	0	0	no change
1	0	1	$Q = 1, \bar{Q} = 0$ (Set)
1	1	0	$Q = 0, \bar{Q} = 1$ (Reset)
1	1	1	forbidden

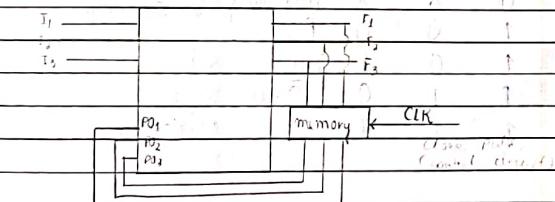
Enable (control) is a level triggered signal

In SR flip-flop enables will be replaced by clocks

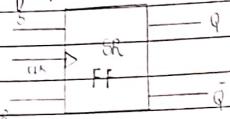
Clocks



$$\text{Duty cycle} = \frac{T_{on}}{T} = \frac{1}{2} = 50\%$$

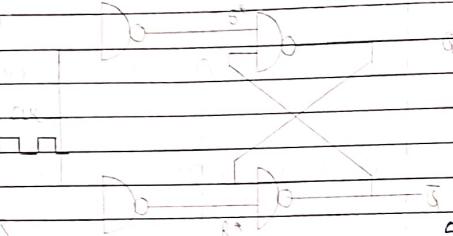


SR flip-flops



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S*	R*	Q	\bar{Q}
0	0	-	-
0	1	0	1
1	0	1	0
1	1	Prev	Prev

$S^* = \overline{(S \cdot \bar{R} \cdot \bar{Q})}$
 $R^* = \overline{(R \cdot \bar{S} \cdot Q)}$

Clock	S	R	Q, \bar{Q}
0	X	X	memory } no change
1	0	0	Prev
1	0	1	$Q=0, \bar{Q}=1$ set
1	1	0	$Q=1, \bar{Q}=0$ reset
1	1	1	- forbidden

Clock	S	R	Q, \bar{Q}	Q_{n+1}
0	X	X	memory	Q_n
1	0	0	memory	Q_n
1	0	1	$Q=0, \bar{Q}=1$	0
1	1	0	$Q=1, \bar{Q}=0$	1
1	1	1	not used	forbidden

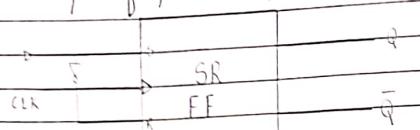
Characteristics table

Q_n	S	R	Q_{n+1}	Q_{n+1}	SR
0	0	0	0	00	
0	0	1	0	0	
0	1	0	1	0	
0	1	1	x	11	
1	0	0	1	1	
1	0	1	0	1	
1	1	0	1	Q _{n+1} = S + Q _n R	
1	1	1	x	1	

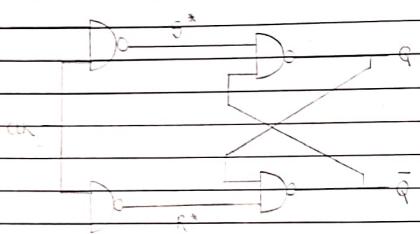
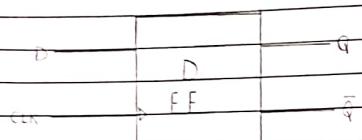
Excitation table

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D-Flip-flop



D-Flip-flop using SR flip-flop



Truth-table

Clock	D	$Q \& \bar{Q}$	Q_{n+1}
0	X	memory	Q_n
1	0	$Q=0 \bar{Q}=1$	0
1	1	$Q=1 \bar{Q}=0$	1

Characteristics Table

Q_n	D	Q_{n+1}	Q_{n+1}
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	2

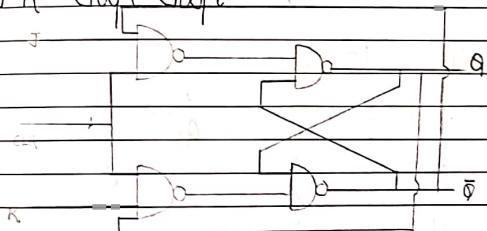
$Q_{n+1} = D$

Excitation table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

3-01-22

J-K Flip Flop



CLK	J	K	Q_n
0	X	X	Memory (Q_n)
1	0	0	Memory (Q_n)
1	0	1	0
1	1	0	1
1	1	1	-X (Joggle) (Q_n)

Assume: $Q = Q_n$, $\bar{Q} = \bar{Q}_n$
 $Q = 0, \bar{Q} = 1$

$J = K = CLK = 1$

$Q = 1, \bar{Q} = 0$

Characteristic Table

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Excitation Table

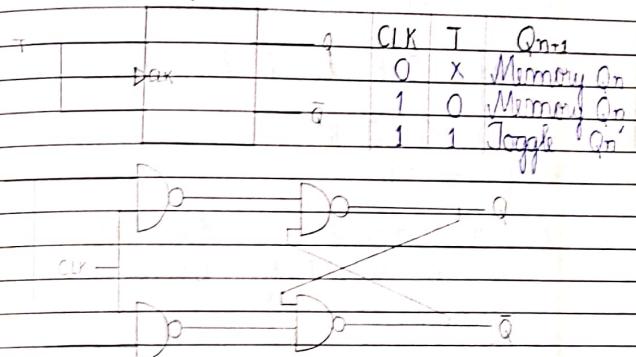
Q_n	Q_{n+1}	J	K	Q_n	Q_{n+1}
0	0	0	X	0	0
0	1	1	X	0	1
1	0	X	1	1	X
1	1	X	0	1	X

$Q_n = 0, 1$
 $K = \bar{Q}_{n+1}$

T	Q _n	Q _{n+1}	Q _{n+1}
0	0	1	0
1	1	1	1
1	1	1	1

$Q_{n+1} = K'Q_n + JQ_n'$

T Flip-Flop



Characteristics Table Excitation Table

T	Q_n	Q_{n+1}	Q_n	Q_{n+1}	T
0	0	0	0	0	0
0	1	1	1	1	1
1	0	1	1	0	0
1	1	0	0	1	1

Flip-flop conversions

- 1 Identify available & required flip-flop
- 2 Draw characteristic table of required
- 3 Draw excitation table for available flip-flop
- 4 Write excitation expression for required
- 5 Draw circuit diagram
- 6 Convert J-K to D flip-flop

Available - J-K

Required - D

Characteristics

Characteristics			Excitation					
Q_n	D	Q_{n+1}	J	K	Q_n	Q_{n+1}	J	K
0	0	0	0	X	0	0	0	X
0	1	1	1	X	0	1	1	X
1	0	0	X	1	1	0	X	1
1	1	1	X	0	1	1	X	0

D
J
K
O/P

$$D = K$$

1

1

J	Q_n	1	K	Q_n	X	X
X	X		X	X		1

$J = D$

$K = D'$

Convert SR to T flip-flop

Available - SR

Required - T

Characteristics

Characteristics			Excitation		
T	Q_n	Q_{n+1}	Q_n	Q_{n+1}	S R
0	0	0	0	0	X
0	1	1	1	1	X 0
1	0	1	0	1	0 1
1	1	0	1	0	1 0

S	Q_n	X	R	Q_n	X
T	Q_n		T	Q_n	

$$S = TQ_n'$$

$$R = TQ_n$$

Introduction to state table, state diagram and state equation

State table
State table is like a truth-table which provides relationship between present state, next state and input-output.

State diagram

Graphical representation of state table

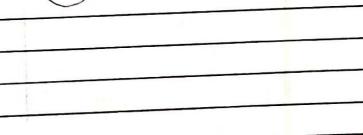
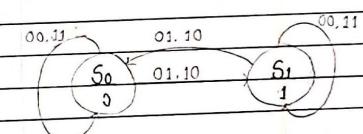
State table

P.S	X	N.S	Y
$Q_3(4)Q_2(3)Q_1(2)$	X	$Q_3(4)Q_2(3)Q_1(2)$	$\frac{S_1}{S_0}$
$Q_3(1)Q_2(0)$	0	1	10
01	0	01	1
		$\frac{S_0}{S_0}$	($\frac{S_1}{10}$)

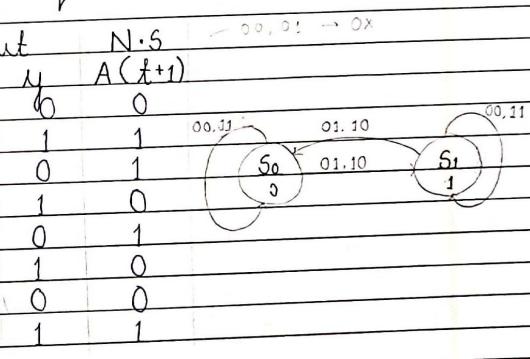
Present State	Input	Next State	Output
$A(t)$	x	y	$A(t+1)$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Present State	Input	Next State	Output
$A(t)$	x	y	$A(t+1)$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$00, 01 \rightarrow 0X$



Seq circuit (D+FF)



$00, 11 \rightarrow 01, 10$

Mealy and Moore State Machines

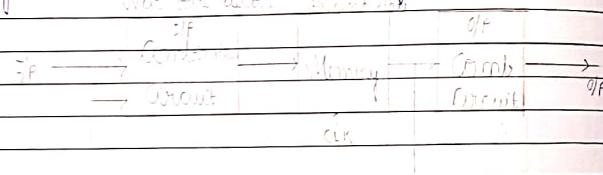
There are two models developed for representing sequential circuit

1. Moore state machine
2. Mealy state machine

State machine identification is based on how output is produced

1. Moore State Machine

Output is a function of present state only and independent of input



Q

$$Y_1 = AB \\ \Rightarrow \text{Moore model}$$

$$\begin{aligned} T - FF \\ Q(t+1) = T \oplus Q \end{aligned}$$

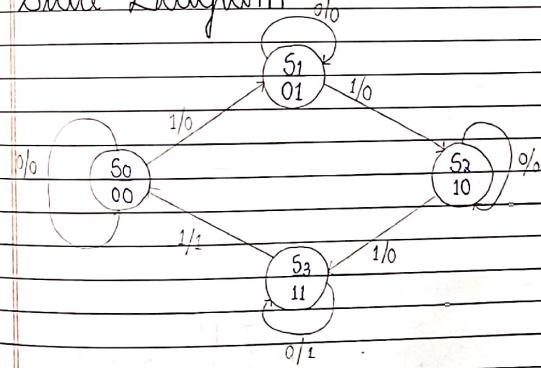
From the circuit

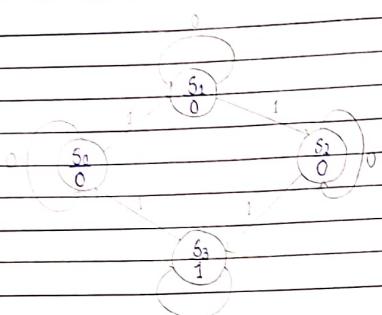
$$T_A = Bx \quad T_B = x$$

$$\begin{aligned} A(t+1) &= T_A \oplus A \\ &= Bx \oplus A \\ B(t+1) &= T_B \oplus B \\ &= x \oplus B \end{aligned}$$

P.S	I/P	N.S	O/P
A	B	X	A(t+1)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	0	1	1
1	1	0	1
1	1	1	1

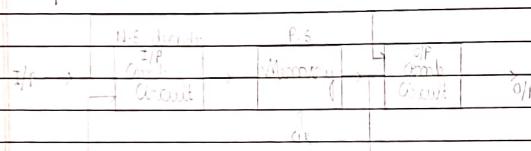
State Diagram





Mealy State Machine

Output depends on present state & input



Q.

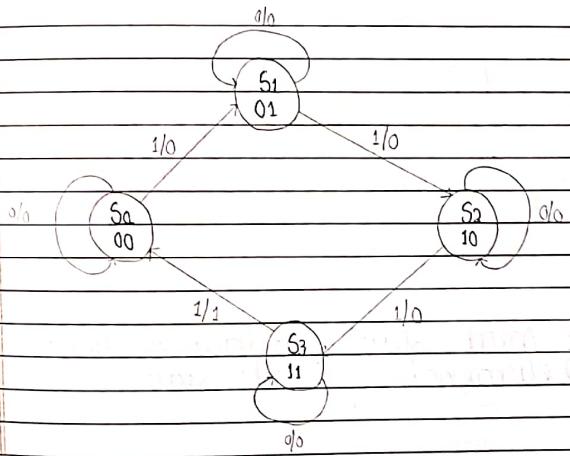
$$T\text{-FF}$$

$$Q(t+1) = T \oplus Q(t)$$

$$\begin{aligned} T_A &= Bx \\ T_B &= Ax \\ y &= ABx \end{aligned}$$

$$\begin{aligned} A(t+1) &= T_A \oplus A \\ &= Bx \oplus A \\ B(t+1) &= T_B \oplus B \\ &= Ax \oplus B \end{aligned}$$

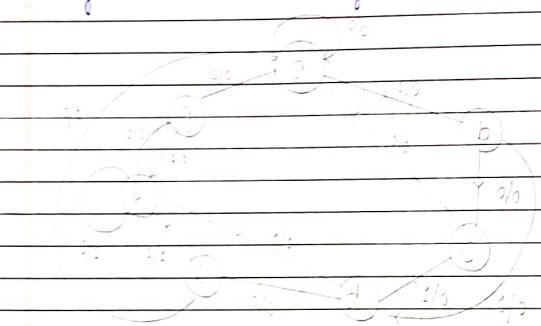
P.S	T/P	N.S	O/P
A 0 0	B 0 0	A(t+1) B(t+1) 0 0	y d
0 0 1	0 1 0	0 1 1	0
0 1 0	0 1 1	0 1 0	0
0 1 1	1 0 0	1 0 1	0
1 0 0	1 0 1	1 1 0	0
1 0 1	1 1 0	1 1 1	0
1 1 0	1 1 1	1 1 0	0
1 1 1	0 0 1	0 0 1	1



State reduction and assignment

State table

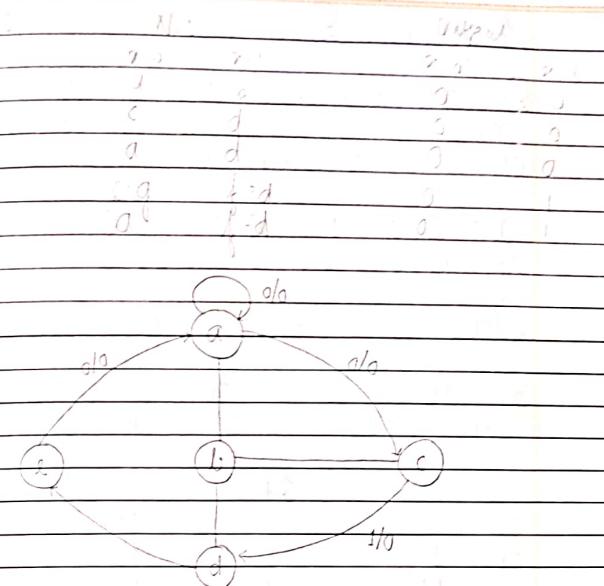
P.S	N.S	Output	
		$x=0$	$x=1$
a	a	b	0 0
b	c	d	0 0
c	a	d	0 0
d	e	f	0 1
e	a	f	0 1
f	b	f	0 1
g	a	b	0 1



* If next state & output is same we can eliminate present state

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Date _____
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Design procedure for clocked sequential circuit

- From word description and specification of desired operation derive state diagram
- Reduce no. of states

Sequence Detector

Design sequence detector to detect 3 or more consecutive 1's in string of bits coming through input line

$$x = 00111011110$$

$$y = 00001000110$$

Start with state S_0 , rest state

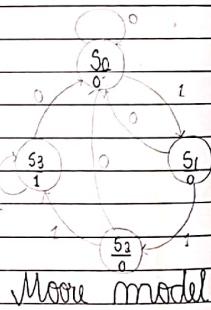
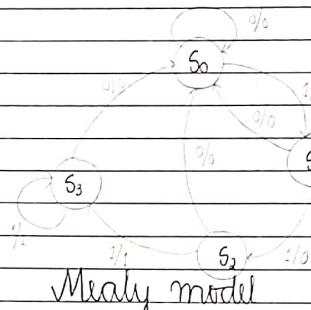
If input is 0, circuit stays in S_0 but if input is 1 it goes to S_1

S_0 rest

S_1 1 1 1 ...

S_2 11 11 1 ...

S_3 111 111 ...



State table

		x	Q _A	Q _B	N.S.	O/P	N.S.	O/P
Q _A	Q _B		0	0	0	0	0	0
0	0		0	1	0	1	0	0
0	1		1	0	0	0	0	0
0	1		1	1	0	1	0	0
1	0		0	0	0	0	0	0
1	0		1	1	1	1	1	0
1	1		0	0	0	0	0	1
1	1		1	1	1	1	1	1

Mealy model

Moore model

$$Q_A' = Q_B x + Q_A x$$

Q _A	Q _B x	00	01	11	10
0				1	
1			1	1	1

Q _A	Q _B x	00	01	11	10
0				1	
1			1	1	1

$$Q_B' = Q_B x + Q_A x$$

Q _A	Q _B x	00	01	11	10
0				1	
1			1	1	1

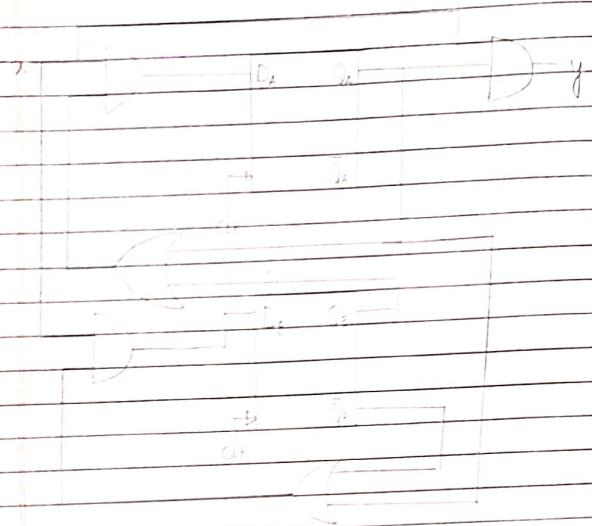
Q _A	Q _B x	00	01	11	10
0				1	
1			1	1	1

$$y = Q_A x$$

Mealy Model

$$D_A = Q_A +$$

$$D_B = Q_B +$$



Meine Modell

$$D_A = Q_A +$$

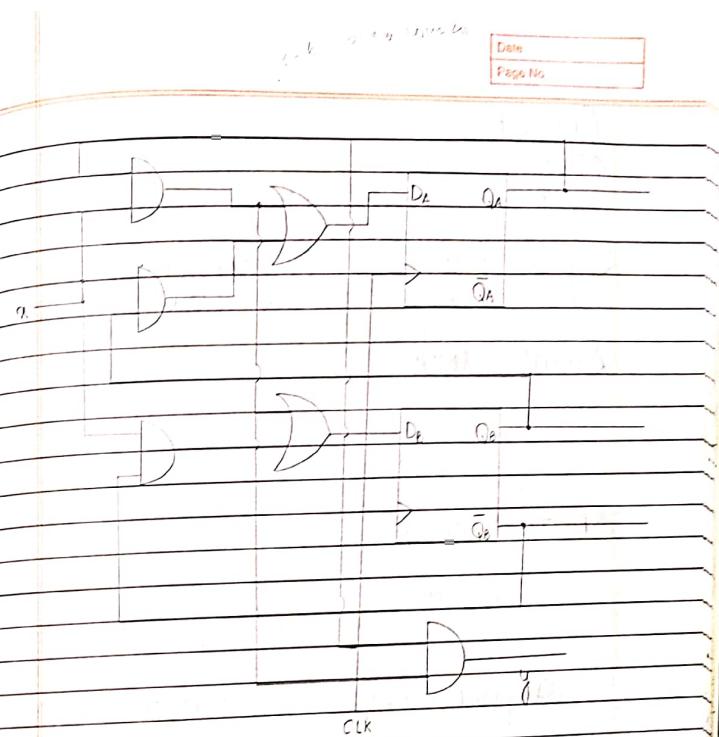
$$= Q_A S + Q_B S$$

Q_A	Q_B	S	Q_A'	Q_B'	Y
0	0	0	0	0	0
0	1	1	1	0	0
1	0	1	0	1	0
1	1	0	1	1	1

$$D_B = Q_B +$$

$$= Q_A S + Q_B S$$

$$Y = Q_A Q_B$$

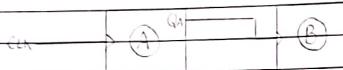


Counters

Special type of sequential circuit used to count pulses

- Types :
1 Ripple / Asynchronous counter
2 Synchronous counter

Serial clock



Parallel clock



Asynchronous

Synchronous

- 1 Flip-flops are connected. There's no connection such that o/p of first bit "o/p" of first FF and FF drives clock of next clock of next FF
- 2 FFs are not clocked. FFs are clocked simultaneously
- 3 Circuit is simple for circuit becomes complicated more no. of states as no. of states increase
- 4 Space is slow as clock is space is high as clock propagated through no. given of same time of stage

Counters (contd.)

Up counters

0-1-2-

Down counters

7, 6, 5, ... 0

Up/Down

Asynchronous Counters

1 Up - counter

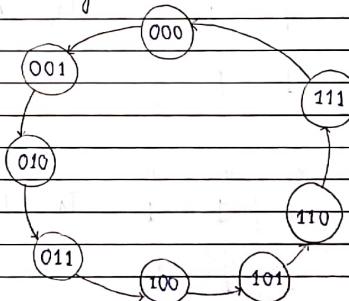
2 Down - counter

3 Ripple up / down

Design of 3-bit binary up counter (synchronous)

An m-bit binary counter consists of m-FF that can count in binary from 0 to $2^n - 1$.

State diagram



State table

A_2	A_1	A_0	A_2	A_1	A_0	FF inputs
I/P (P.S)			O/P (N.S)			T_{A_2} T_{A_1} T_{A_0}
0	0	0	0	0	1	0 0 1
0	0	1	0	1	0	0 1 1
0	1	0	0	1	1	0 0 1
0	1	1	1	0	0	1 1 1
1	0	0	1	0	1	0 0 1
1	0	1	1	1	0	0 1 1
1	1	0	1	1	1	0 0 1
1	1	1	0	0	0	1 1 1

T_{A_2}

$A_2 A_0$

A_2 00 01 11 10

$$T_{A_2} = A_1 A_0$$

0

1

T_{A_1}

$A_1 A_0$

A_2 00 01 11 10

$$T_{A_1} = A_0$$

0

1

T_{A_0}

$A_1 A_0$

A_2 00 01 11 10

$$T_{A_0} = 1$$

0

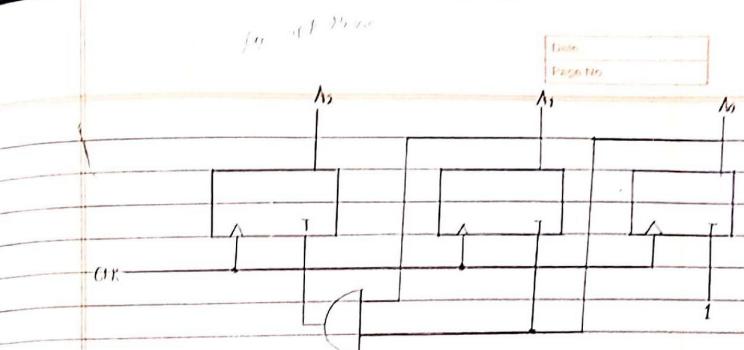
1

A_2

$A_1 A_0$

A_2 00 01 11 10

$$T_{A_2} = A_1' A_0'$$



3-bit synchronous down counter

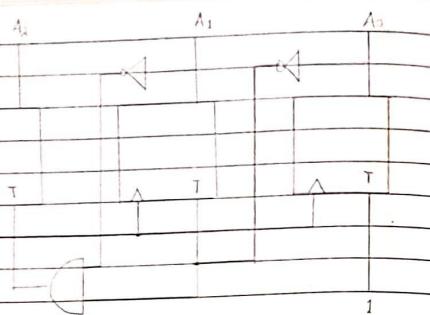
A_2	A_1	A_0	A_2	A_1	A_0	FF inputs
I/P (P.S)			O/P (N.S)			T_{A_2} T_{A_1} T_{A_0}
0	0	0	1	1	1	1 1 1
1	1	1	1	1	0	0 0 1
1	1	0	1	0	1	0 1 1
1	0	1	1	0	0	0 0 1
1	0	0	0	1	1	1 1 1
0	1	1	0	1	0	0 0 1
0	1	0	0	0	1	0 1 1
0	0	1	0	0	0	0 0 1

A_2	A_1	A_0	A_2	A_1	A_0
0	1				
1	1				

$$T_{A_2} = A_1' A_0'$$

A_2	A_1	A_0	A_2	A_1	A_0
0	1				
1	1				

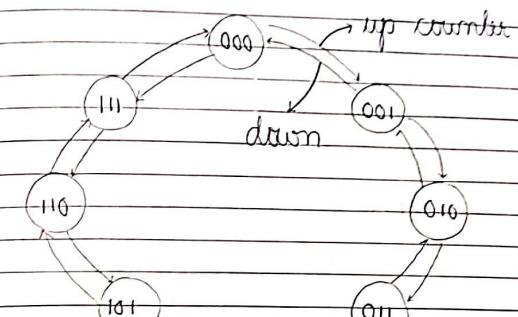
$$T_{A_1} = A_0'$$



12-1-22

3-bit up/down counter

T/P	O/P	FF inputs	Count
C	A2 A1 A0	A2 A1 A0 TA2 TA1 TA0	111 count
0	0 0 0	0 0 1 0 0 1	
0	0 0 1	0 1 0 0 1 1	
0	0 1 0	0 1 1 0 0 1	up count
0	0 1 1	1 0 0 1 1 1	
0	1 0 0	1 0 1 0 0 1	TA
0	1 0 1	1 1 0 0 1 1	101001
0	1 1 0	1 1 1 0 0 1	TA 10101
1	0 0 0	1 1 1 1 1 1	111111
1	1 1 1	1 1 0 0 0 1	101000
1	1 1 0	1 0 1 0 1 1	110101
1	1 0 1	1 0 0 0 0 1	101000
1	0 0 0	0 1 1 1 1 1	111101
1	0 1 1	0 1 0 0 0 1	101000
1	0 1 0	0 0 1 0 1 1	110101
1	0 0 1	0 0 0 0 0 1	101000

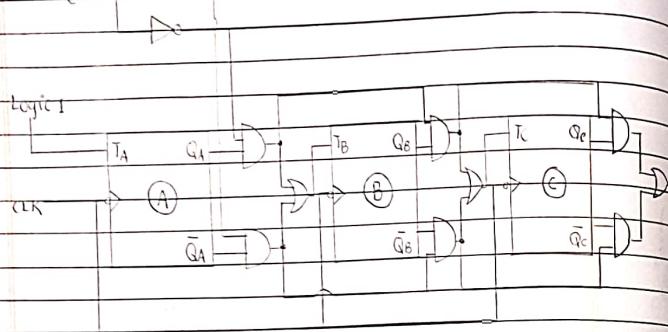


CA2	TA2	TA1	00	01	11	10	CA2	TA2	TA1	00	01	11	10
00	00	00	1				00	00	00	1			
01	01	01		1			01	01	01		1		
11	11	11			1		11	11	11		1		
10	10	10				1	10	10	10		1		1

$$T_{A_2} = CA_1'A_0' + C'A_1A_0 \quad T_{A_1} = C'A_0 + CA_0' \\ = C \oplus A_0$$

CA2	TA2	00	01	11	10	CA2	TA2	00	01	11	10
00	00	1	1	1	1	00	00	1	1	1	1
01	01	1	1	1	1	01	01	01	1	1	1
11	11	1	1	1	1	11	11	11	1	1	1
10	10	1	1	1	1	10	10	10	1	1	1

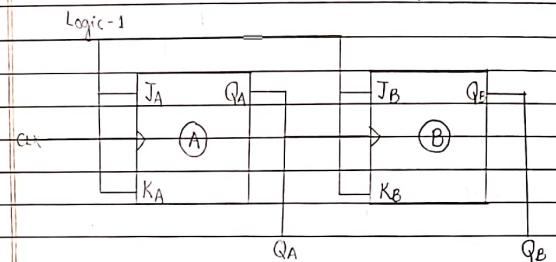
$$T_{A_0} = 1$$



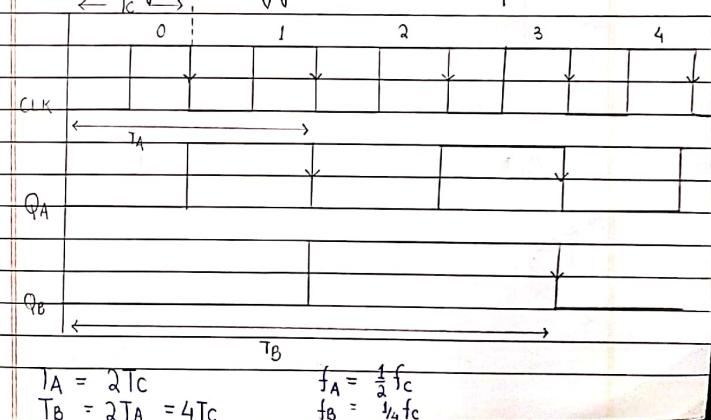
Asynchronous counter as frequency divider

Asynchronous counter will work as frequency divider

Minimum two flip-flops are needed



* Ripple counters are designed using -ve edge triggered clock pulse



$$T_A = 2T_C$$

$$T_B = 2T_A = 4T_C$$

$$f_A = \frac{1}{2} f_C$$

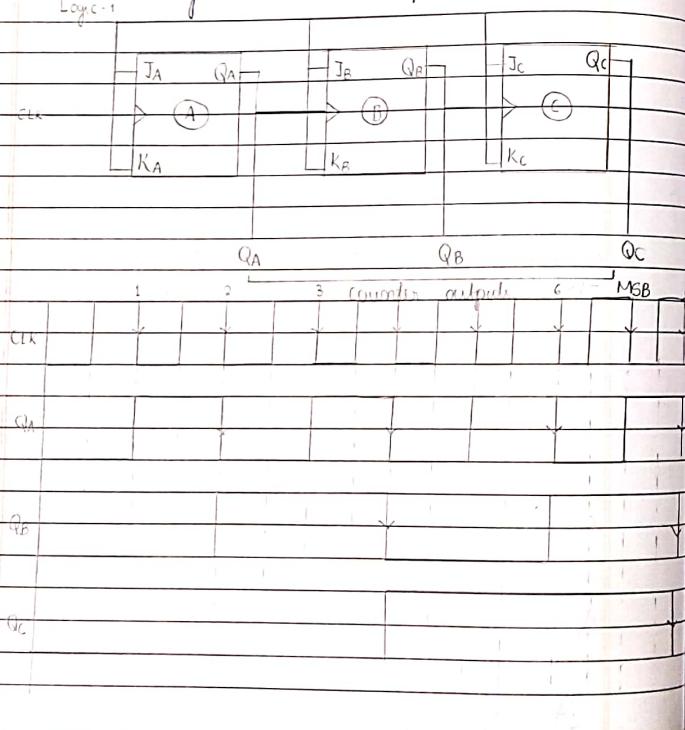
$$f_B = \frac{1}{4} f_C$$

For N FF's final frequency is clock frequency divided by 2^{2^n} i.e.

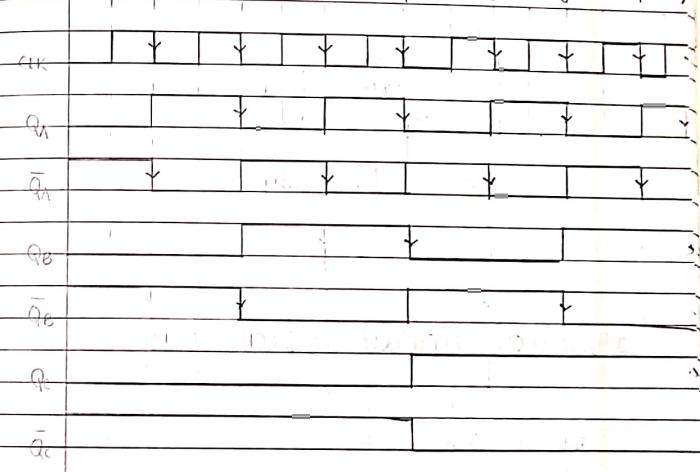
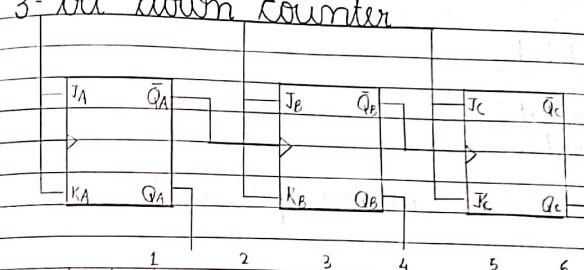
$$f_o = \frac{f_c}{2^2} = \frac{f_c}{4}$$

* This also works as 2-bit up counter

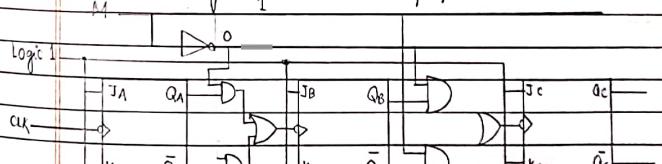
3-bit asynchronous up counter



3-bit down counter



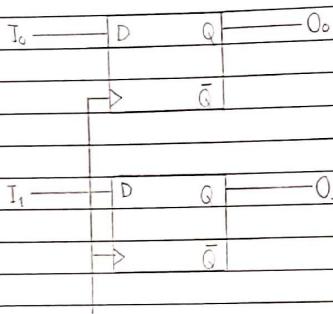
3-bit up/down ripple counter



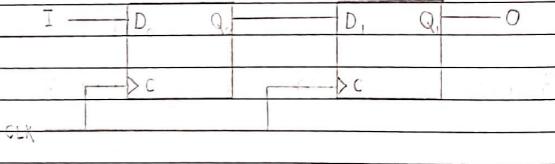
Shift Register

1. PIPLO
2. SISO
3. SIPO
4. PIPO

1. Parallel input parallel output



2. Serial input serial output



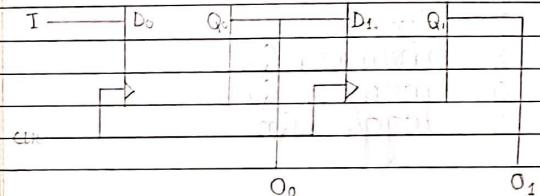
Date 17 - 01 - 23
Page No.

$SJ = 2^{b+1} + 1 \rightarrow d/2^b$

Date _____
Page No. _____

Initial	Q ₀	Q ₁
1st clock	0	X
2nd clock	1	0
3rd clock	X	1

3. Serial input parallel output

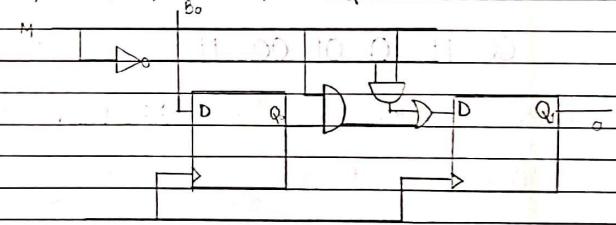


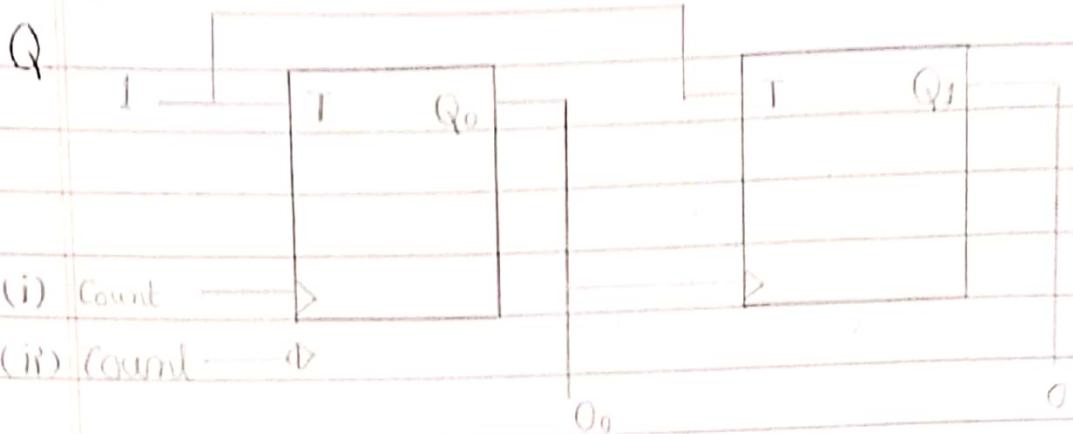
4. Parallel input serial output

$M = 0$ load $M = 1$ shift
Data B, Q

$$Y = \bar{M}B + MQ$$

$$M = 0, Y = B ; M = 1, Y = Q$$





Initially $Q_1 Q_0 = 00$

CLK	T	Q_{n+1}
0	X	memory Q_n
1	0	memory Q_n
1	1	toggle Q_n'

