

Ansl:-

Difference between Sequential, Direct & Random Access:-

SEQUENTIAL:- Access is made in a specific linear sequence; shared read-write mechanism is used and this must be moved from its correct location to the desired location; passing & rejecting each intermediate method. Thus, the time to access an arbitrary record is highly variable. eg: Tape

DIRECT:- It involves a read-write mechanism; however individual blocks or records have a unique address based a physical location; access is accompanied by direct access to reach a general vicinity plus sequential searching counting or waiting to reach the final location access time is variable. eg: Disk Unit

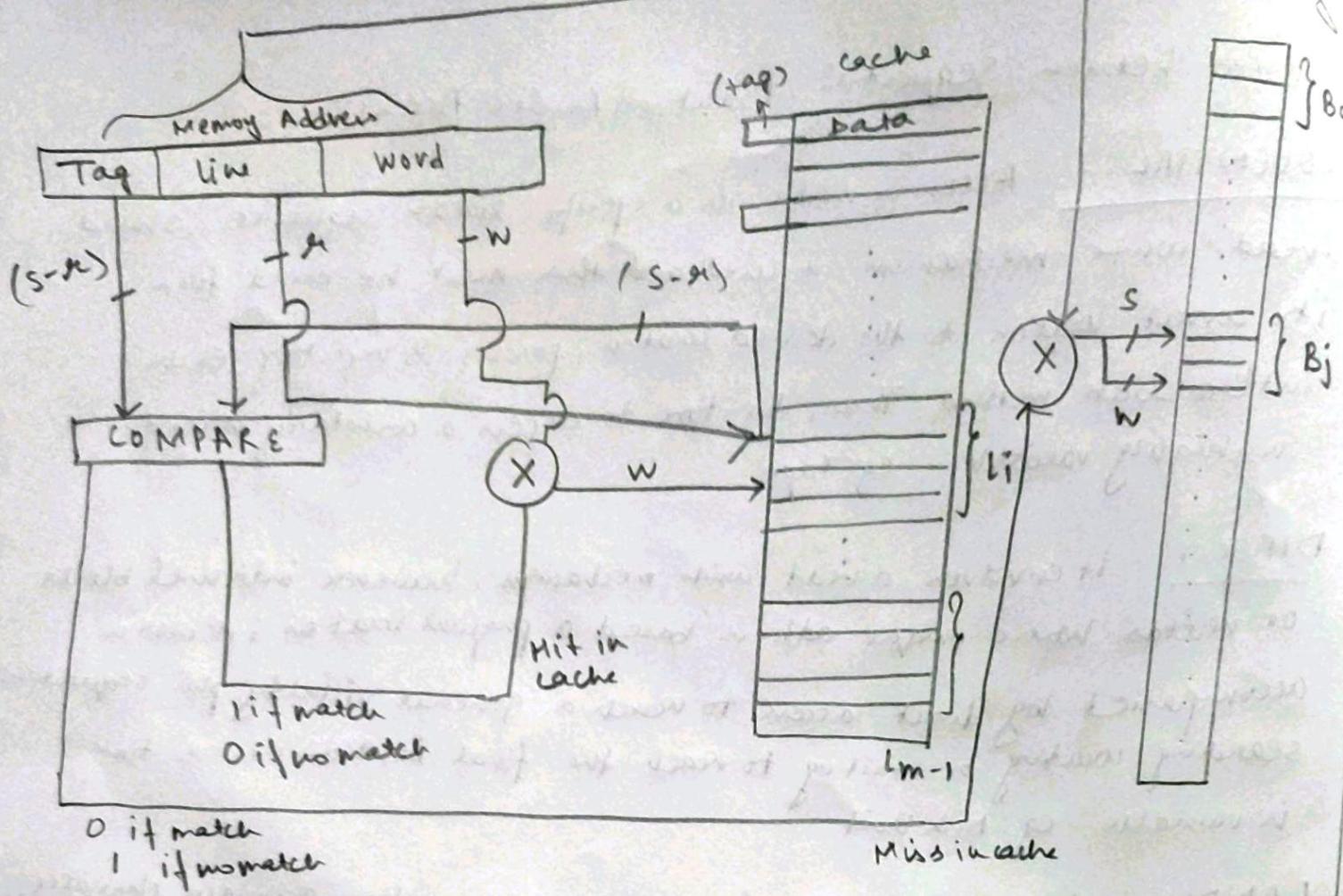
RANDOM:- Each addressable location in memory has a unique physically-wired in addressing mechanism, the time to access a given location is independent of the sequence of prior access & is constant. Any location can be selected at random & directly addressed & accessed. eg: Main memory & Cache memory.

Ansl:-

Difference between Direct Mapping & Associative Mapping

DIRECT MAPPING:- The simplest technique known as direct mapping; each block of main memory into one possible cache line. The mapping is expressed as  $i = j \bmod m$ .

(DIRECT MAPPING CACHE ORGANIZATION)  
↓ Fig (next page)



- ① Address length =  $(S+W)$  bits
- ② no. of addressable units =  $2^{S+W}$  words / bytes
- ③ Block size = line size =  $2^W$  words
- ④ no. of blocks =  $\frac{2^{S+W}}{2^W} = 2^S$
- ⑤ no. of blocks in cache =  $M = 2^R$
- ⑥ size of cache =  $2^{R+W}$  words / bytes
- ⑦ size of tag =  $(S-W)$  bits

ASSOCIATIVE MAPPING :- Associative mapping overcomes the disadvantage of direct mapping by permitting each main memory block to be loaded into any line of the cache. In this case, the cache control logic interprets a memory address as a tag & word field. The tag field uniquely identifies a block of main memory to determine whether a block is in the cache; the cache control logic must simultaneously examine to determine every's line tag for a match.

Ans 3:-

These are the access methods:-

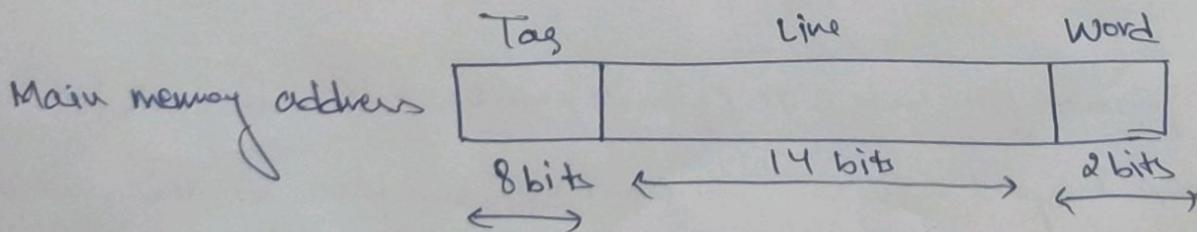
SEQUENTIAL: Access is made in a specific linear sequence; a shared read-write mechanism is used and this must be moved from its correct location to the desired location; passing and rejecting each intermediate method. Thus, the time to access an arbitrary record is highly variable.

DIRECT: It involves a read-write mechanism; however individual blocks or records have a unique address based on physical address location; access is accomplished by direct access to reach a general vicinity plus sequential searching counting on waiting to reach the final location access time is variable.

RANDOM ACCESS: Each addressable location in memory has a unique physically-wired-in addressing mechanism, the time to access a given location is independent of the sequence of prior access & is constant. Any location can be selected at random & directly addressed & accessed.

ASSOCIATIVE: This is a random access type of memory that enables one to make a comparison of desired big locations within a word for a specified match and to do this for all a portion of its contents rather than its address. The retrieval time is constant rather than its address independent local or prior access pattern.

Ans 4:- For direct mapping cache, the memory address is divided into Tag, line & word.



Tag: A unique identifier for a group of data, because different regions of memory may be mapped into the block, the tag is used to differentiate between them.

Line: The line field defines the cache line where the memory line should reside.

Word: Word field selects one from among all the addressable words in a line.

Ans: - Number of blocks = Cache size / block size

$$\frac{32 \text{ kb}}{32} = 1024 \text{ bytes}$$

So indexing requires 10 bits, no. of offset bit to access the 32 bit block is 5. So no. of tag bits =  $32 - 10 - 5 = 17$ .

So it is 10, 17 (a)

Ans: -

Ans 7:

## DRAM

stands for Dynamic RAM (DRAM). It stands for Static RAM (SRAM).

is made with cells that stores data as charge on capacitors, the presence or absence of capacitors is interpreted as binary 1 & 0.

- ① Volatile; continuous power supply is needed to preserve the bit values
- ② DRAM is smaller & simpler, thus less expensive & more dense
- ③ DRAM tend to be favoured for large memory requirements
- ④ SRAM is faster than DRAM
- ⑤ DRAM is used for main memory

## SRAM

It is a digital device that uses the same logic elements used in processors, binary values are stored using traditional flip-flop logic gate configurations.

- ⑥ Volatile; power is continuously needed to preserve the bit values
- ⑦ More complex as compared to DRAM, in comparison more expensive.
- ⑧ Favoured for small memory requirements
- ⑨ Faster in speed
- ⑩ SRAM is used for cache memory (both on & off chip).

Ans 8: Types of ROM (Read Only Memory)

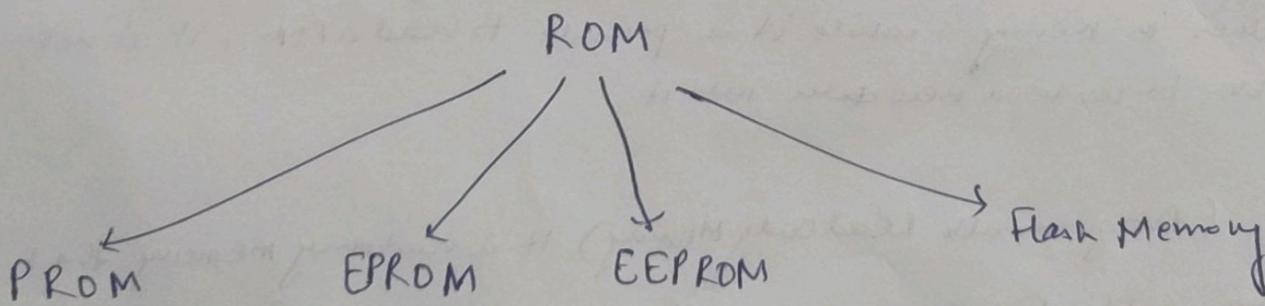
ROM: contains a permanent pattern of data that cannot be changed. A ROM is non-volatile; no power source is required to maintain the bit values in memory, while it is possible to read a ROM, it is not possible to write a new data into it.

PROM: (Programmable Read Only Memory) It is read only memory that can be modified only once by the user. The user buys a blank PROM & desired contents using a PROM programmer. Inside PROM chips, there are small chips/fuses which are burned open during programming. It can only be programmed once. Provides flexibility & convenience, non-volatile & is less expensive.

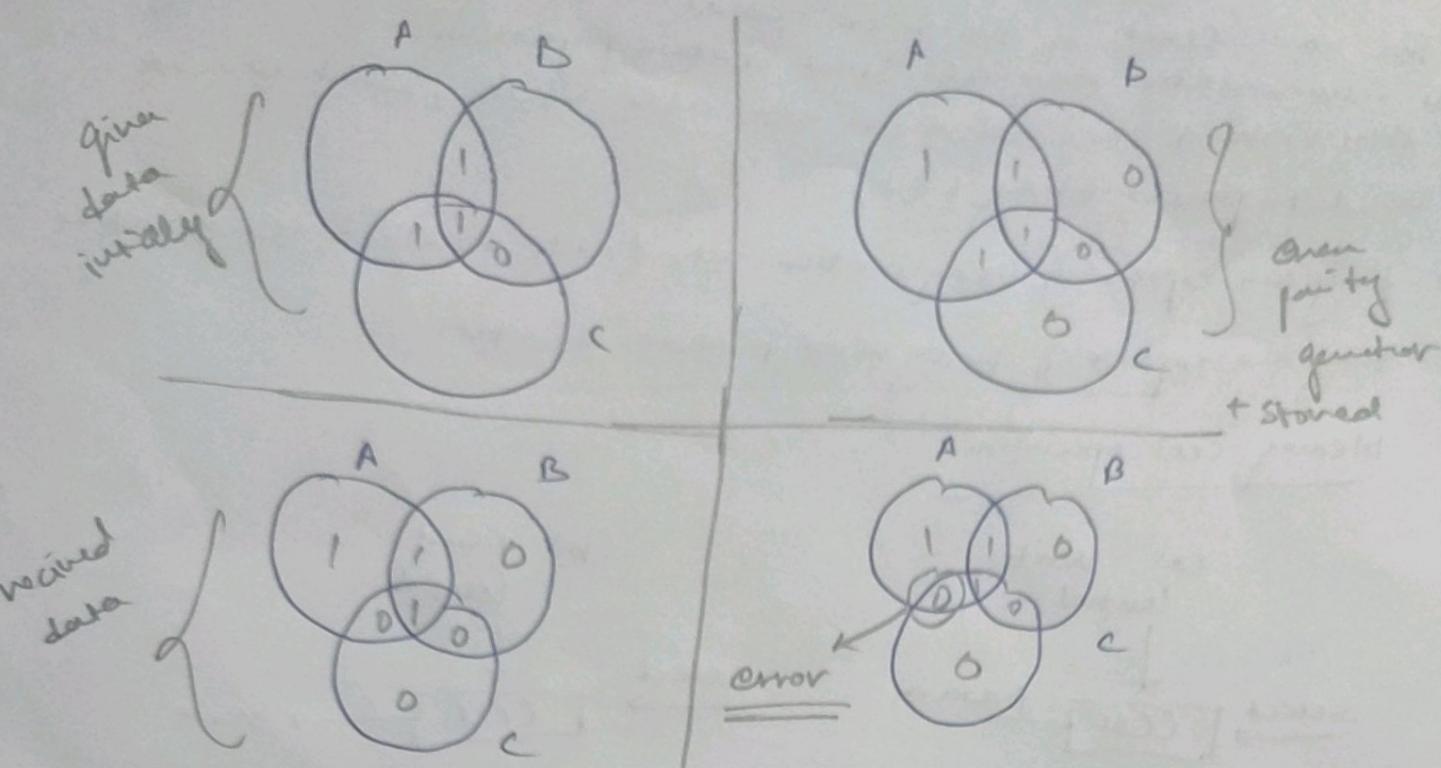
EPROM: (Erasable PROM) It can be erased by exposing it to UV light for a duration of no minutes. It is erased & written electrically, as with PROM. Before a write operation, all the storage cells must be cleared/exposed to the same initial state by exposure of the packaged chip to UV. EPROM can be altered many times & like ROM & EEPROM holds its data indefinitely. More expensive than PROM but allows multiple update capability.

EEPROM: (Electrically Erasable & PROM) It is a read mostly memory that can be written into at anytime without erasing prior contents; only bytes addresses are updated. Write operation takes longer than read operation. It combines the advantage of non-volatility with flexibility of being updatable in place, using bus control, address & data lines. More expensive than EPROM.

Flash memory: Intermediate between EEPROM & EEPROM. It uses an electrical erasing technology. It is possible to erase a block rather than an entire chip. It does not provide byte-level erasure. Like EEPROM it uses only one transistor per bit & so achieves high level density.



### Hamming



It uses Venn - diagram to illustrate the use of this code on 4 bit ( $M=4$ ) with three intersecting circles & seven components. We assign 4 data bits to the inner components & rest are filled by 'parity bits'. Parity is chosen such that the total no. of 1's is even in a circle.

Now, it is easier to find the if error changes one bit. Then by checking with parity values stored, the error can be corrected by changing that bit.

A bit by bit comparison is done by taking XOR, the result is called syndrome word, then each bit of the syndrome is 0 or 1.

$$2^k - 1 \geq M+k ; \text{ tell me how many check bits are required.}$$

if syndrome contains all '0' then no error.

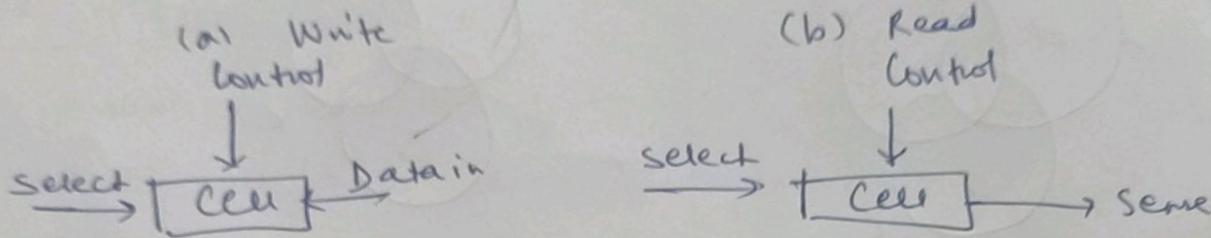
if syndrome contain 1 in one of the checked bit then no correction

if syndrome contains 1 in equal more than two places , the data bit is inverted for correction.

Ans 10:- Semiconductor memory organization:-

- The basic element of the semiconductor memory is the memory cell.
- All semiconductor memory cells share certain properties:-
- they exhibit two stable (or semi-stable) states, which can be used to represent binary 1 & 0.
  - they are capable of being written into (at least one), to set the state.
  - they are capable of being read to sense the state.

Memory cell operation:



Ans 11:- We need  $(2)^{10}$  outputs to map 1 kb RAM.

For this we need  $10 \times 2^{10}$  decoders.

$$\text{Hence } m = 10$$

$$n = 2^{10}$$

$$m+n = 10+4. (b)$$

Ans 12:-

Stored word       $\begin{smallmatrix} 8 & 7 & 6 & 5 & 4 & 3 & 2 & 1 \\ | & | & 0 & 0 & 0 & 0 & 1 & 0 \end{smallmatrix}$

$$2^k - 1 \geq M + k \cdot n$$

$$2^8 - 1 \geq 12 + 4 \cdot 8$$

$$C_4 = 0 \oplus 0 \oplus 1 \oplus 1$$

$$0 \oplus (2) \oplus -1 \oplus 1$$

$$8+4 = 12 \quad 2 \times 2 \times 2 \times 2 - 1$$

$$= 15 > 12$$

$$C_1 : D_1 \oplus D_2 \oplus D_4 \oplus D_5 \oplus D_7 = 0$$

$$(k=4)$$

$$C_2 : D_1 \oplus D_3 \oplus D_4 \oplus D_6 \oplus D_7 = 1$$

$$C_4 : D_2 \oplus D_3 \oplus D_4 \oplus D_8 = 0 \quad C_2 \quad 0 \oplus 0 \oplus 0 \oplus 0 \oplus 1$$

$$C_8 : D_5 \oplus D_6 \oplus D_7 \oplus D_8 = 0 \quad 0 \quad 0 \quad 1 \quad 1$$

$$C_1 = 0 \oplus 1 \oplus 0 \oplus 0 \oplus 1 \quad 0 \oplus 1 \oplus 0$$

$$C_3 = 1 \oplus 0 \oplus 0 \oplus 1 \quad 1 \oplus 0 \oplus 1 \oplus 0$$

Bit Position:	12	11	10	9	8	7	6	5	4	3	2	1
Date bit :	D8	D7	D6	D5	D4	D3	D2	D1	C4	C2	C1	
Check bit :					C8							
Word stored:	0	1	0	0	0	0	0	1	0	1	1	0

Ans 3:- Given 8 bit word    00 111 001  
                             b7 654 321

$$\text{Parity calculated} = \begin{matrix} 0 & 1 & 1 & 1 \\ 2^3 & 2^2 & 2^1 & 2^0 \end{matrix}$$

Word now:    D8 D7 D6 C8 D4 D3 D2 C4 D1 C - C1  
                   0 0 1 1 0 1 0 0 1 1 1 1

Word fetched: 00 1 1 1 1 0 0 1 0 1 0 1  
                   (1101)  
                   3421

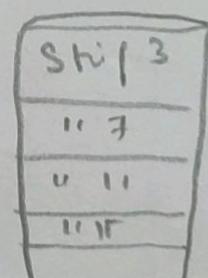
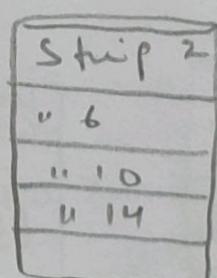
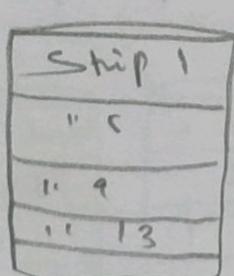
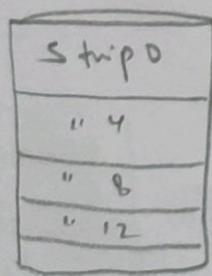
Doing XOR

$$\begin{array}{r} 0 \ 1 \ 1 \ 1 \\ 1 \ 1 \ 0 \ 1 \\ \hline 1 \ 0 \ 1 \ 0 \end{array} \rightarrow \text{error in bit } 10 \text{ D}$$

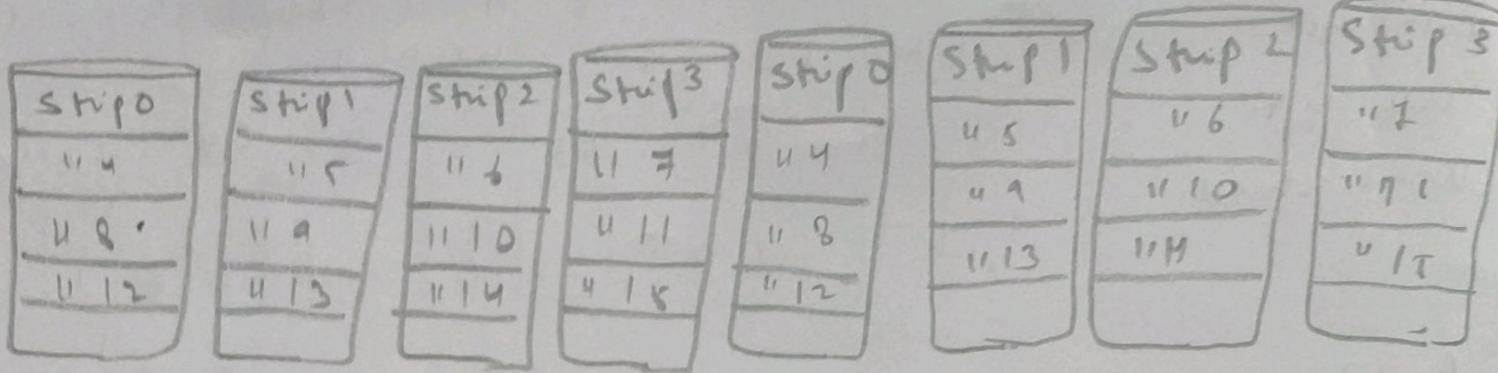
hamming word

Thus, data read from memory was 000 11001.

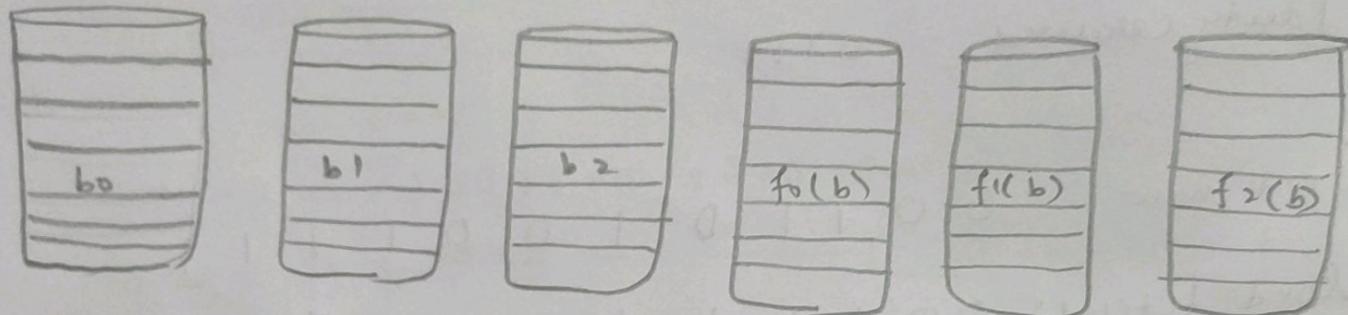
Ans 4:- RAID '0' (non redundant)



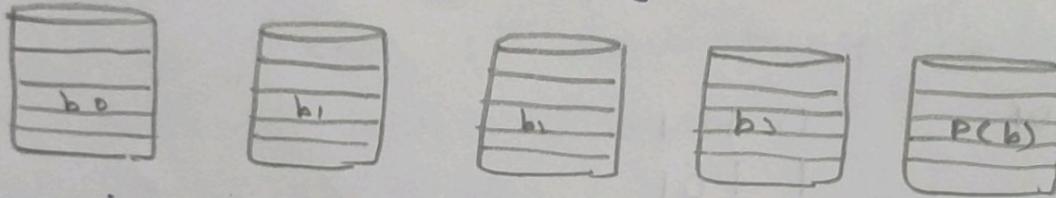
RAID '1' (Mirrored)



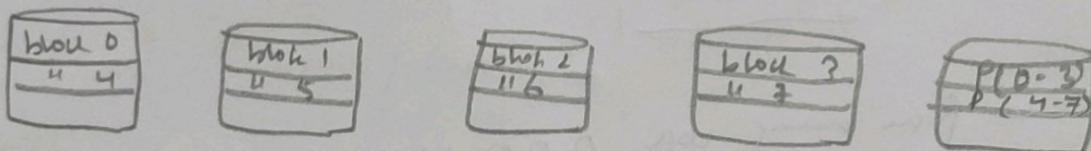
RAID '2' (Redundancy through Hamming code)



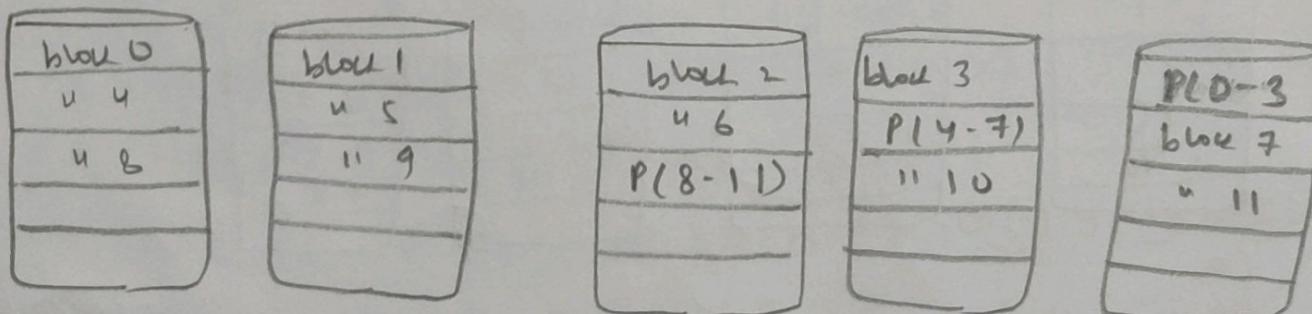
RAID '3' (Bit interleaved parity)



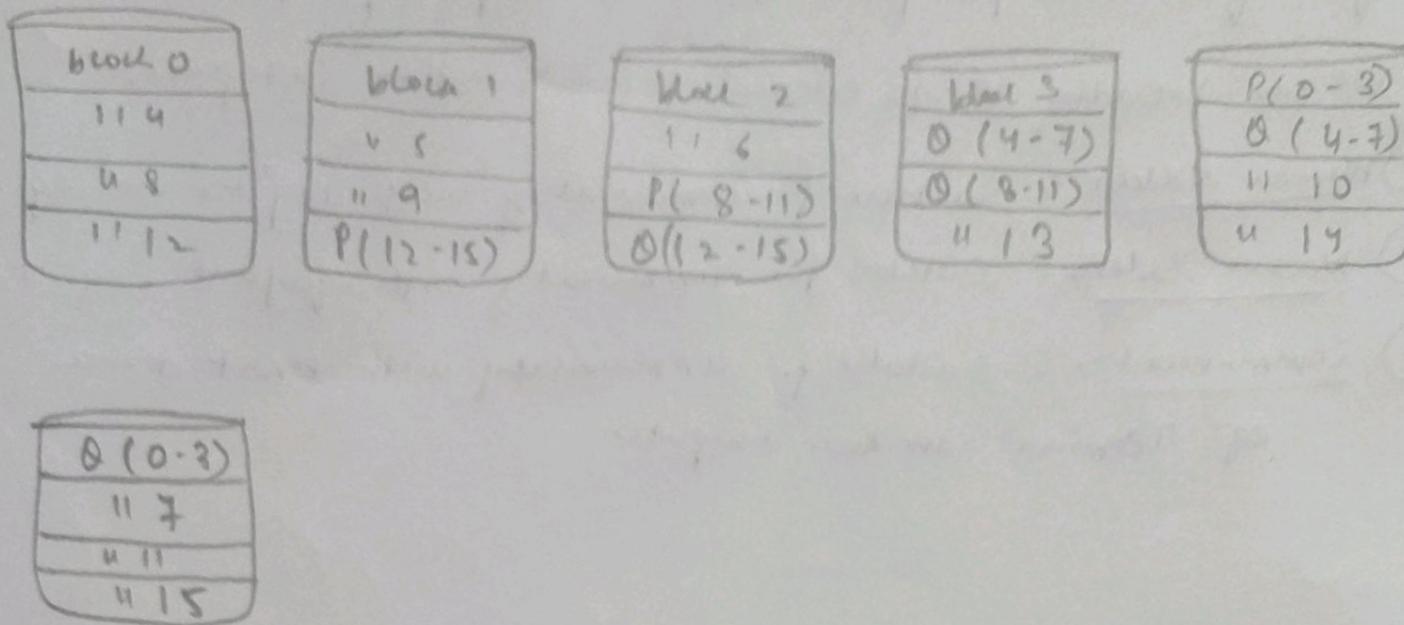
RAID '4' (Block level parity)



RAID '5' (Block level distributed parity)



## RAID '6' ( Dual Redundancy)



Ans 15:- Raid configuration of disks is used to provide fault tolerance . RAID disks is a disk subsystem that stores your data across multiple disks to either increase performance or provide fault tolerance to your system.

Fault tolerance is the property that enables a system to continue operating properly in the event of the failure of some of its components. The ability of maintaining functionality when portions of a system break down is referred to as graceful degradation. (a)

Ans 16:- I/O module contains logic for performing a communication function between peripheral & the bus.

This module has two major functions:

- (1) Interface to the processor & memory via the system bus or central switch
- (2) Interface to one or more peripheral devices by tailored data links.

Ans 17:- An external device connected to an I/O module is often referred to as peripheral device or simply a peripheral.

We can broadly classify external devices into three categories:-

- ① Human readable: Suitable for communicating with computer over. e.g. VDU
- ② Machine readable: Suitable for communicating with equipment. e.g. Tape
- ③ Communication: Suitable for communicating with remote devices.  
e.g. Terminal, another computer.