Computer Organization and Architecture (EET 2211)

Chapter 3
A Top-Level View of Computer Function and Interconnection

Interconnection Structures

- A computer consists of a set of components or modules of three basic types (processor, memory, I/O) that communicate with each other.
- In effect, a computer is a network of basic modules.
- Thus, there must be paths for connecting the modules.
- The collection of paths connecting the various modules is called the *interconnection structure*.
- The design of this structure will depend on the exchanges that must be made among modules.

Computer Modules

- Fig.1. shows the types of exchanges that are needed by indicating the major forms of input and output for each module type.
- The wide arrows represent multiple signal lines carrying multiple bits of information in parallel.
- Each narrow arrow represents a single signal line.

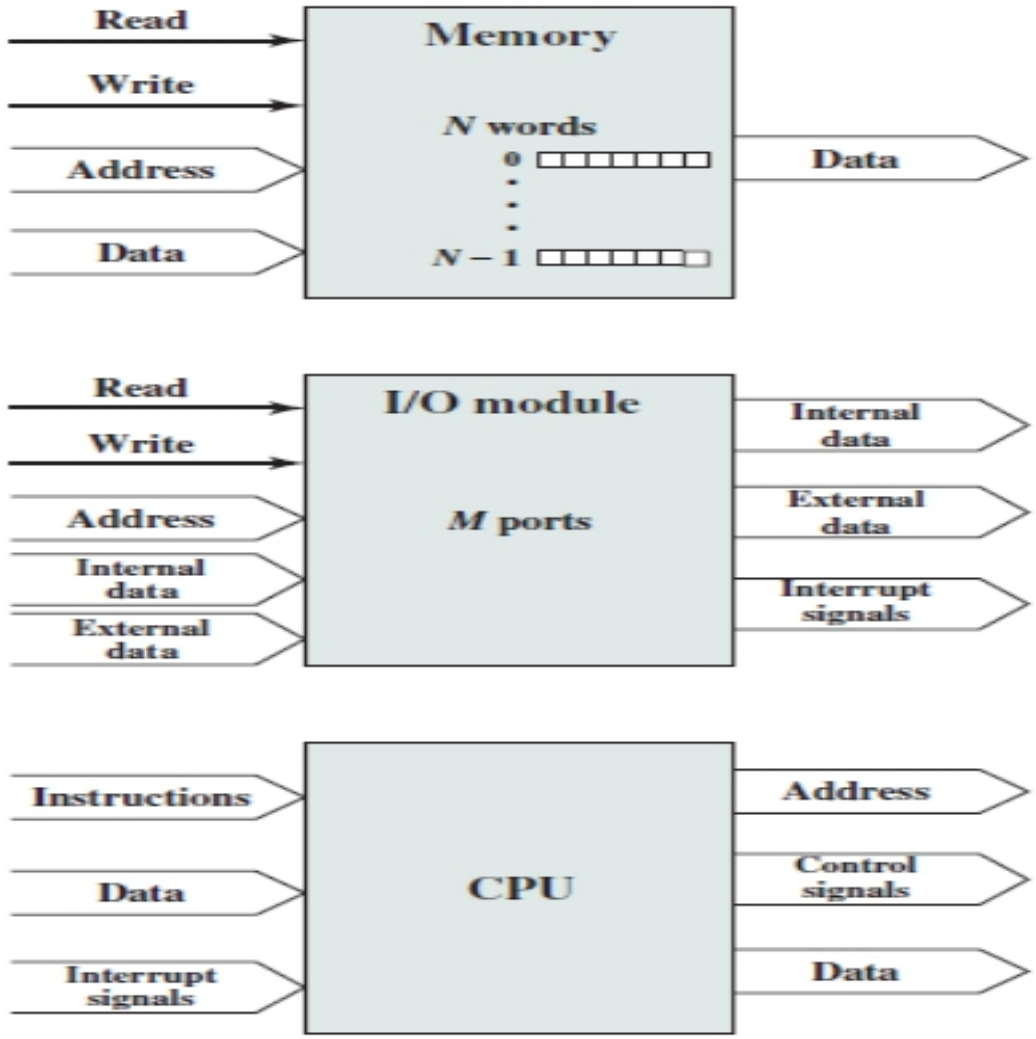

Fig.1. Computer Modules

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- **Memory:**
- Typically, a memory module will consist of *N* words of equal length.
- Each word is assigned a unique numerical address (0, 1,……., *N*-1).
- A word of data can be read from or written into the memory.
- The nature of the operation is indicated by read and write control signals.
- The location for the operation is specified by an address.

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- **I/O module:**
- From an internal (to the computer system) point of view, I/O is functionally similar to memory.
- There are two operations; read and write.
- An I/O module may control more than one external device.
- Each of the interfaces to an external device is referred as a *port* which is assigned with a unique address (e.g., 0, 1,…….,*M*-1).
- Also, there are external data paths for the input and output of data with an external device.
- An I/O module may be able to send interrupt signals to the processor.

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- **Processor:**

- The processor reads in instructions and data, writes out data after processing, and uses control signals to control the overall operation of the system.

- It also receives interrupt signals.

Types of transfers

- The interconnection structure must support the following types of transfers:
- **Memory to processor:** The processor reads an instruction or a unit of data from memory.
- **Processor to memory:** The processor writes a unit of data to memory.
- **I/O to processor:** The processor reads data from an I/O device via an I/O module.
- **Processor to I/O:** The processor sends data to the I/O device.
- **I/O to or from memory:** For these two cases, an I/O module is allowed to exchange data directly with memory, without going through the processor, using direct memory access.

Bus Interconnection

- A bus is a communication pathway connecting two or more devices.
- The bus is a shared transmission medium.
- Multiple devices connect to the bus, and a signal transmitted by any one device is available for reception by all other devices attached to the bus.
- If two devices transmit during the same time period, their signals will overlap and become garbled.
- Thus, only one device at a time can successfully transmit.

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- A bus consists of multiple communication pathways, or lines.
- Each line is capable of transmitting signals representing binary 1 and binary 0.
- Hence a sequence of binary digits can be transmitted across a single line.
- Taken together, several lines of a bus can be used to transmit binary digits simultaneously (in parallel).
- For example, an 8-bit unit of data can be transmitted over eight bus lines.

System Bus:

- Computer systems contain a number of different buses that provide pathways between components at various levels of the computer system hierarchy.

- A bus that connects major computer components (processor, memory, I/O) is called a **system bus**.

- The most common computer interconnection structures are based on the use of one or more system buses.

- A system bus consists around fifty to hundreds of separate lines. Each line is assigned a particular meaning or function.

Types of System Bus:

- Although there are many different bus designs, but on any bus the lines can be classified into three functional groups:

- Data lines

- Address lines, and

- Control lines.

Bus Interconnection Scheme

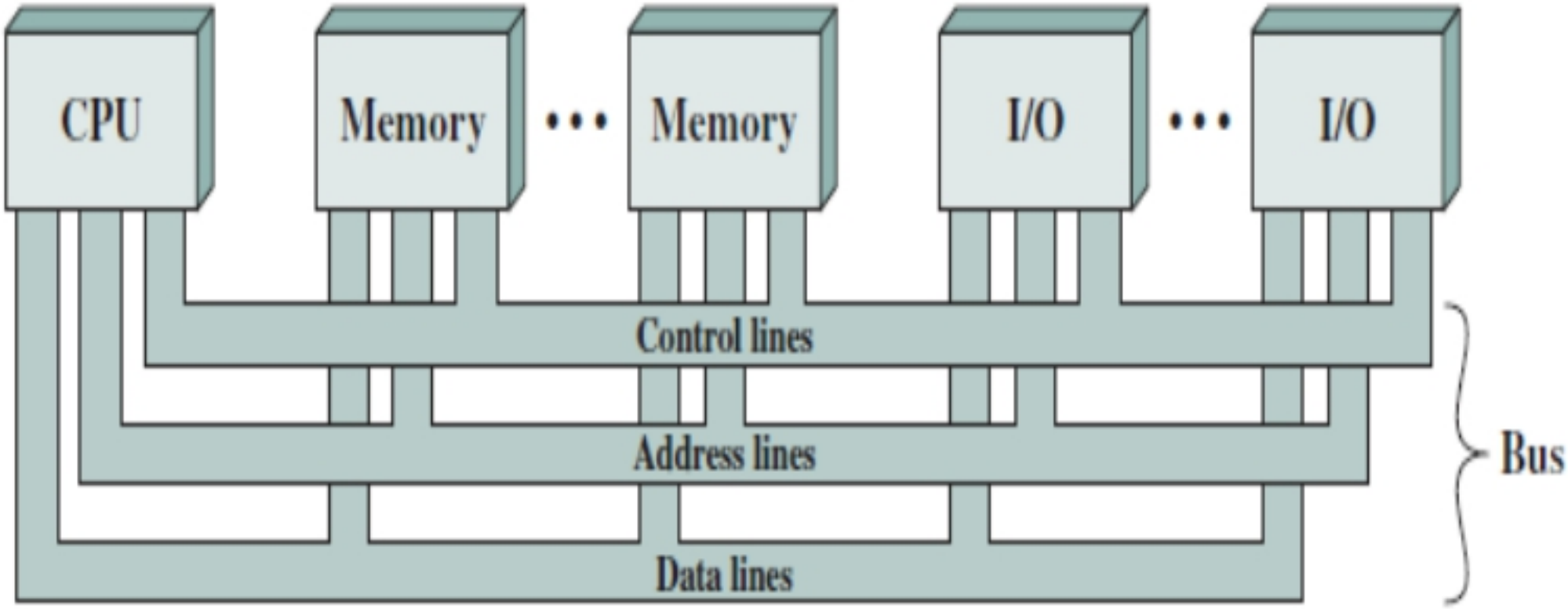

Fig.2. Bus Interconnection Scheme

Data lines:

- The **data lines** provide a path for moving data among system modules.
- These lines, collectively, are called the **data bus**.
- The data bus may consist of 32, 64, 128,or even more separate lines.
- The number of lines being referred to as the *width* of the data bus.
- Because each line can carry only one bit at a time, the number of lines determines how many bits can be transferred at a time.
- The width of the data bus is a key factor in determining overall system performance.
- For example, if the data bus is 32 bits wide and each instruction is 64 bits long, then the processor must access the memory module twice during each instruction cycle.

Address lines:

- The **address lines** are used to designate the source or destination of the data on the data bus.
- For example, if the processor reads a word (8, 16, or 32 bits) of data from memory, it puts the address of the desired word on the address lines.
- The width of the **address bus** determines the maximum possible memory capacity of the system.
- The address lines are generally also used to address I/O ports.
- Typically, the higher-order bits are used to select a particular module on the bus, and the lower-order bits select a memory location or I/O port within the module.

Control Lines:

- The **control lines** are used to control the access to and the use of the data and address lines.
- Because the data and address lines are shared by all components, there must be a means of controlling their use.
- Control signals transmit both command and timing information among system modules.
- Timing signals indicate the validity of data and address information.
- Command signals specify operations to be performed.

Typical control lines include:

- **Memory write:** causes data on the bus to be written into the addressed location.
- **Memory read:** causes data from the addressed location to be placed on the bus.
- **I/O write:** causes data on the bus to be output to the addressed I/O port.
- **I/O read:** causes data from the addressed I/O port to be placed on the bus.
- **Transfer ACK:** indicates that data have been accepted from or placed on the bus.

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- **Bus request:** indicates that a module needs to gain control of the bus.
- **Bus grant:** indicates that a requesting module has been granted control of the bus.
- **Interrupt request:** indicates that an interrupt is pending.
- **Interrupt ACK:** acknowledges that the pending interrupt has been recognized.
- **Clock:** is used to synchronize operations.
- **Reset:** initializes all modules.

Operation of the Bus

- The operation of the bus is as follows:
- If one module wishes to send data to another, it must do two things:

  (1) obtain the use of the bus, and

  (2) transfer data via the bus.
- If one module wishes to request data from another module, it must:

  (1) obtain the use of the bus, and

  (2) transfer a request to the other module over the appropriate control and address lines.
- It must then wait for that second module to send the data.

Thank You !