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COA Assignment 2

Q1 List and briefly define two approaches to dealing with multiple interrupt.

Soln The two approaches can be taken to dealing with multiple interrupt.

- Disabled interrupt (Sequential interrupts processing)
  i) Processor will ignore further interrupts while processing one interrupt.
  ii) Interrupts remain pending and are checked after first interrupt has been processed.
  iii) Interrupts handled in sequence as they occur.

- Define priorities (Nested interrupts processing)
  i) Low priority interrupts can be interrupted by high priority interrupts
  ii) When higher priority has been processed, processor return to previous interrupt.

Q2 List and briefly define the QPI protocol layers.

Soln QPI is defined as a four-layer protocol architecture which has the following layers:

1. Physical: Consists of the actual wires carrying the signals, as well as circuitry and logic to support necessary features required in the transmission and receipt of the 1s and 0s.

- Link: Responsible for reliable transmission and flow control. The Link layer's unit of transfer is an 80-bit Flit.
- Routing: Provides the framework for directing packets through the fabric.
- Protocol: The high-level set of rules for exchanging packets of data between devices. A packet is comprised of an integral number of Flits.

Q3 Consider a hypothetical 32-bit microprocessor having 32-bit instruction composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.

a) What is the maximum directly addressable memory capacity (in bytes)?

b) Discuss the impact on the system speed if the microprocessor bus has:
1. 32-bit local address bus and a 16-bit local data bus or
2. 16-bit local address bus and a 16-bit local data bus.

c) How many bits are needed for the program counter and the instruction register?

Soln a) The maximum directly addressable memory capacity in bytes is:

$$2^{(32-8)} = 2^{24} = 16777216 \text{ bytes} = 16 \text{ MB}$$

(8 bits = 1 byte for the opcode)

b).

1) A 32-bit local address bus and a 16-bit local data bus. Instruction and data transfers would take three bus cycles each one for the address and two for the data.

Since if the address bus is 32 bits, the whole address can be transferred to memory at once and decoded there; however, since the data bus is only 16 bits, it will require 2 bus cycles (access to memory) to fetch the 32 bit instruction or operand.

2) A 16-bit local address bus and a 16-bit local data bus. Instruction and data transfer would take four bus cycles each, two for the address and two for the data.

Therefore, that will have the processor to perform two transmissions in order to send to ~~money~~ memory the whole 32-bit address; this will require more complex memory interface control to latch the two halves of the address before it performs an access to it.

In addition to this two-step address issue, since the data bus is also 16 bit, the microprocessor will need 2 bus cycles to fetch the 32-bits instruction or operand.

c) For the PC needs 24 bits (24-bit address), and for the IR needs 32 bits (32 bit address).

4) For computers based on three-address field can be used to specify which of the following:

(S1) A memory operand
(S2) A processor register
(S3) An implied accumulator register.

A. Either S1 or S2
B. Either S2 or S3
C. Only S2 or S3
D. All of S1, S2, S3.

Soln In three address instruction formats, each address filled can specify a memory operand or a processor register.
But Accumulator register is implicitly used as destination address.

Option (A) Either S1 or S2.

5) A CPU has 24-bit instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in decimal)?

A. 400
B. 500
C. 600
D. 700.

Soln Each address is multiple of 3 as the starting address is 300 and is each instruction consists of 24 bits ie 3 bytes

Option (C) 600.

6) The most appropriate matching for the following pairs.

X : Indirect addressing. 1 : Loops
Y : Immediate addressing. 2 : Pointers
Z : Auto decrement addressing 3 : Constants.

Soln X-2, Y-3, Z-1

7) Consider the following sequence of micro-operations

MBR ← PC
MAR ← X
PC ← Y
Memory ← MBR

Which one of the following is a possible operation performed by this sequence?

A) Instruction Fetch
B) Operand Fetch
C) Conditional Branch.
D) Initiation of Interrupt Service.

Soln

MBR ← PC means the value of the program counter will get stored in MBR.

MAR ← X means some address value X is storing in MAR so to access memory location X

PC ← Y means storing new instruction value Y to the program counter to access new instruction.

Memory ← MBR means MBR register will store its value to Memory. This same the previous value of PC to memory.

This sequence of instructions matches with Interrupt Service Routine (ISR) since the sequence of instruction saved the address of current instruction into memory.

Ans = Option D (Initiation of interrupt service)

9) Write an assembly language code to find the lower nibble and higher nibble of a 8-bit number present in physical memory location 30500H and store the result in 30501H (lower nibble) and 30502H (higher nibble)

Soln

```
MOV AX, 0000H
MOV DS, AX
MOV AX, [30500H]
MOV CL, 04H
AND AL, 0FH
MOV AL, [30501H], AL
MOV AL, AH
AND AL, 0FH
MOV [30502H], AL
HLT
```

10) Write an assembly language code to perform the logical operations (AND, OR, XOR and NOT) on two 16 bit numbers.

Soln

```
MOV AX, [1000H]
MOV BX, [3000H]
MOV CX, [5000H]
MOV DX, [7000H]
AND AX, BX
OR CX, BX
XOR DX, BX
NOT BX
HLT
```