COMPUTER ORGANIZATION AND ARCHITECTURE (COA)

EET 2211
4TH SEMESTER – CSE & CSIT
CHAPTER 5, LECTURE 21

INTERNAL MEMORY

TOPICS TO BE COVERED

- Semiconductor Main Memory
- Error Correction

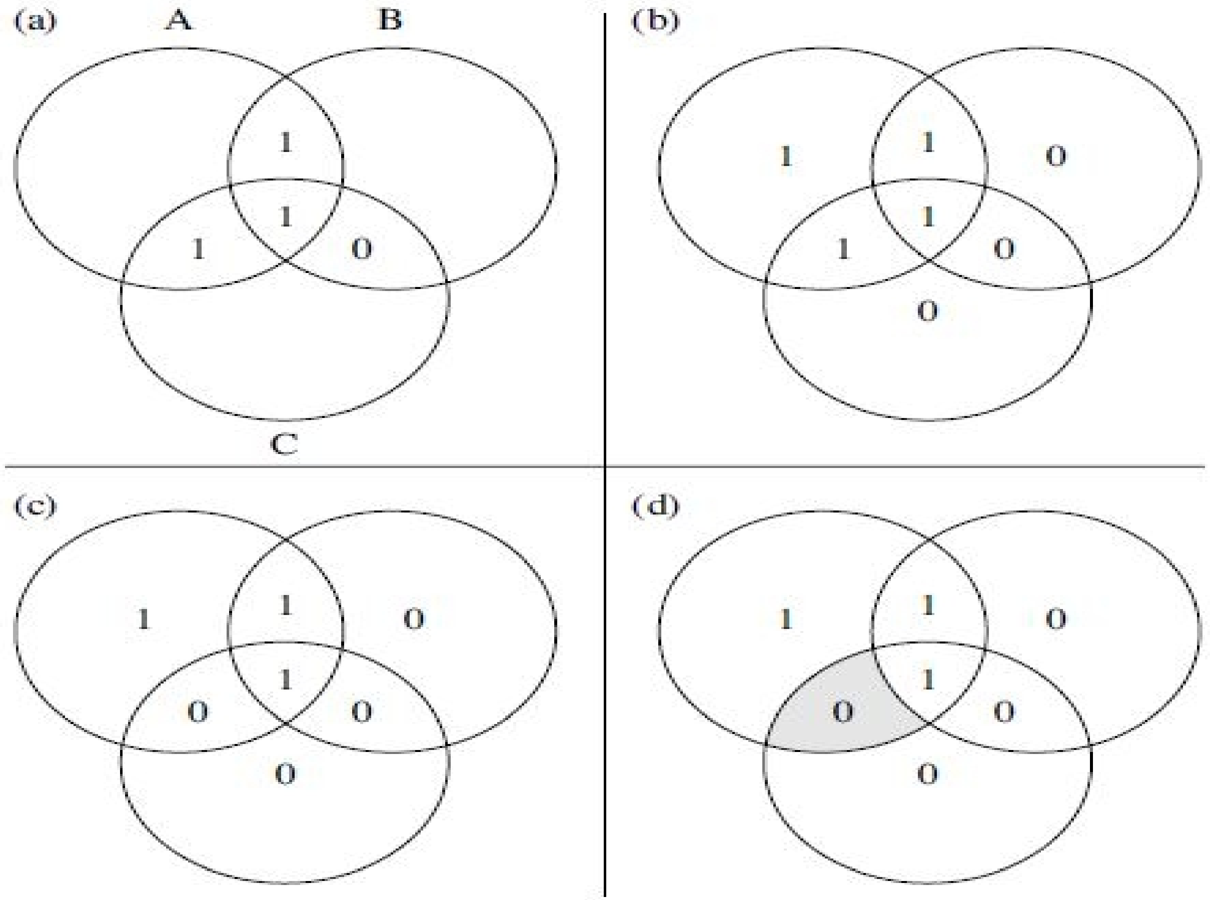
LEARNING OBJECTIVES

After studying this chapter you should be able to:

- Present an overview on the principle types of semiconductor main memory.
- Understand the operation of a basic code that can detect and correct single-bit errors in 8-bit words.

Hamming Error correcting code

- It is the simplest of all error correction codes.
- The figure uses Venn diagrams to illustrate the use of this code on 4-bit words (M=4).
- With 3 intersecting circles there are seven compartments.
- We assign the 4 data bits to the inner compartments. (a)



Syndrome

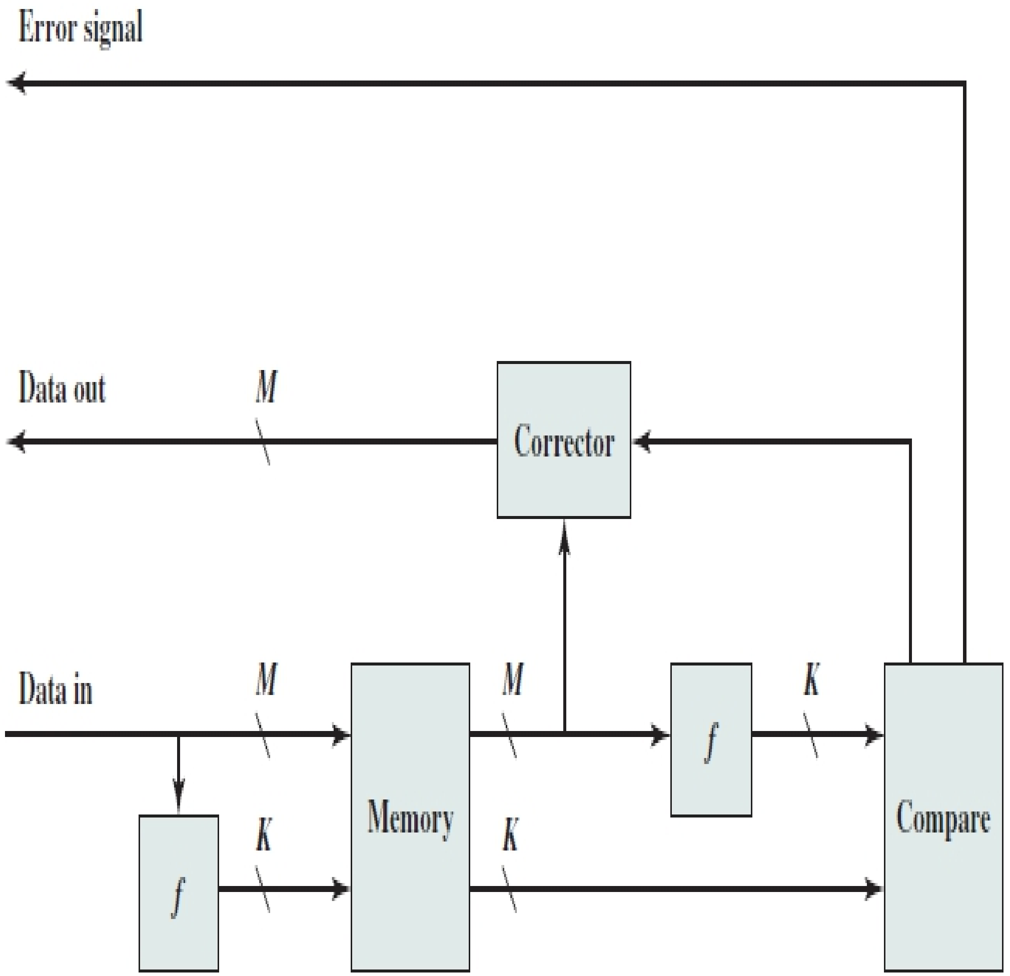
- Eight data bits required four check bits.
- The following table indicates the list of numbers of check bits corresponding to different data word lengths.

	Single-Error Correction		Single-Error Correction/ Double-Error Detection	
Data Bits	Check Bits	% Increase	Check Bits	% Increase
8	4	50	5	62.5
16	5	31.25	6	37.5
32	6	18.75	7	21.875
64	7	10.94	8	12.5
128	8	6.25	9	7.03
256	9	3.52	10	3.91

Contd.

- The comparison logic receives as input two K-bit values.
- A bit-by-bit comparison is done by taking the exclusive-OR of the two inputs.
- The result is called the syndrome word.
- Thus, each bit of the syndrome is 0 or 1 according to if there is or is not a match in that bit position for the two inputs.
- The syndrome word is therefore K bits wide and has a range between 0 and (2^k-1).
- Now because an error could occur on any of the M data bits or K check bits, we must have

$$2^k - 1 \geq M + K$$



Data bits and check bits

- Data bits and check bits

Data Bits	Check Bits
8	4
16	5
32	6
64	7
128	8
256	9

M=8,K=3,K=4
$2^k-1 \geq M+K$
$2^3-1 < 8+3$
$2^4-1 > 8+4$

Contd.

- The syndrome words are generated with the following characteristics.
  - If the syndrome contains all zeros, no error is detected.
  - If the syndrome contains one and only one bit set to 1,then the error has occurred in one of the check bits. No error correction is needed.
  - If the syndrome contains more than one bit set to 1,then the numerical value of the syndrome indicates the position of the data bit in error. This data bit is inverted for correction.
- To achieve this characteristic, consider one example.

- In this example data bit is of 8 bits and check bit is of 4bits, in total 12-bit word.
- The bit positions are numbered from 1 to 12.

Contd.

- Those bit positions whose positions are power of 2 are designated as check bits.
- The layout of the data bits and check bits are given in the following table.

Bit position	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
Position Number	110 0	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Data bits	D_8	D_7	D_6	D_5		D_4	D_3	D_2		D_1		
Check bits					C_8				C_4		C_2	C_1

Contd.

Corresponding to bit position, check bits are calculated as follows

- $C1 = D1 \oplus D2 \oplus D4 \oplus D5 \oplus D7$
- $C2 = D1 \oplus D3 \oplus D4 \oplus D6 \oplus D7$
- $C4 = D2 \oplus D3 \oplus D4 \oplus D8$
- $C8 = D5 \oplus D6 \oplus D7 \oplus D8$

Let the 8-bit data is 00111001.

The check bits are

- $C1 = 1 \oplus 0 \oplus 1 \oplus 1 \oplus 0 = 1$
- $C2 = 1 \oplus 0 \oplus 1 \oplus 1 \oplus 0 = 1$
- $C4 = 0 \oplus 0 \oplus 1 \oplus 0 = 1$
- $C8 = 1 \oplus 1 \oplus 0 \oplus 0 = 0$

Contd.

Let the 3rd bit of data word changes from 0 to 1,the new word becomes 00111101

The corresponding check bit is

- $C1= 1\oplus 0 \oplus 1 \oplus 1 \oplus 0=1$
- $C2=1\oplus 1\oplus 1 \oplus 1\oplus 0=0$
- $C4=0 \oplus 1\oplus 1\oplus 0=0$
- $C8= 1\oplus 1\oplus 0\oplus 0=0$

The syndrome word formed, the ex-or operation of the check bits

C8	C4	C2	C1
0	1	1	1
0	0	0	1
0	1	1	0

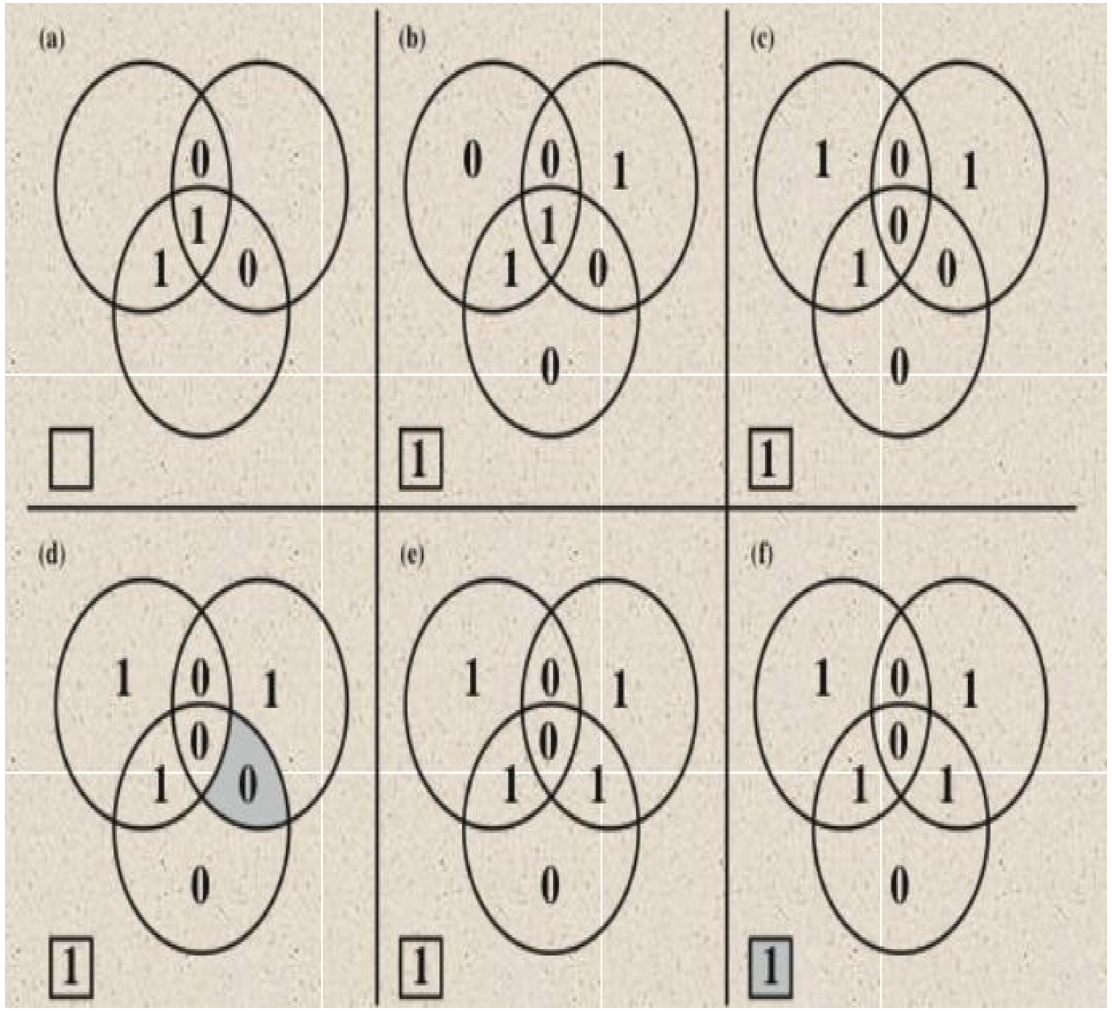
The result is 0110,this indicates the position 6 is in error. The position 6 means the data 3 is in error.

Check bit Calculation

Bit position	12	11	10	9	8	7	6	5	4	3	2	1
Position number	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Data bit	D8	D7	D6	D5		D4	D3	D2		D1		
Check bit					C8				C4		C2	C1
Word stored as	0	0	1	1	0	1	0	0	1	1	1	1
Word fetched as	0	0	1	1	0	1	1	0	1	1	1	1
Position number	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Check bit					0				0		0	1

Hamming SEC-DEC Code

- 4-bit data word.
- The sequence shows that if two errors occur (c), the checking procedure goes astray (d) and worsens the problem by creating a third error (e).
- To overcome the problem an 8th bit is added that is set so that the total number of 1s in the diagram is even.
- The extra parity bit catches the error (f).
- An error correcting code enhances the reliability of the memory at the cost of added complexity.



REVIEW QUESTIONS

1. What happens if a check bit is in error instead of data bit?
2. Suppose an 8-bit data word stored in memory is 11000010. Using the Hamming algorithm, determine what check bits would be stored in memory with the data word?
3. For the 8-bit word 00111001, the check bits stored with it would be 0111. Suppose when the word is read from memory, the check bits are calculated to be 1101. What is the data word that was read from memory?
4. How many check bits are needed if the Hamming error correction code is used to detect single bit errors in a 1024-bit data word?
5. Develop an SEC code for a 16-bit data word. Generate the code for the data word 0101000000111001. Show that the code will correctly identify an error in data bit 5.

THANK YOU