Computer Organization and Architecture (EET 2211)

Chapter 3
A Top-Level View of Computer Function and Interconnection

Point-to-Point Interconnect

- The shared bus architecture was the standard approach to interconnection between the processor and other components (memory, I/O, and so on) for decades.

- But contemporary systems increasingly rely on point-to-point interconnection rather than shared buses.

- At higher data rates, the synchronization and arbitration functions in a timely manner is highly desirable, but the realization of these synchronization functions becomes very difficult.

- Again for multicore chips, where multiple processors and large memories are residing on a single chip, the shared bus failed to provide increased bus data rate and reduced bus latency in order to keep up with the processors.

Quick Path Interconnect (QPI)

- It is a point-to-point processor interconnect developed by Intel and was introduced in 2008.

- The point-to-point interconnect has lower latency, higher data rate, better scalability and increased bandwidth.

Characteristics of QPI

- **Multiple direct connections:** Multiple components within the system have direct pairwise connections to other components. This eliminates the need for arbitration found in shared transmission systems.

- **Layered protocol architecture:** As found in network environments, such as TCP/IP-based data networks, these processor-level interconnects use a layered protocol architecture, rather than the simple use of control signals found in shared bus arrangements.

- **Packetized data transfer:** Data are not sent as a raw bit stream. Rather, data are sent as a sequence of packets, each of which includes control headers and error control codes.

Multicore Configuration Using QPI

- Fig.1. shows the use of QPI on a multicore computer.
- The QPI links (indicated by the green arrow pairs in the figure) form a switching fabric that enables data to move throughout the network.
- Direct QPI connections can be established between each pair of core processors.
- Larger systems with eight or more processors can be built using processors with three links and routing traffic through intermediate processors.

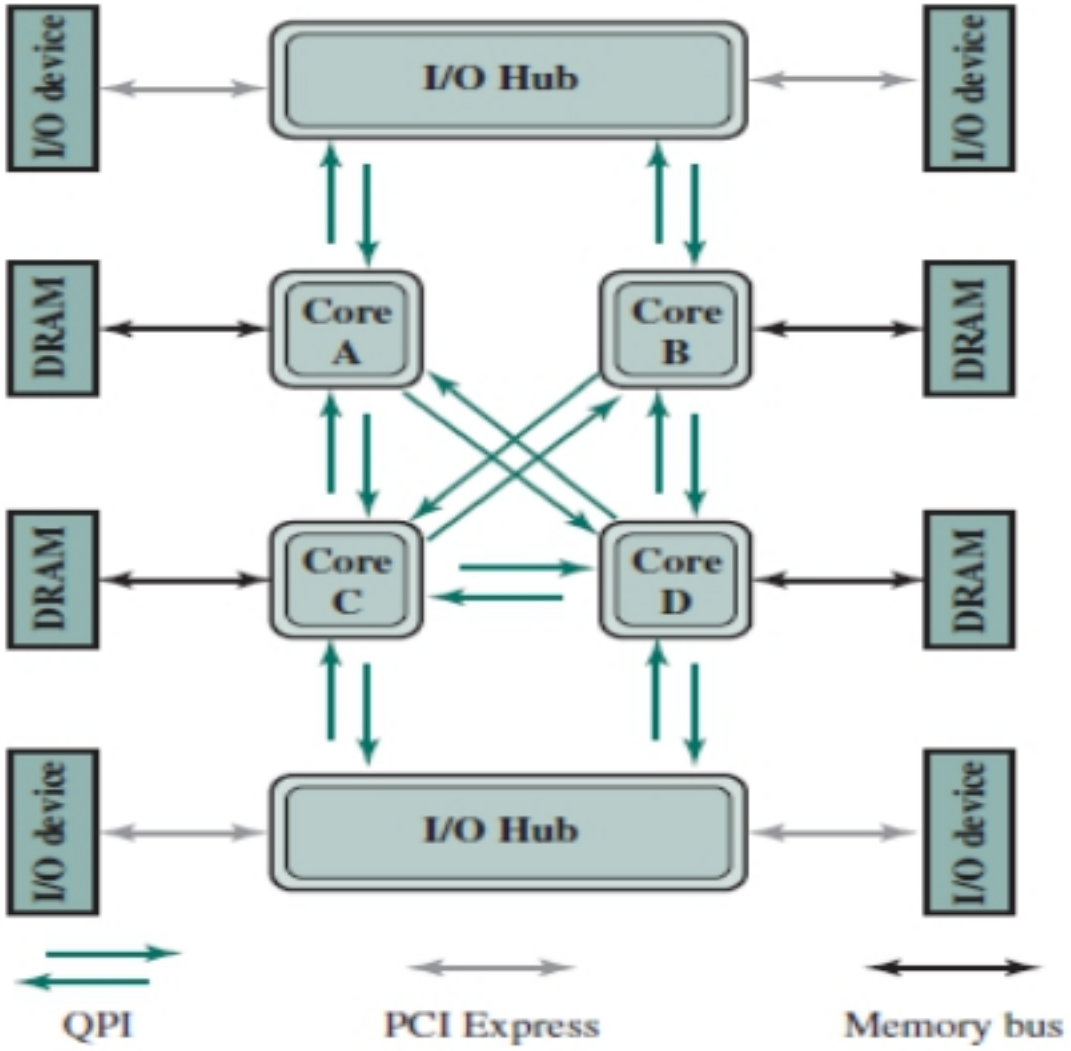

Fig.1. Multicore Configuration Using QPI

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- QPI is used to connect to an I/O module, called an I/O hub (IOH).
- The IOH acts as a switch directing traffic to and from I/O devices.
- The link from the IOH to the I/O device controller uses an interconnect technology called PCI Express (PCIe).
- The IOH translates between the QPI protocols and formats and the PCIe protocols and formats.
- A core also links to a main memory module (typically the memory uses dynamic random access memory (DRAM) technology) using a dedicated memory bus.

QPI Layers

QPI is defined as a four-layer protocol architecture which has the following Layers:

1. **Physical**
2. **Link**
3. **Routing**
4. **Protocol**

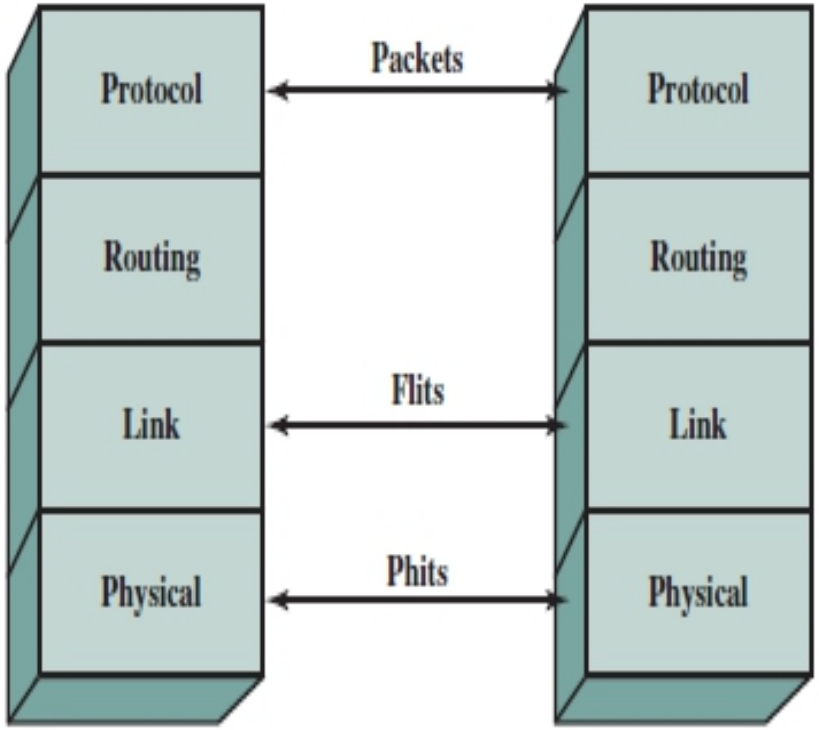

Fig.2. QPI Layers

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- **Physical:** Consists of the actual wires carrying the signals, as well as circuitry and logic to support necessary features required in the transmission and receipt of the 1s and 0s. The unit of transfer at the Physical layer is 20 bits, which is called a **Phit** (physical unit).

- **Link:** Responsible for reliable transmission and flow control. The Link layer's unit of transfer is an 80-bit **Flit** (flow control unit).

- **Routing:** Provides the framework for directing packets through the fabric.

- **Protocol:** The high-level set of rules for exchanging **packets** of data between devices. A packet is comprised of an integral number of Flits.

QPI Physical Layer

- Fig.3. shows the physical architecture of a QPI port.
- The QPI port consists of 84 individual links grouped as follows:
- Each data path consists of a pair of wires that transmits data one bit at a time; the pair is referred to as a **lane**.
- There are 20 data lanes in each direction (transmit and receive), plus a clock lane in each direction.

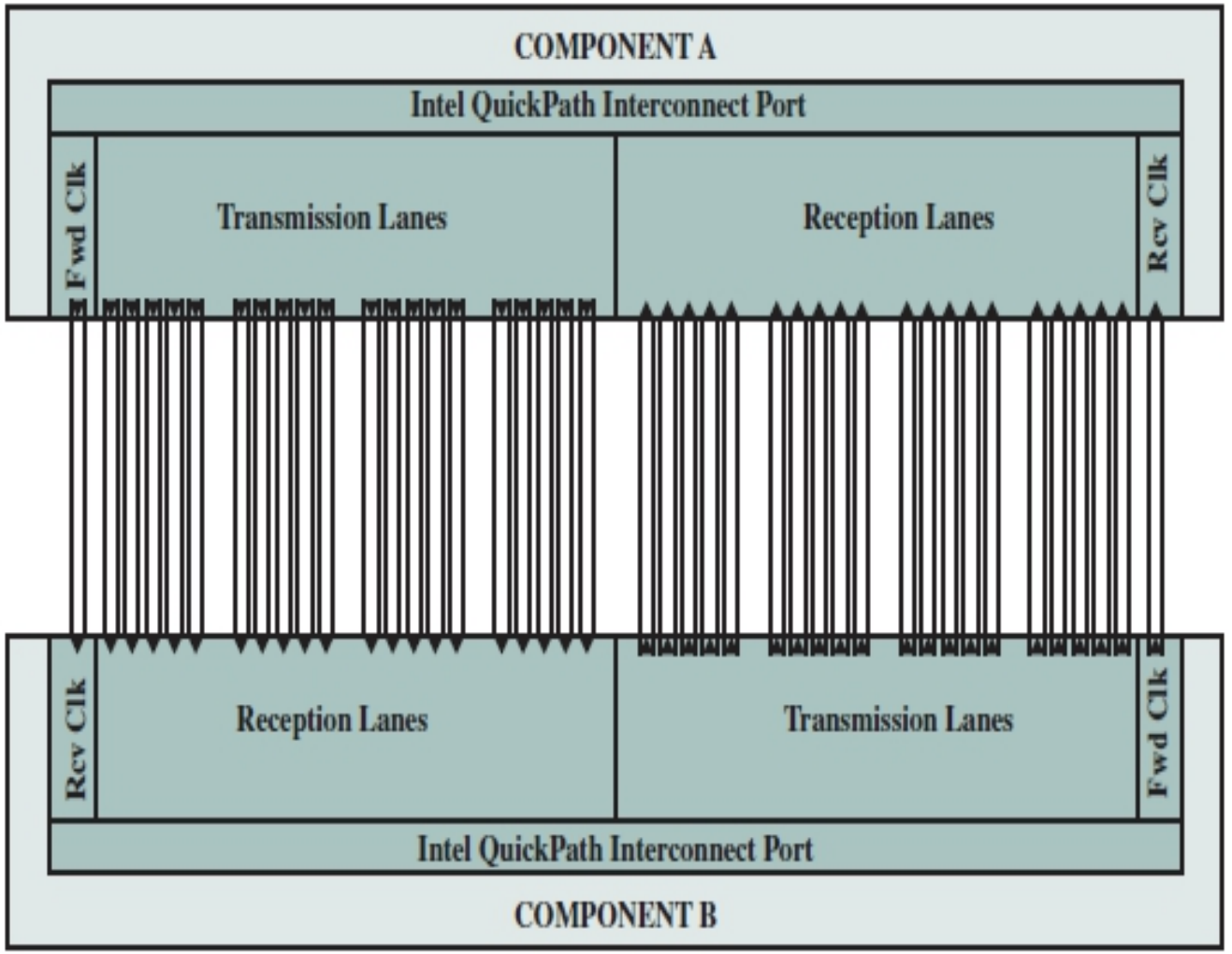

Fig.3. Physical Interface of the Intel QPI Interconnect

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- Thus, QPI is capable of transmitting 20 bits in parallel in each direction. The 20-bit unit is referred to as a *phit*.
- Typical signaling speeds of the link in current products calls for operation at 6.4 GT/s (transfers per second).
- At 20 bits per transfer, that adds up to 16 GB/s, and since QPI links involve dedicated bidirectional pairs, the total capacity is 32 GB/s.
- The lanes in each direction are grouped into four quadrants of 5 lanes each.
- Sometimes, the link can also operate at half or quarter widths in order to reduce power consumption or work around failures.

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- The form of transmission on each lane is known as **differential signaling**, or **balanced transmission**.

- With balanced transmission, signals are transmitted as a current that travels down one conductor and returns on the other.

- The binary value depends on the voltage difference. Typically, one line has a positive voltage value and the other line has zero voltage, and one line is associated with binary 1 and one line is associated with binary 0.

- Specifically, the technique used by QPI is known as ***low-voltage differential signaling*** **(LVDS).**

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- The physical layer is that it manages the translation between 80-bit flits and 20-bit phits using a technique known as **multilane distribution**.

- The flits can be considered as a bit stream that is distributed across the data lanes in a round-robin fashion (first bit to first lane, second bit to second lane.

- This approach enables QPI to achieve very high data rates by implementing the physical link between two ports as multiple parallel channels.

QPI Link Layer

- The QPI link layer performs two key functions: flow control and error control.
- These functions are performed as part of the QPI link layer protocol, and operate on the level of the flit (flow control unit). Each flit consists of a 72-bit message payload and an 8-bit error control code called a cyclic redundancy check (CRC).

- A flit payload may consist of data or message information. The data flits transfer the actual bits of data between cores or between a core and an IOH.

- The message flits are used for functions such as flow control, error control, and cache coherence.

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- **Flow control function:**
- The flow control function is needed to only send as much data as the other side can receive.

- Intel **QPI** has link layer buffers to hold data from receipt on the link until consumption.

- Buffers may store flits or packets, depending on the virtual network on which the data was sent.

- The flow control function can process the data and clear buffers for more incoming data.

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- **Error control function:**

- Occasionally, a bit transmitted at the physical layer is changed during transmission, due to noise or some other phenomenon.

- The **error control function** at the link layer detects and recovers from such bit errors, and so isolates higher layers from experiencing bit errors.

QPI Routing Layer

- The routing layer is used to determine the course that a packet will traverse across the available system interconnects.
- Routing tables are defined by firmware and describe the possible paths that a packet can follow.
- In small configurations, such as a two-socket platform, the routing options are limited and the routing tables quite simple.
- For larger systems, the routing table options are more complex, giving the flexibility of routing and rerouting traffic depending on how

  (1) devices are populated in the platform,

  (2) system resources are partitioned, and

  (3) reliability events result in mapping around a failing resource.

QPI Protocol Layer

- In this layer, the packet is defined as the unit of transfer.
- The key function performed at this level is a cache coherency protocol, which deals with making sure that main memory values held in multiple caches are consistent.
- A typical data packet payload is a block of data being sent to or from a cache.

Thank You !