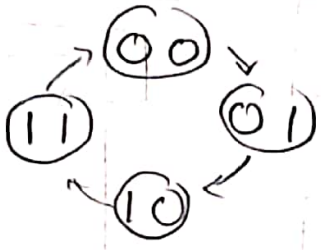
II PRE LAB

Objective 1

a State Diagram:

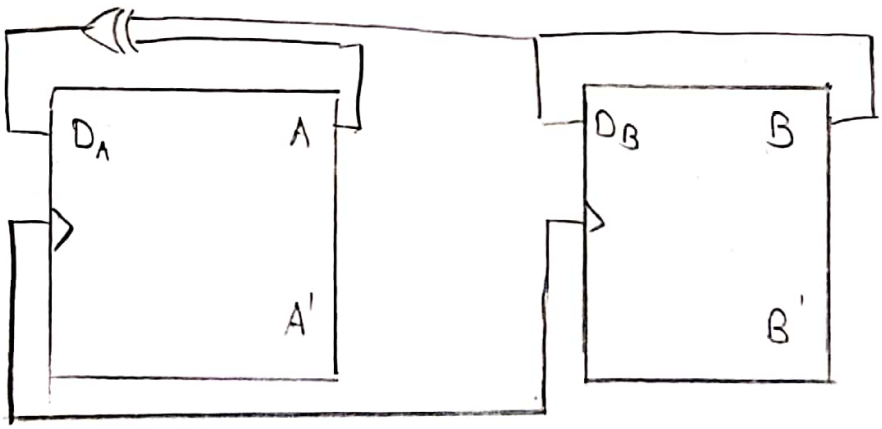


State Table:

Present State		Next State		Flip Flop inputs.		
A	B	A	B	D_A	D_B	D_c
0	0	0	1	0	1	
0	1	1	0	1	0	
1	0	1	1	1	1	
1	1	0	0	0	0	

$D_A = A'B + AB'$ $\quad D_B = B'$

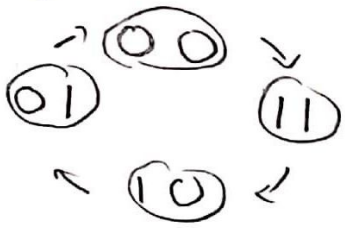
$= A \oplus B$



b)
```
module dff(
input D, clk,
output Q
);
reg Q
always @(posedge clk)
 Q <= D
 end module
module Counter(
input d, clk, reset,
output Q0, Q1
 );
dff d1((Q0 ^ Q1), clk, reset, Q0)
dff d2(Q1, clk, reset, Q1)
end module.
```

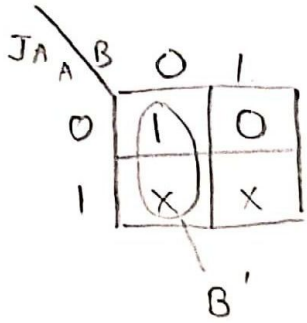
Objective 2

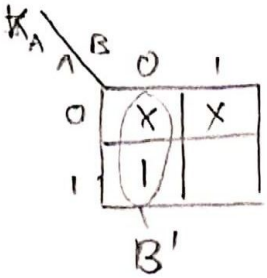
a) State Diagram.



State Table.

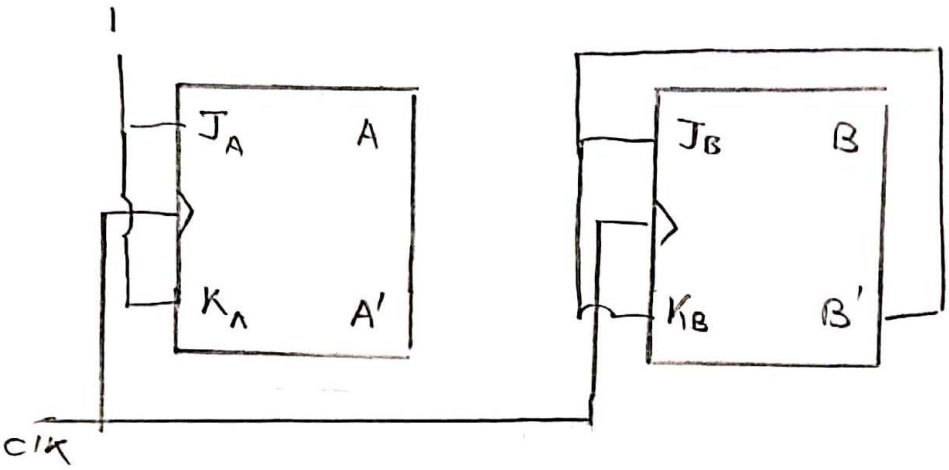
Present State		Next State		Flip-Flop input			
A	B	A	B	J_A	K_A	J_B	K_B
0	0	1	1	1	X	1	X
0	1	0	0	0	X	X	1
1	0	0	1	X	1	1	X
1	1	1	0	X	0	X	1





$J_A = K_A = B'$

$J_B = K_B = 1$



b)

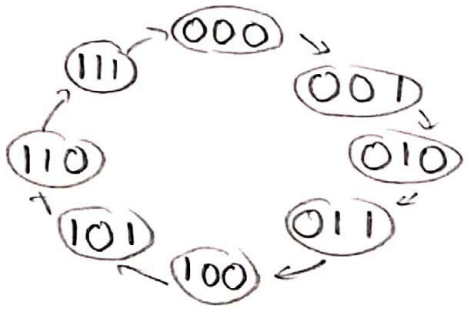
```
module jkff(
input j,k,clk,clear;
output Q;
);
reg Q;
always @(posedge(clk))
begin
if(~clear) begin
Q=1'b0;
end
else
begin
case({j,k})
2'b00: Q<=Q
2'b01: Q<=0;
2'b10: Q<=1;
2'b11: Q=~Q;
```

```
endcase
end
end
endmodule
module counter(
input J, K, clk, clear;
output Q0, Q1
);
jkff A(1, 1, clk, clear, Q0);
jkff B(Q1, ~Q1, clk, clear, Q1);
endmodule
```

Page:

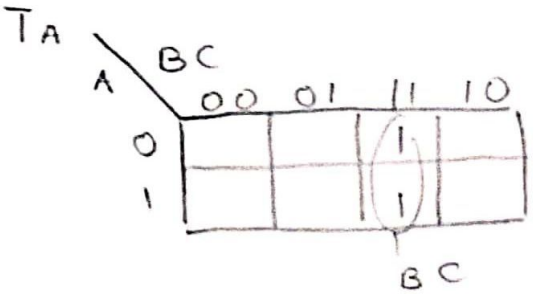
Objective 3

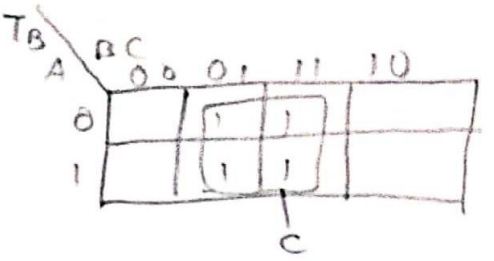
a) State Diagram



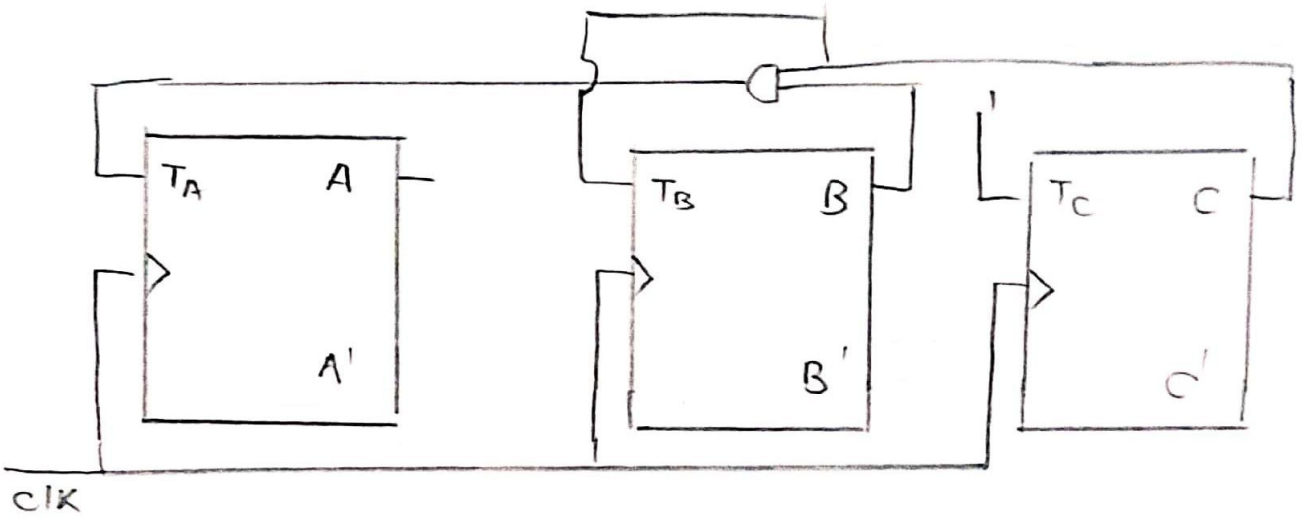
State diagram.

Present State			Next State			Flip Flop Inputs		
A	B	C	A	B	C	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1





$T_A = BC, \quad T_B = C \quad T_C = 1$



b)
```
module tff(
 input T, clk, clear;
output Q
 );
reg Q;
always @ (posedge (clk))
begin
if(~clear)
begin
Q=1'b0;
end
 else
 begin
 Q<= T^Q;
 end
 end module.
```

```
module counter(
 input T, clk, clear;
 output Q0, Q1, Q2
  );
 tff ((Q2 && Q1), clk, clear);
 tff ( Q2 , clk, clear);
 tff ( 1 , clk, clear);
endmodule.
```

III LAB

Components Required.

S.No	Name of the Component	Specification	Quantity
1	D-Flip Flop	IC-7474	1
2	J-K Flip-Flop	IC-7476	2
3	XOR Gates	IC-7486	1
4	AND Gates	IC-7408	1
5	Connecting Wires	23 SWG	As per required

Conclusion

Obj 1- It can be concluded that 2 D-Flip Flop are used to Design 2 bit Synchronous up counter

Obj 2- It can be concluded that 2 JK Flip Flop are used to Design 2 bit Synchronous up down counter.

Obj 3- It can be concluded that 3 T Flip Flop are used to Design 3 bit Synchronous Up Counter.

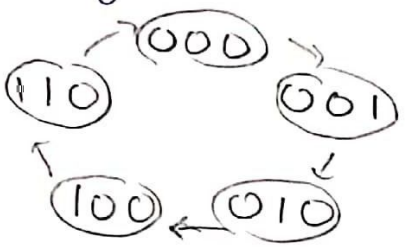
IV POST LAB

1. 1001100111
   +1
   1001101000

Page

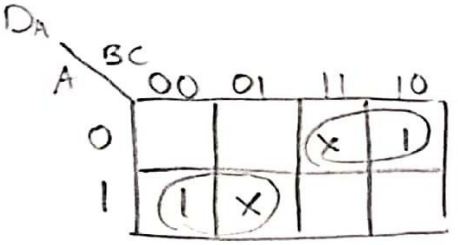
Ans :- 4 Flip-Flops will be complemented.

2. State diagram

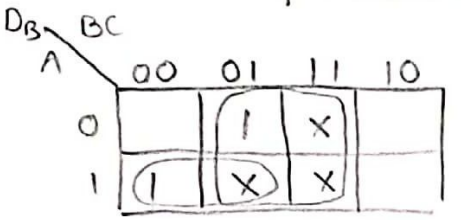


State table :

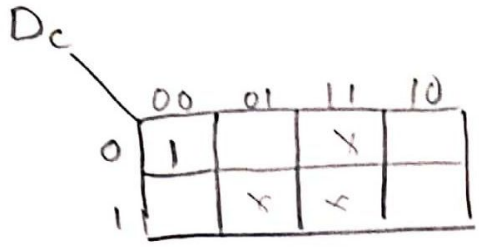
Present State			Next State			Flip Flop inputs		
A	B	C	A	B	C	D_A	D_B	D_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	1	0	0	1	0	0
0	1	1	x	x	x	x	x	x
1	0	0	1	1	0	1	1	0
1	0	1	x	x	x	x	x	x
1	1	0	0	0	0	0	0	0
1	1	1	x	x	x	x	x	x



$D_A = AB' + A'B$
$= A \oplus B$



$D_B = AB' + C$



$D_C = A'B'C'$