COMPUTER ORGANIZATION AND ARCHITECTURE (COA)

EET 2211
4TH SEMESTER – CSE & CSIT
CHAPTER 3, LECTURE 14

CHAPTER 3 – A TOP-LEVEL VIEW OF COMPUTER FUNCTION AND INTERCONNECTION

TOPICS TO BE COVERED

- Computer Components
- Computer Function
- Interconnection Structures
- Bus Interconnection
- Point-to-Point Interconnect
- PCI Express

LEARNING OBJECTIVES

After studying this chapter, you should be able to:

- Understand the basic elements of an instruction cycle and the role of interrupts.
- Describe the concept of interconnection within a computer system.
- Assess the relative advantages of point-to-point interconnection compared to bus interconnection.
- Present an overview of QPI.
- Present an overview of PCIe.

Q1. Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.

a) What is the maximum directly addressable memory capacity (in bytes)?

b) Discuss the impact on the system speed if the microprocessor bus has:
1. 32-bit local address bus and a 16-bit local data bus, or
2. 16-bit local address bus and a 16-bit local data bus.

c) How many bits are needed for the program counter and the instruction register?

Answer 1:

(a) The maximum directly addressable memory capacity in bytes is :

2^(32-8) = 2^24 = 16,777,216 bytes = 16 MB ,(8 bits = 1 byte for he opcode).

(b)1. A 32-bit local address bus and a 16-bit local data bus. Instruction and data transfers would take three bus cycles each, one for the address and two for the data.

Since If the address bus is 32 bits, the whole address can be transferred to memory at once and decoded there; however, since the data bus is only 16 bits, it will require 2 bus cycles (accesses to memory) to fetch the 32-bit instruction or operand.

(b) 2. A 16-bit local address bus and a 16-bit local data bus. Instruction and data transfers would take four bus cycles each, two for the address and two for the data.

Therefore, that will have the processor to perform two transmissions in order to send to memory the whole 32-bit address; this will require more complex memory interface control to latch the two halves of the address before it performs an access to it.

In addition to this two-step address issue, since the data bus is also 16 bits, the microprocessor will need 2 bus cycles to fetch the 32-bit instruction or operand.

(c) For the PC needs 24 bits (24-bit addresses), and for the IR needs 32 bits (32-bit addresses).

Q2. Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that, on average, 20% of the operands and instructions are 32 bits long, 40% are 16 bits long, and 40% are only 8 bits long. Calculate the improvement achieved when fetching instructions and operands with the 32-bit microprocessor.

Answer 2:

By assuming that we have a mix of 100 instructions and operands. From the question:

- 20% of the operands and instructions are 32-bits long, so it is 20 32-bit.
- 40% of the operands and instructions are 16-bits long, so it is 40 16-bit.
- 40% of the operands and instructions are only 8-bits= 1 byte long, so it is 40 bytes.
- The number of bus cycles needed for the16-bit microprocessor will equal to:(20 *2) + 40 + 40 = 120bus cycles.
- The number of bus cycles needed for the 32-bit microprocessor will equal to: 20 + 40 + 40 = 100bus cycles.
- By calculating the improvement achieved with the 32-bit microprocessor to the 16-bit microprocessor will equal to 20/120 = **16.6%**.

THANK YOU