CHAPTER - 19

# SOLIDS AND SEMICONDUCTOR DEVICES

## SYNOPSIS

Conductors have large number of free electrons. Good conductors : silver, copper, gold.

Insulators have very few free electrons. Good insulators : Mica, glass, paper.

Semiconductors have conductivity much less than that of conductors but slightly more than that of insulators.

Outermost energy band in solids is conduction band; Band gap energy is the difference between the energies of conduction band and valence band.

### 1 Types of Semiconductor

1) Intrinsic Semiconductor

eg: pure silicon or pure germanium

2) Extrinsic Semiconductor

eg: Impure Semiconductor

### 1.1 Difference between Intrinsic and extrinsic semiconductors

| | Intrinsic | Extrinsic |
|---|---|---|
| 1 | Semiconductor in pure form. It contains only one element like Si or Ge | Pure semiconductor is doped with impurity to increase the conductivity. |
| 2 | There is only one type semiconductor | There are two type; N-type and P-type depending on the nature of the material. |
| 3 | Number of electrons and holes are equal, $n_e = n_h = n_i$ were $n_i$ is intrinsic carrier concentration | In N-type, number of electrons are greater than number of holes and vice versa in P-type |
| 4 | Electrical conductivity is small. | Electrical conductivity is high. |
| 5 | Conductivity is increased with increase in temperature. | Conductivity is mainly increased with increase in doping concentration. |
| 6 | Conductivity at particular temperature is constant and cannot be changed | By adding impurity, conductivity at particular temperature can be changed. |
| 7 | Almost no practical use | Used in electronic devices |

Table 1.1

### 1.2 Types of extrinsic semiconductors :

1) N - type semiconductors

2) P-type semiconductors

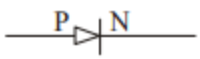
• Doping is the process of adding impurity to the intrinsic semiconductor.

### 1.3 Distinguish between N-type and P-type semiconductors

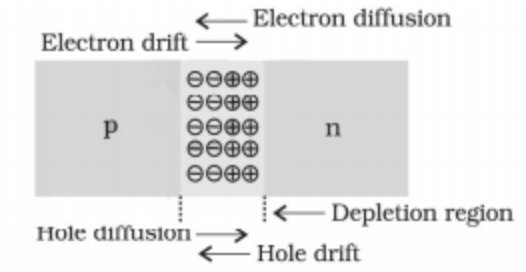
| | N-type | P-type |
|---|---|---|
| 1 | Intrinsic semiconductor with pentavalent impurity | Intrinsic semiconductor with trivalent impurity |
| 2 | Impurities are N, P, As, Sb, Bi | Impurities are B, Al, Ga, In, Tl |
| 3 | Impuritiy atoms are called donor impurity which donate extra electrons | Impurity atoms are called acceptor atom which provide extra holes. |
| 4 | It has excess of electrons but electrically neutral | It has excess of holes but electrically neutral |
| 5 | $n_e > n_h$; electrons are called majority charge carriers and holes are called minority charge carriers | $n_h > n_e$; holes are called majority charge carriers and electrons are called minority charge carriers |
| 6 | Donor energy level is just below the conduction band | Acceptor energy level is just above the valence band |
| 7 | Fermi level shifted towards conduction band | Fermi level shifted towards valence band |
| 8 | Electrons are due to both doping and thermal generation but $n_e \approx N_D$ | Holes are due to both doping and thermal generation but $n_h \approx N_A$ |
| 9 | Holes are only due to thermal generation | Electrons are only due to thermal generation |
| 10 | $I_e >> I_h$ and $I \approx I_e$ | $I_h >> I_e$ and $I \approx I_h$ |
| 11 | $n_h = \frac{n_i^2}{n_e} \approx \frac{n_i^2}{N_D}$ | $n_e = \frac{n_i^2}{n_h} \approx \frac{n_i^2}{N_A}$ |

Table 1.2

## 2 PN junction diode

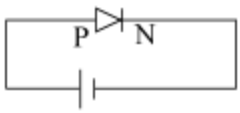



### 2.1 PN junction formation

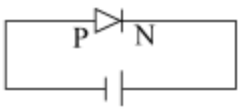



- Two important process during PN junction formation are diffusion and drift.
- During formation of PN junction, due to concentration gradient, hole diffused from P to N and electrons diffused from N to P. This motion results in diffusion current.
- As the diffusion of charge carriers continue, a layer of positive charge developed on N - side and a layer of negative charge developed on P - side. This space charge region is called deplition region.
- Larger the doping, smaller is the width of the PN junction.
- Due to the oppositively charged immobile ions, and electric field is directed from positive charge to the negative charge ie, from N - side to P - side.
- Motion of charge carriers due to the electric field is drift current which is opposite to the direction of diffusion current
- In a P-N junction under equilibrium there is no net current.
- Barrier potential prevents the further motion of majority charge carriers.

## 2.2 Biasing of PN juction




Forward bias



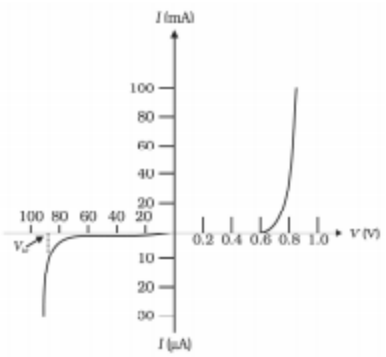

Reverse bias

2.2.1 Comparission of biasing

| | Forward bias | Reverse bias |
|---|---|---|
| 1 | Positive terminal of cell is connected to P-region and negative terminal is connected to N-region | Positive terminal of cell is connected to N region and negative terminal is connected to P-region |
| 2 | External voltage (V) opposes the internal voltage ($V_o$) | External voltage (V) support the internal voltage ($V_o$) |
| 3 | Effective voltage is $\|V - V_o\|$ | Effective voltage is $\|V + V_o\|$ |
| 4 | Depletion width decreases | Depletion width increases |
| 5 | Diffusion current flows from P to N | Drift current flows from N to P |
| 6 | Current is due to majority charge carriers | Current is due to minority charge carries |
| 7 | Current is in milli ampere order | Current is in micro ampere order |
| 8 | Forward current rapidly increase at knee voltage or threshold voltage | Reverse current rapidly increase at breadown voltage |
| 9 | It offers low resistance | It offers high resistance |
| 10 | For ideal diode it is equivalent to short circuited path | For ideal diode it is equivalent to open circuited path |

Table 2.1

### 2.2.2 V–I characteristics of a PN junction diode




Forward resistance $r_f = \frac{\Delta V}{\Delta I}$ is very small. For an ideal PN junction the forward resistance is zero.

Reverse resistance $r_r = \frac{\Delta V}{\Delta I}$ is large. For Germanium diode it is $40k\Omega$. For silicon diode it is $1000k\Omega$.

When the reverse biasing is larger than a certain value, the PN junction breaks down.

### 2.2.3 There are two types of junction breakdown

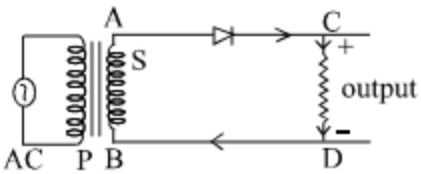
1) Avalanche break down

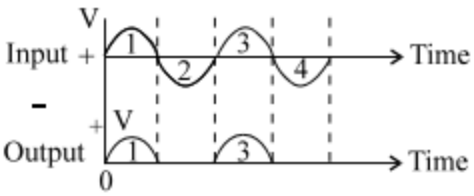
2) Zener breakdown

Avalanche breakdown is due to collision. Avalanche breakdown takes place in lightly doped diodes. Zener breakdown takes place in heavily doped diodes.

## 2.3 Application of PN junction diode

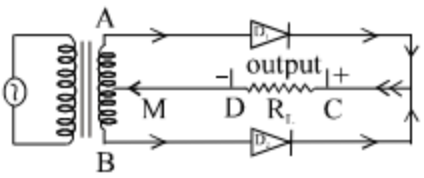
### 2.3.1 Half wave rectifier

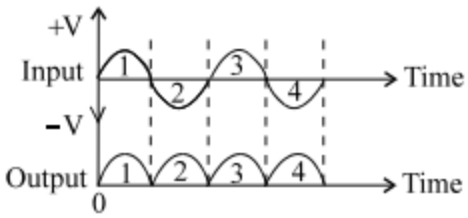



The output of a half wave rectifier is in the form of ripples. In a half wave rectifier the ripple frequency is equal to the input frequency. The number of ripples per second is called ripple frequency.

### 2.3.2 Full wave rectifier



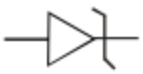
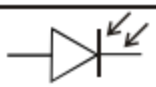
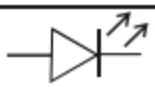
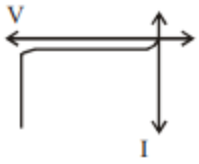
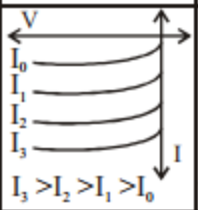
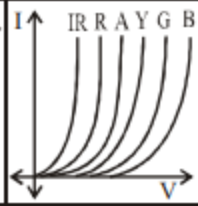
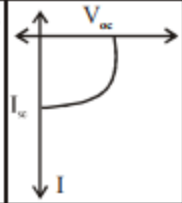

### 2.3.3 Comparission of rectifiers

| Name | | Half wave rectifier | Full wave rectifier (Centre-Tapped) | Full wave rectifier (Bridge) |
|---|---|---|---|---|
| 1 | Number of diodes | 1 | 2 | 4 |
| 2 | Transformer | Ordinary transformer | Center taped transformer | Ordinary transformer |
| 3 | i/p wave form |  |  |  |
| 4 | o/p wave form |  |  |  |
| 5 | o/p frequency | i/p frequency | 2 x i/p frequency | 2 x i/p frequency |
| 6 | efficiency | 40.6% | 81.2% | 81.2% |
| 7 | ripple factor | 1.21 | 0.482 | 0.482 |
| 8 | $I_{rms}$ | $I_0/2$ | $I_0/\sqrt{2}$ | $I_0/\sqrt{2}$ |
| 9 | $E_{rms}$ | $E_0/2$ | $E_0/\sqrt{2}$ | $E_0/\sqrt{2}$ |
| 10 | $I_d$ or $I_{avg}$ | $I_0/\pi$ | $2I_0/\pi$ | $2I_0/\pi$ |
| 11 | $E_d$ or $E_{avg}$ | $2E_0/\pi$ | $2E_0/\pi$ | $2E_0/\pi$ |

Table 2.2

Filter circuits are circuits used to remove the ac components in the output of a rectifier. In forwrd biased diodes the current is due to diffusion. Forward current is due to majority carriers. In reverse biased diodes the current is due to drifting of electrons and holes.

## 2.4 Special purpose PN juction diodes

| 1. | Name | Zener diode | Photo diode | LED | Solar cell |
|---|---|---|---|---|---|
| 2. | Symbol |  |  |  |  |
| 3. | Operating region | III$^{rd}$ Quadrent | III$^{rd}$ Quadrent | I$^{st}$ Quadrent | IV$^{th}$ Quadrent |
| 4. | Biasing | Reverse biasing | Reverse biasing | Forward biasing | No biasing |
| 5. | Application | Voltage regulator | 1. To measure intensity of light<br>2. Photodetector | Convert electrical energy to light | Convert light to electrical energy |
| 6. | Doping | Heavily doped | Lightly doped | Heavily doped | Lightly doped |
| 7. | Deplition width | Narrow | Wide | Narrow | Wide |
| 8. | Characteristics |  |  |  |  |
| 9. | Process during operation | Field ionization or field emission | 1. Carrier generation<br>2. Carrier seperation | Radiative recombination | 1. Carrier generation<br>2. Carrier seperation<br>3. Carrier Collection |
| 10. | Working principle | - | Photo voltaic effect | - | Photo voltaic effect |

IR - Infra red, R - Red, A - Amber, Y - Yellow, G - Green, B - Blue

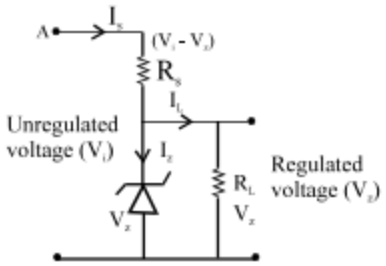
**Table 2.3**

### 2.4.1 Zener Diode

- Deplition width is less than $10^{-6}$ m
- Electric field of the junction is high about $5\times10^{6}\,V/m$
- After reverse voltage $V_z$ , zener voltage remains constant even though current through the zener diode varies over a wide range.
- Field ionization or field emission : when reverse voltage, $V = V_z$, the electric field strength is high enough to pull valance electrons from the host atom on the P side which are accelerated to N side. These electrons account for the high current at break down. This emission of electrons from host atom due to high electric field is known as internal field emission.

- The electric field required for field ionization is of the order of $10^6 V/m$

**Zener diode as voltage regulator:**




(i) $I_s = \frac{V_i - V_z}{R_s}$ (ii) $I_L = \frac{V_z}{R_L}$ (iii) $I_z = I_s - I_L$ (iv) $P_z = V_z I_z$

(v) $R_s = \frac{V - V_z}{I_s} = \frac{V - V_z}{I_z + I_L}$

- If input voltage increases, current through $R_s$ and zener diode also increases. This increases voltage drop across $R_s$ without any change in voltage drop across zener. This is because in the break down region, zener voltage remains constant eventhough current through zener changes.
- If we decrease input voltage, current through $R_s$ and zener decrease without any change in voltage across zener.
- Any increase/decrease in the input voltage results in increase/decrease of voltage drop across $R_s$ without any change in voltage across zener diode, thus it act as a voltage regulator.

### 2.4.2 Opto electric PN junction diode

(i) Photo diode:

- It is fabricated with a transperent window to allow the light to fall on it
- When photodiode is illuminated with light (photon) with $h\nu > E_g$, then electron-hole pair generates, near the depletion region.
- Due to electric field at junction, electrons and holes are seperated before they recombine. [electrones are collected on N - side holes are connected on P-side]
- Magnitude of photo current depends on intensity of incident light
- On illumination of light, fractional change in majority carriers would be much less than that in minority charge carriers. ie, fractional change due to the photo effects on minority carrier dominated reverse bias current and is more easily measurable than forward bias current.

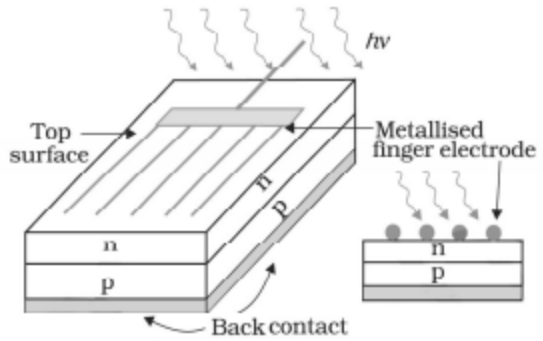
(ii) LED

- Due to forward bias, minority carrier concentration at the junction increases. Thus they recombine with majority carrier and energy is released in the form of photon with energy equal to or slightly less than the band gap.
- Intensity of light from LED increases as forward current increases and reaches a maximum at a critical value, further increase in forward current results in decrease of light intensity.
- V-I characteristics of LED is similar to that of silicon but threshold voltage is much higher and different for each colour
- For fabrication of visible LED the energy gap must lie between 1.8 eV and 3 eV.
- $GaAs_{1-x}P_x$ and for LED of different colours

- $GaAs_{0.6}P_{0.4}$ (Eg $\approx$ 1.9 eV) and for Red LED
- GaAs (Eg $\approx$ 1.43 eV) for infra red LED
- LED is used in remote controls, burglar alarm system
- advantages (i) low operational voltage and less power
  (ii) fast action, no warm up time required
  (iii) nearly monochromatic
  (iv) long life and ruggedness
  (v) fast on-off switching

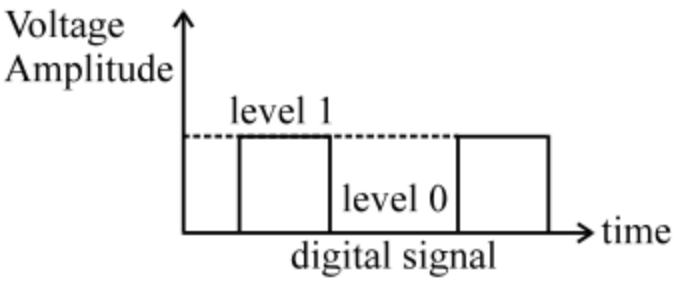
(iii) Solar cell

- Top layer is made to be thin for generation near the depleation area
- Junction area has kept larger for handling more power
- Materials with band gap close to 1.5 eV (between 1eV – 1.8 eV) are ideal for solar cell fabrication eg: Si (1.12 eV), GaAs (1.43 eV), Cd Te (e.45 eV) $CuInSe_2$(1.04 eV)
- Sunlight is not required for a solar cell. Any light with photon energy greater than the band gap can be used.




## 4 Digital Electronics

- In digital electronics we use only digital signals
- Digital signal is a pulse wave form, in which discrete values of voltage are possible
- We use binary numbers to represent digital signal ie 0 (say 0V) and 1 (Say 5V)




· In digital system, we follows boolean algebra

| boolean multiplication | boolean addition |
|---|---|
| 0 x 0 = 0 | 0 + 0 = 0 |
| 0 x 1 = 0 | 0 + 1 = 1 |
| 1 x 0 = 0 | 1 + 0 = 1 |

1 x 1 = 1 1 + 1 = 1

## 4.1 Logic Gates

- Logic gate is a digital circuit that follows certain logical relationship between the input and output voltages
- Logic gates are basic building blocks of digital electronics
- Logic gate also represented by boolean expressions [We use capital letters of english alphabet for representing variables of boolean expression]
- Operation of logic gate is indicated in a table known as truth table. It is the tabular representation of all the possible combination of inputs and their corresponding outputs.

### 4.1.1 Basic logic gates

- There are three basic logic gates. AND gate, OR gate and NOT gate.
- We can realize all the boolean expression with the combination of these three logic gates.

**Basic logic gates**

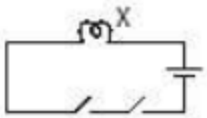
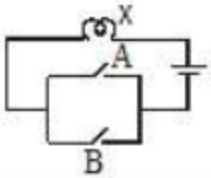
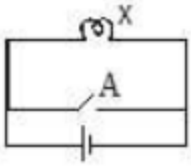
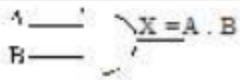
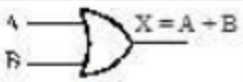
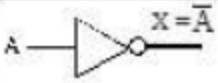
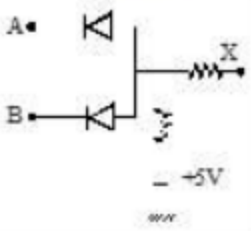
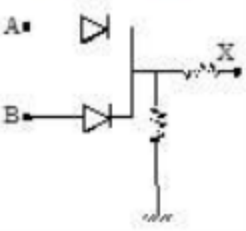
| 1. | Name | AND | OR | NOT |
|---|---|---|---|---|
| 2. | Electrical Analogue |   |   |   |
| 3. | Truth Table | i/p A B / o/p X: 0 0 0; 0 1 0; 1 0 0; 1 1 1 | i/p A B / o/p X: 0 0 0; 0 1 1; 1 0 1; 1 1 1 | i/p A / o/p X: 0 1; 1 0 |
| 4. | Boolean expression | X = A . B | X = A + B | X = $\bar{A}$ |
| 5. | Symbol |   |   |   |
| 6. | law | AND law<br>A . 0 = 0<br>A . 1 = A<br>A . A = A | OR law<br>A + 0 = A<br>A + 1 = 1<br>A + A = A | NOT law<br>A + $\bar{A}$ = 1<br>A . $\bar{A}$ = 0<br>$\bar{\bar{A}}$ = A |
| 7. | realization using diodes |   |   | |

Table 4.1

- Demorgan's law : (i) $\overline{A+B}=\overline{A}.\overline{B}$

  (ii) $\overline{A.B}=\overline{A}+\overline{B}$
- Indentities : (i) A + AB = A (iii) (A+B) (A+C) = A + BC

  (ii) A . (A+B) = A (iv) $A\left(\overline{A}+B\right)=AB$

### 4.1.2 Universal logic gates

- There are two universal logic gates, NAND gate and NOR gate.
- We can realize all the boolean expression using repeated use of universal logic gates. ie we can realize other basic gates like OR, AND, NOT etc with these gates. Hence it is considered as basic building blocks of other gates.
- NAND gate is an AND gate followed by a NOT gate similarly NOR gate is an OR gate followed by a NOT gate

**Universal logic gates**

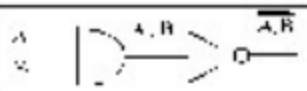
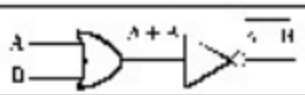
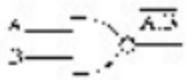
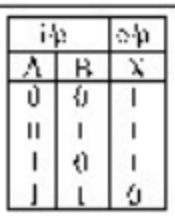
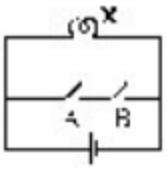
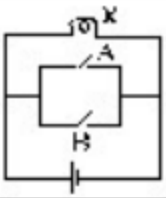
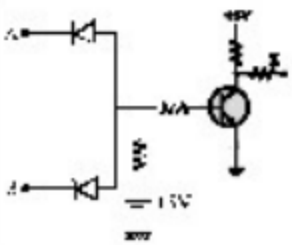
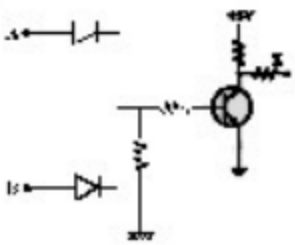
| | Name | NAND | NOR |
|---|---|---|---|
| 3. | Structure |  |  |
| 4. | Symbol |  |  |
| 4. | Boolean expression | $X=\overline{A.B}$ | $X=A+B$ |
| 5. | Truth Table |  |  |
| 6. | Electrical analogue |  |  |
| 7. | realization using diode and transistor |  |  |

Table 4.2

### 4.1.3 Exclusive logic gates

- There are two exclusive logic gate XOR gate and XNOR gate

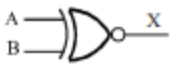
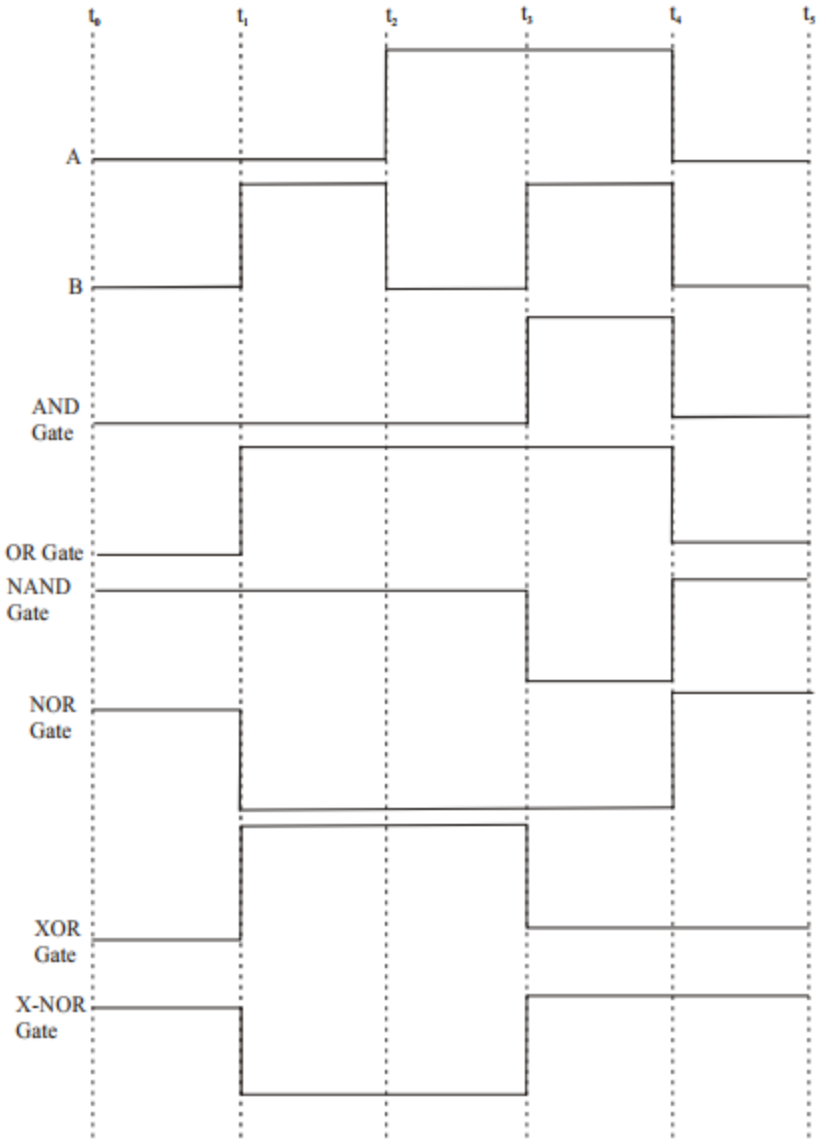
| 1. | Name | XOR | XNOR |
|---|---|---|---|
| 2. | Symbol |  |  |
| 3. | Boolean expression | $X = A \oplus B$<br>$X = \bar{A}B + A\bar{B}$ | $X = \overline{A \oplus B}$ $X = A \odot B$<br>$X = \bar{A}\bar{B} + AB$ |
| 4. | Truth Table | i/p: A B; o/p: X<br>0 0 0<br>0 1 1<br>1 0 1<br>1 1 0 | i/p: A B; o/p: X<br>0 0 1<br>0 1 0<br>1 0 0<br>1 1 1 |

Table 4.3

### 4.2 Wave form representation (A, B represent i/p)



### 4.3 Realization of other gates using universal logic gates

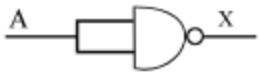
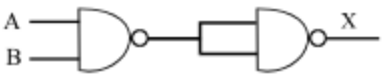
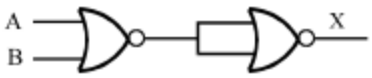
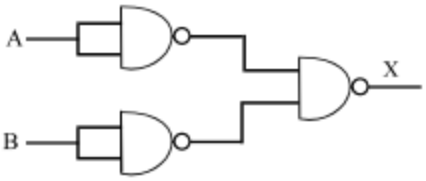
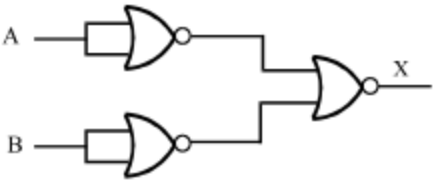
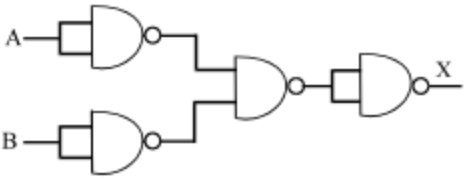
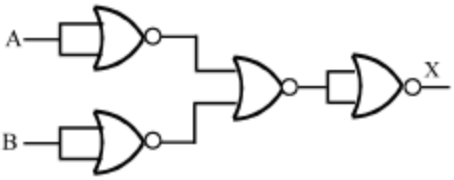
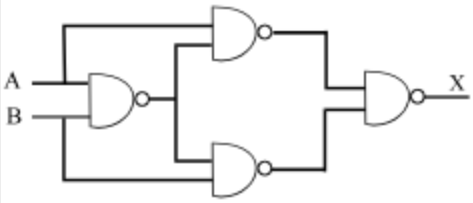
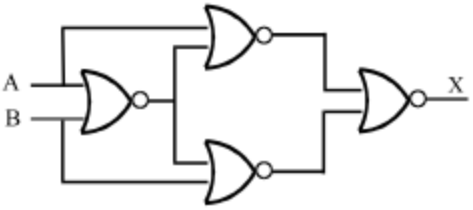
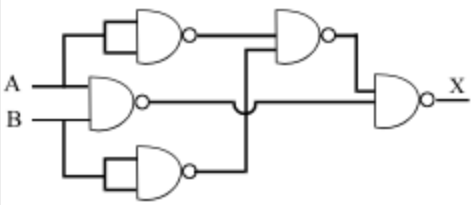
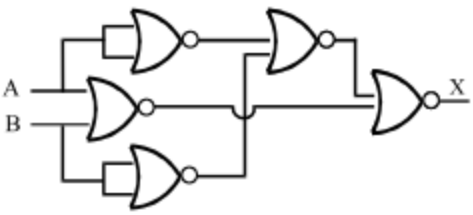
| No. of gate used | NAND | NOR |
|---|---|---|
| 1. |  Shorted NAND gate = NOT |  Shorted NOR gate = NOT |
| 2. |  AND gate |  OR gate |
| 3. |  OR gate |  AND gate |
| 4. |  NOR gate |  NAND gate |
| 4. |  XOR gate |  X-NOR gate |
| 5. |  X-NOR gate |  XOR gate |

Table 4.4

### 4.4 Integrated Circuits:

- We can fabricate an entire circuit including passive and active compounds, on a small single chip. These are known as integrated circuit.
- Most widely used technology for IC manufacturing is monolithic integrated circuit.

- The chip dimensions are very small and is about 1mm $\times$ 1mm.
- IC can be grouped into two categories
  a) Linear or analogue IC eg : Operational Amplifier
  b) Digital IC eg : logic gates

| Term used for IC | No of components |
|---|---|
| SSI (small scale integration) | logic gate $\leq$ 10 |
| MSI (medium scale integration) | logic gate $\leq$ 100 |
| LSI (large scale integration) | logic gate $\leq$ 1000 |
| VLSI (very large scale integration) | logic gate $\leq$ 1000 |

Table 4.5

- The memory capacity of IC is doubled every one and half year. This is popularly known as moore's law.

## SECTION - I - Straight objective type questions

1. Which of the following is wrong about a conductor

   A) Lowest energy level of conduction band is lower than highest energy level of valance band

   B) Conduction band and valance band overlap each other

   C) The valence band is partially empty and conduction band is partially filled

   D) The valence band is completely filled and conduction band is completely empty

   E) None of these

2. The number of silicon atom per $m^3$ is $5\times10^{28}$. This is doped simultaneously with Arsenic and Indium at doping concentration 1:$10^6$ and 1:$10^8$ respectively. Then number of hole is $\left[n_i = 1.5\times10^{16} \text{ per } m^3\right]$

   A) $4.95\times10^{22}$ B) $4.5\times10^{9}$

   C) $4.5\times10^{10}$ D) $4.95\times10^{20}$

   E) $3\times10^{10}$

3. The charge of an n-type semiconductor is

   A) positive

   B) negative

   C) depends on doping concentration

   D) neutral

   E) Both A and C

4. A PN junction diode is not connected to any circuit, then

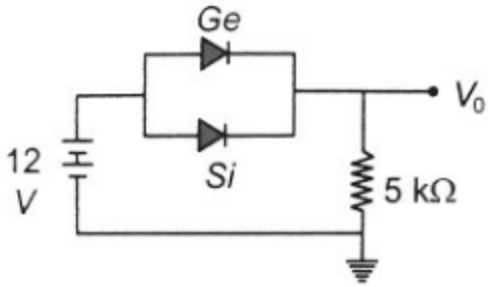
   A) Electron diffuses from P side to N side and hole diffuses from N side to P side

   B) P-type side is at higher potential than the N-type side

   C) There is an electric field at the junction directed from the P-type side to the N-type side

   D) Barrier potential developed across the PN junction depends on nature of the material, doping concentration on either side and temperature

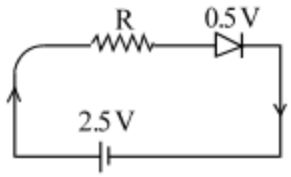
5. Ge and Si diodes conduct at 0.3 V and 0.7 V, respectively. In the following figure, if Ge diode connection are reversed, the value of $V_0$ changes by




A) 0.2 V B) 0.4 V

C) 0.6 V D) 0.8 V

6. The diode used in the circuit shown in fig. has a constant voltage drop at 0.5 V at all currents and a maximum power rating of 100 milliwatt. What should be the value of the resistance R connected in series and with diode for obtaining maximum current?




A) 2Ω B) 4Ω

C) 6Ω D) 10Ω

7. Which of the following statement is not true about intrinsic semiconductor

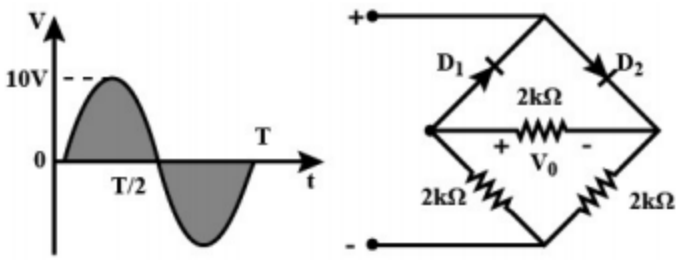
A) The hole behaves as apparent free particle with effective positive charge

B) Number of free electrons $n_e$ is equal to number of holes $n_h$, that is $n_e = n_h = n_i$

C) Motion of hole is a convenient way of describing the actual motion of bound electrons

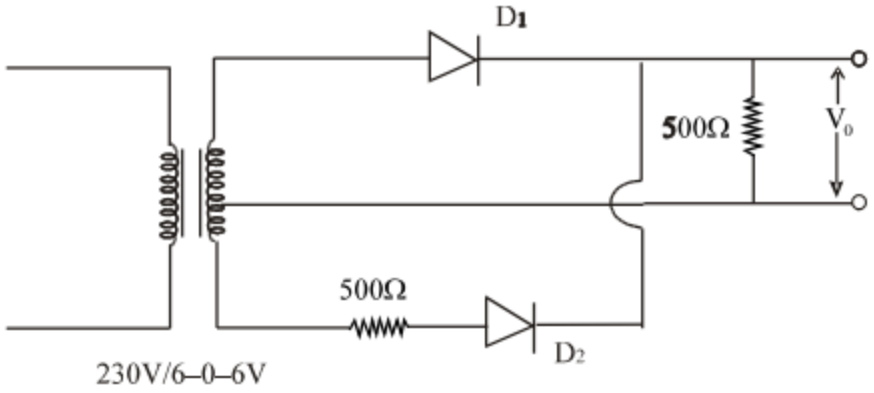
D) At equilibrium rate of thermal generation greater than the rate of recombination of charge carriers

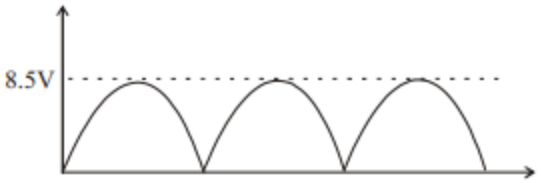
8. In the circuit shown in figure, the maximum output voltage $V_0$ is

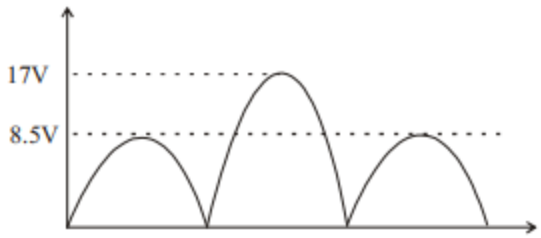


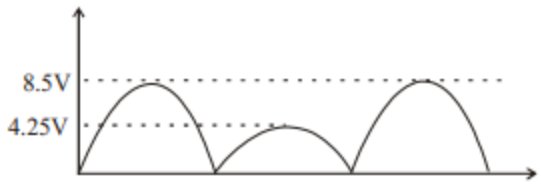

A) 0 V B) 5 V C) 10 V D) $\frac{5}{\sqrt{2}}$ V

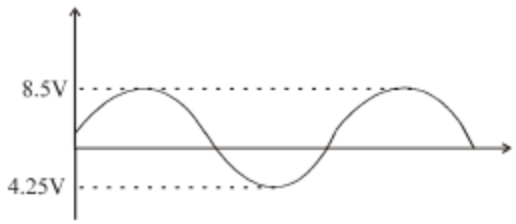
9. Output Waveform of the given circuit diagram is




A)



B)



C)



D)



10. In a p-type semiconductor the acceptor level is situated 60 meV above the valence band. The maximum wavelength of light required to produce a hole will be

A) $0.207 \times 10^{-5}$ m

B) $2.07 \times 10^{-5}$ m

C) $20.7 \times 10^{-5}$ m

D) $207 \times 10^{-5}$ m

11. V-I characteristics of some PN junction devices are given:

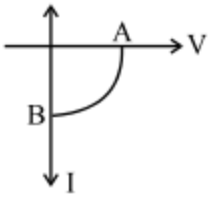


Fig 1

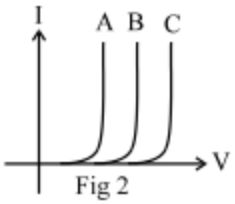


Fig 2

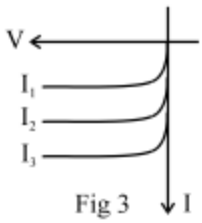


Fig 3

(i) Fig 1 represent V-I characteristics of solar cell with A and B represent open circuit voltage and open circuit current

(ii) Fig 2 represent V-I characteristics of LED with A, B, C are corresponding to Green, Red and Infra red colour respectively

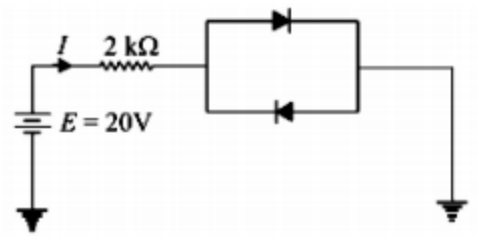
(iii) Fig 3 represent the V-I characteristics of photo diode with $I_3 > I_2 > I_1$

A) (iii) only correct B) (ii) only correct

C) (i) only correct D) (i) and (iii) are correct

E) (i) and (ii) are correct

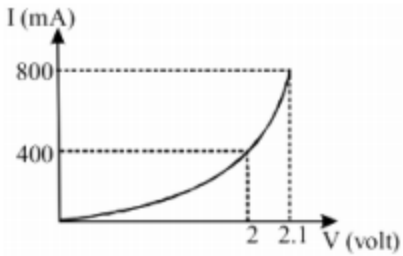
12. Assuming the diodes to be of silicon with forward resistance zero, the current I in the following circuit is




A) 0 B) 9.65 mA C) 10 mA

D) 10.36 mA E) 8.5 mA

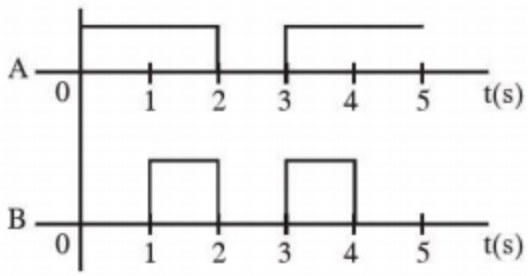
13. The I-V characteristic of a P-N junction diode is shown below. The approximate dynamic resistance of the p-n junction when a forward bias of 2 volt is applied is

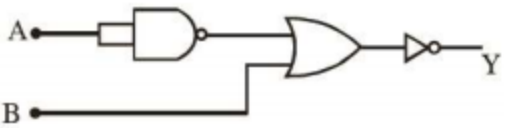



A) 1Ω B) 0.25Ω

C) 0.5Ω D) 5Ω

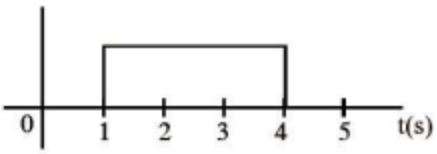
14. Draw the output signal Y in the given combination of gates



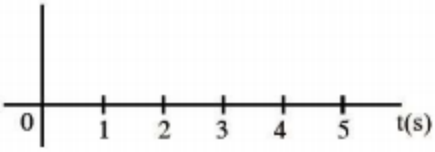




A)

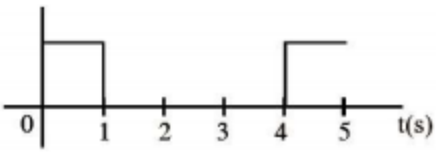

B)




C)



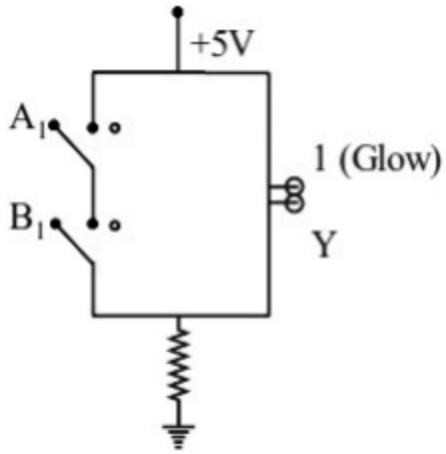

D)




15. An N-type silicon sample of width $4 \times 10^{-3}$ m, thickness and length $25 \times 10^{-5}$, $6 \times 10^{-2}$ respectively carries a current of 4.8 mA. When the voltage is applied across the length of this sample. If the free electron density is $10^{22} m^{-3}$. Find how much time it takes for the electrons to travel the full length of the sample

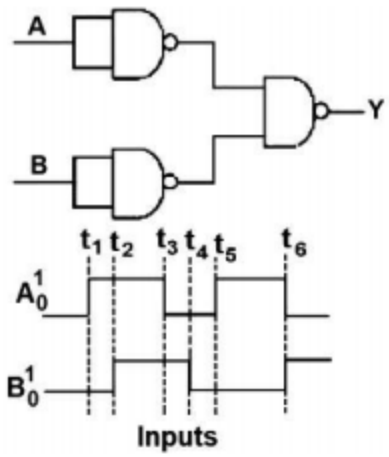
A) 0.5 sec B) 4 sec C) 0.3 sec D) 0.02 sec

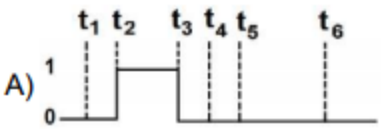
16. The logic gate equivalent to the give circuit diagram is :

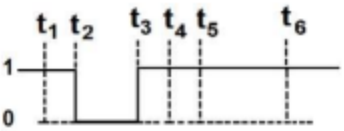


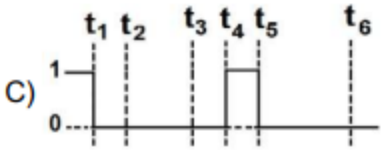

A) OR B) NAND C) NOR D) AND

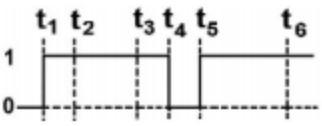
17. The output waveform of the given logical circuit for the following inputs A and B as shown below.



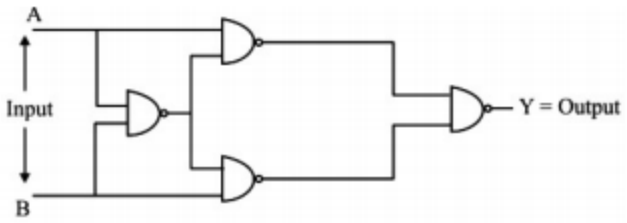

A) 


B) 


C) 


D) 

18. The output Y for the inputs A and B of circuit is given by




A)

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

B)

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

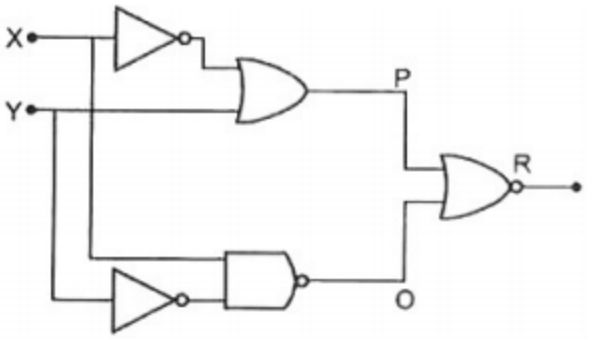
C)

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

D)

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

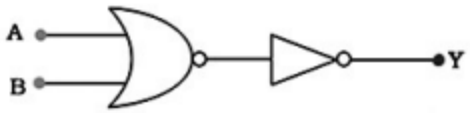
19. Figure given gives a system of logic gates. From the study of truth table it can be found that to produce a high output (1) at R, we must have



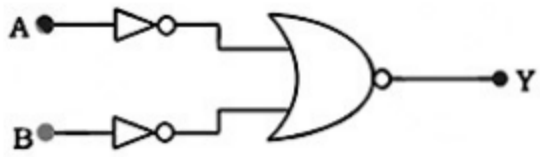

A) X = 0, Y = 1
B) X = 1, Y = 1
C) X = 1, Y = 0
D) X = 0, Y = 0

20. The given circuits are act as

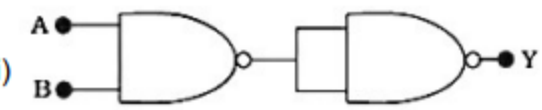
i)



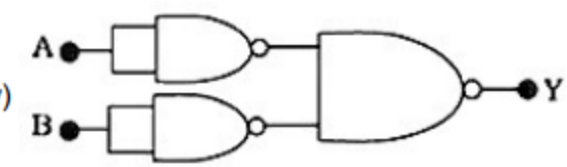

ii)




iii)




iv)



A) (i) and (ii) represent and gate AND (iii) and (iv) represent OR gate

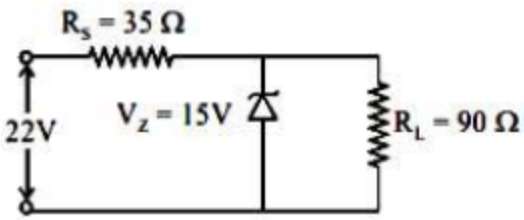
B) (i) and (iii) represent AND gate and (ii) and (iv) represent OR gate

C) (i) and (iv) represent NAND gate and (ii) and (iii) represent NOR gate

D) (i) and (iv) represent OR gate and (ii) and (iii) represent AND gate

**Section 2 - Numerical Type Questions**

21. The value of power dissipated across the zerner diode $(V_z = 15V)$ connected in the circuit as shown in the figure is $x \times 10^{-1}$ watt

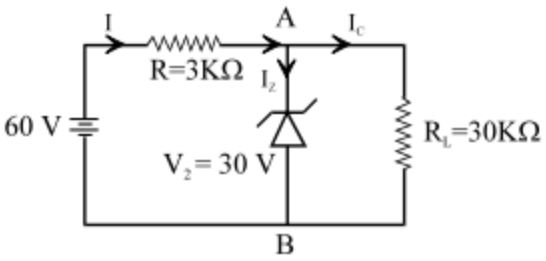



The value of x, to the nearest integer, is

22. An N-type silicon crystal of cross sectional area $10^{-6}m^2$ carries a current of 4.8mA. If free electron density is $10^{22}/m^3$ when the voltage is applied across the length 6cm of the crystal, find how much time taken for the electron to trace full length of the sample

23. The current gain of a transistor in common base mode is 0.995. The current gain of the same transistor in common emitter mode is

24. In the figure the current through the diode is (use ideal diode approximations)




25. In connection with the circuit drawn below, the value of current flowing through $2k\Omega$ resistor is $.....\times 10^{-4}$ A