Daffodil International University

Department of Computer Science & Engineering

Lab Manual

Version: 2017.04

Course Code: **CSE 213**

Course Title: **Digital Electronics Lab**

Table of Contents

Session 1: Introduction to Primary and Universal Logic Gate

a. Get familiar with IC and ALU

b. Understanding Different Combinational circuit.

c. Gathering Idea about sequential circuit and logic design.

Expected Skills:

a. Basic knowledge on logic gate implementation. .

b. Basic knowledge on Hardware

Tools Required:

a. Various type of IC

b. Breadboard Board

c. LED

Session Detail:

To verify the input and output relationships/characteristics of 2-input AND, OR and 1-input NOT gates.

Required Instruments and ICs:

1. AT-700 Portable Analog/Digital Laboratory (or AT-800 Modular Lab, AT-701 Personal Lab)

2. 7404(NOT), 7408(AND), 7432(OR)

Circuit Diagram:

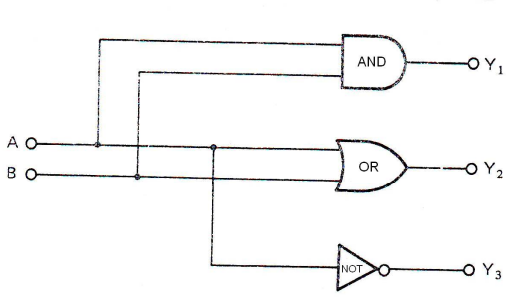
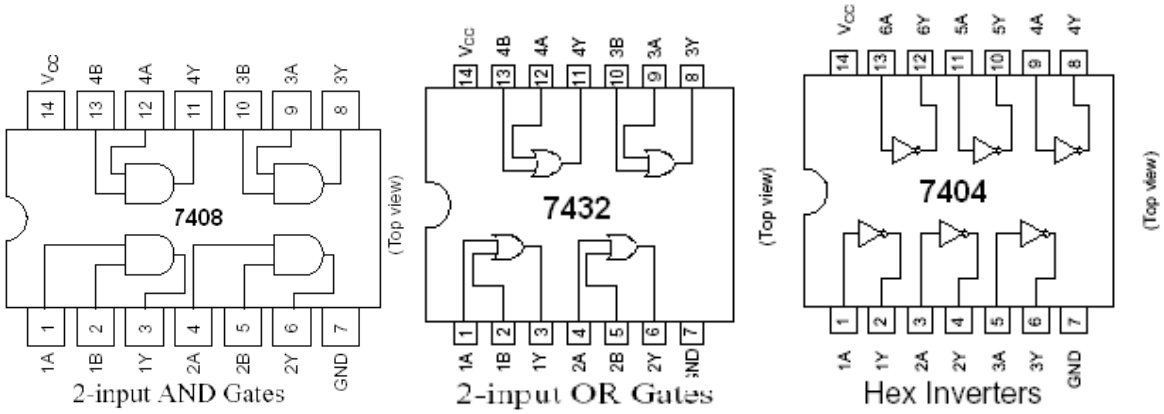


Fig 1–1



Procedure:

Step 1: Find out correctly the input and output pin numbers of each gate.

Step 2: Install the components of Fig 1-1 onto the breadboard of AT-700 and check properly the connections. Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".

Step 3: Connect the Data switches "0" and "1" to point A and B of fig. 1-1 respectively. Then connect 8 bit LED Display's "0", "1" and "2" to the output of point Y1, Y2 and Y3 of Fig. 1-1 respectively. The connection diagram is as follows.

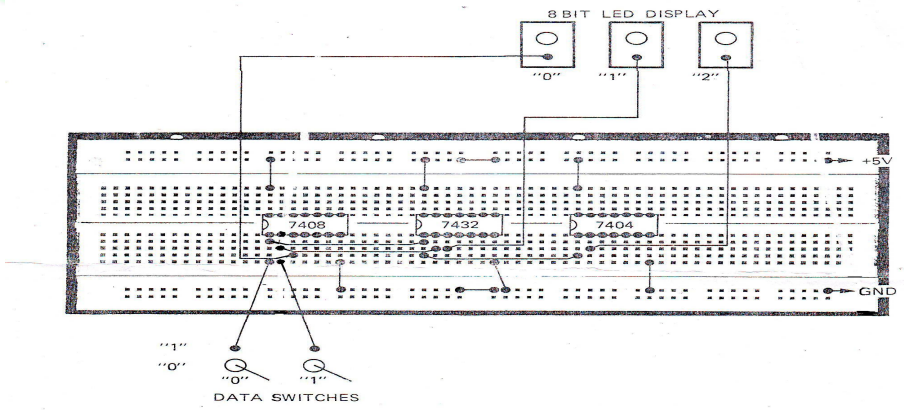


Fig 1—2

Step 4: Change Data Switches "0" and "1" between "0" and "1" position and observe the situation of 8 bit LED Display "0", "1" and "2". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition.

Step 5: Record the results that you have observed into the truth table as follows.

Truth Table 1-3

A	B	Y_1	Y_2	Y_3
0	0			
0	1			
1	0			
1	1			

Discussion & Conclusion:

(On the basis of experimental results)

Session 2: Introduction to Characteristics of NAND and NOR Gates

Session Detail: To verify the input and output relationships/characteristics of 2-input NAND and NOR gates.

Required Instruments and ICs:

1. AT-700 Portable Analog/Digital Laboratory (or AT-800 Modular Lab, AT-701 Personal Lab)

2. 7400(NAND), 7402(NOR)

Circuit Diagram:

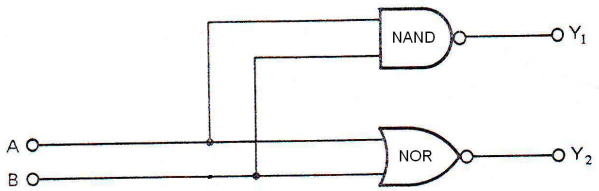
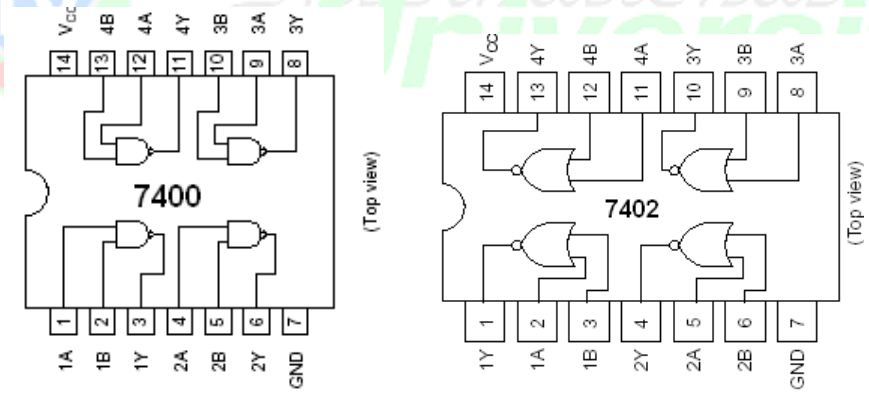


Fig 2–1



Procedure:

Step 1: Find out correctly the input and output pin numbers of each gate.

Step 2: Install the components of Fig 2-1 onto the breadboard of AT-700 and properly check the connections. Remember to connect IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".

Step 3: Connect the Data switches "0" and "1" to point A and B of fig. 2-1 respectively. Then connect 8 bit LED Display's "0" and "1" to the output of point Y1 and Y2 of Fig. 2-1 respectively. The connection diagram is as follows.

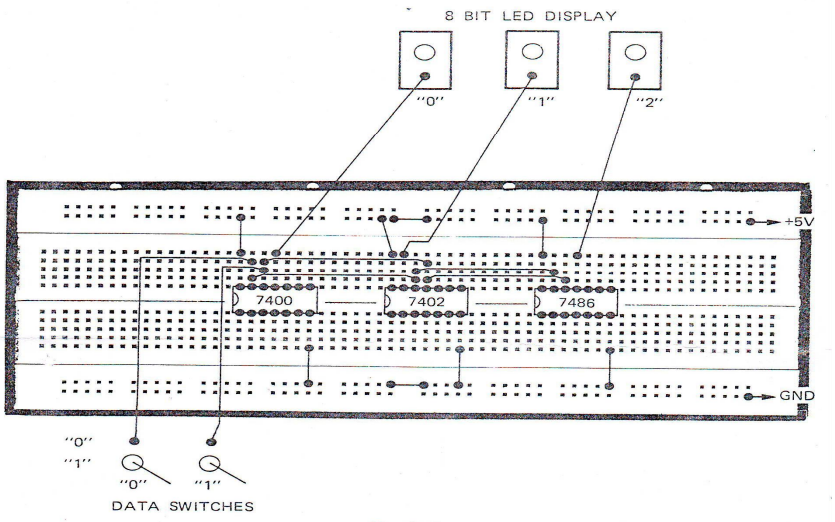


Fig 2–1

Step 4: Change Data Switches "0" and "1" between "0" and "1" position and observe the situation of 8 bit LED Display "0" and "1". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition.

Step 5: Record the results that you have observed into the truth table as follows.

Truth Table 2-2

A	B	Y_1	Y_2
0	0		
0	1		
1	0		
1	1		

Discussion & Conclusion:

(On the basis of experimental results)

Session 3: Verification of De Morgan's Theorem

Session Detail: To verify that A.B = A + B and A+B = A. B by constructing truth tables for both sides of each of these two equations that describe De Morgan's Theorem.

Required Instruments and ICs:

1. AT-700 Portable Analog/Digital Laboratory (or AT-800 Modular Lab, AT-701 Personal Lab)

2. 7404(NOT), 7408(AND), 7432(OR), 7400(NAND), 7402(NOR)

Circuit Diagram:

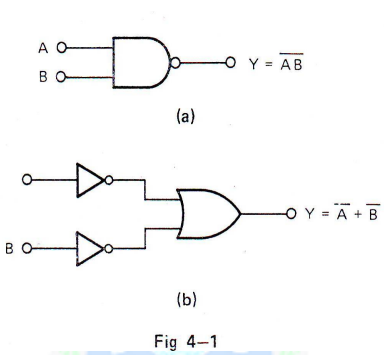


Fig 4–1

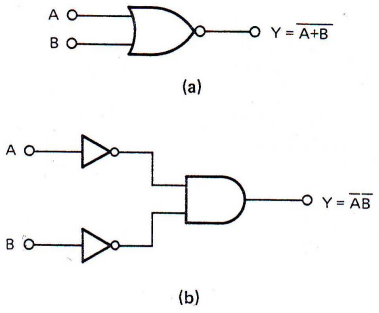


Fig 5–1

Procedure:

Step 1: Install the components of Fig 4-1 onto the breadboard as in Fig 4-2.

Step 2: Connect the Data switches "0" and "1" to point A and B and output "Y" to LED Display "0" of fig. 4-1(a). Connect the Data switches "2" and "3" to point A and B and output "Y" to LED Display "1" of fig. 4-1(b). Refer to Fig 4-2.

Step 3: Change Data Switches "0" and "1" between "0" and "1" position and observe the situation of 8 bit LED Display "0". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition. Record the results into the first empty column of Truth Table 4-3.

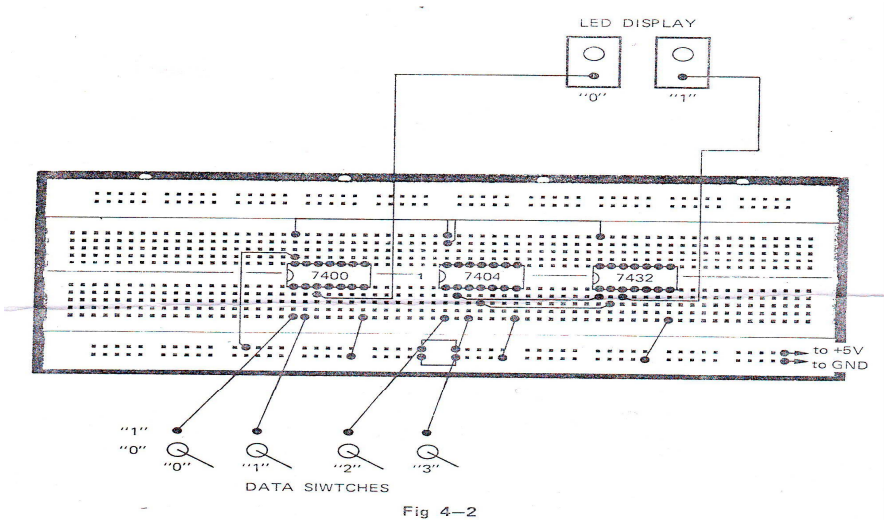


Fig 4—2

Truth Table 4-3

A	B	$Y = \overline{AB}$	$Y = \overline{A}+\overline{B}$
0	0		
0	1		
1	0		
1	1		

Step 4: Change both of the Data Switches "2" and "3" between "0" and "1" position and observe the situation of 8 bit LED Display "1". Record the results into the final empty column of Truth Table 4-3. The results of the last two columns must be identical.

Step 5: Install the components of Fig 5-1 onto the breadboard as shown in Fig. 5-2.

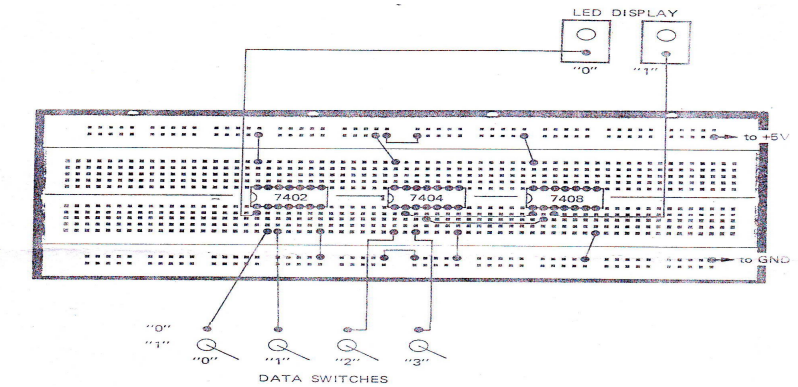


Fig 5—2

Step 6: Connect the Data switches "0" and "1" to point A and B and output "Y" to LED Display "0" of fig. 5-1(a). Connect the Data switches "2" and "3" to point A and B and output "Y" to LED Display "1" of fig. 5-1(b). Refer to Fig. 5-2.

Step 7: Change Data Switches "0" and "1" between "0" and "1" position and observe the situation of LED Display "0". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition. Record the results into the first empty column of Truth Table 5-3.

Truth Table 5-3

A	B	$Y = \overline{A+B}$	$Y = \overline{A}\,\overline{B}$
0	0		
0	1		
1	0		
1	1		

Step 8: Change both of the Data Switches "2" and "3" between "0" and "1" position and observe the situation of 8 bit LED Display "1". Record the results into the final empty column of Truth Table 5-3. The results of the last two columns must be identical.

Discussion & Conclusion:

(On the basis of experimental results)

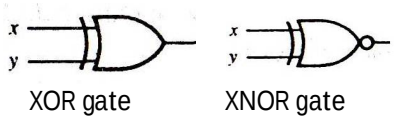
Session 4: XOR, XNOR gates, Parity Generator & Parity Checker Circuits

Session detail: To verify the input-output relationships of XOR, XNOR gates by constructing their truth tables and implement them in parity generator and checker circuits for a 3-bit message.

Equipment Required:

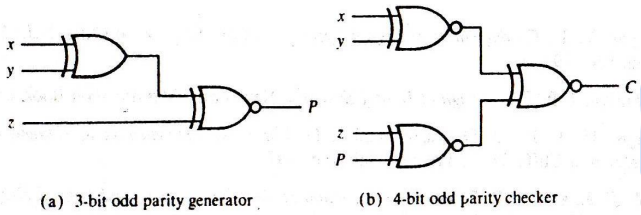
1. AT-700 portable laboratory
2. 7486(XOR), 7481(XNOR)

Circuit Diagram:



XOR gate XNOR gate

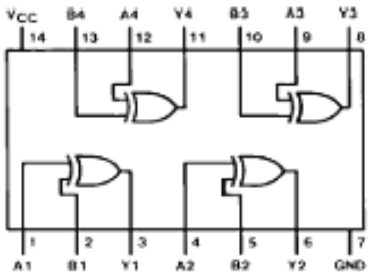
Fig 3-1



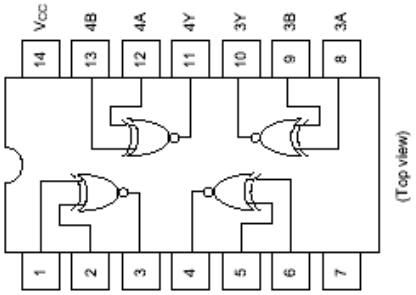
(a) 3-bit odd parity generator (b) 4-bit odd parity checker

Odd parity generator and checker circuits for a 3-bit message

Fig 3-2



Exclusive OR gates



Exclusive-NOR Gates

Procedure:

Step 1: Install the components of Fig 3-1 onto the breadboard of AT-700 and properly link the connections. Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".

Step 2: Connect the Data switches "0" and "1" to point x and y of fig. 3-1 respectively. Then connect 8 bit LED Display's "0", and "1" to the outputs of the XOR and XNOR gates of Fig. 3-1 respectively.

Step 3: Change Data Switches "0" and "1" between "0" and "1" position and observe the situation of 8 bit LED Display "0" and "1". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition.

Step 4: Record the results that you have observed in the following truth table.

Truth Table 3-1

x	y	XOR	XNOR
0	0		
0	1		
1	0		
1	1		

Step 5: Install the components of Fig 3-2(a) onto the breadboard of AT-700 and properly link the connections. The parity generator circuit can also be implemented by the parity checker circuit of Fig. 3-2(b) with the *p* input permanently held at logic "0". Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".

Step 6: Connect the Data switches "0", "1" and "2" to point x, y and z of fig. 3-1 respectively. Then connect 8 bit LED Display's "0" to point *p* of Fig. 3-2(a).

Step 7: Change Data Switches "0", "1" and "2" between "0" and "1" position and observe the situation of 8 bit LED Display "0". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition.

Step 8: Record the results that you have observed in the following truth table.

Truth Table 3-2

Odd parity generation

Three-bit message			Parity bit generated
x	y	z	p
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Step 9: Install the components of Fig 3-2(b) onto the breadboard of AT-700 and properly link the connections. Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".

Step 10: Connect the Data switches "0", "1", "2" and "3" to point x, y, z and p of fig. 3-2(b) respectively. Then connect 8 bit LED Display's "0" to point *C* of Fig. 3-2(b).

Step 11: Change Data Switches "0", "1", "2" and "3" between "0" and "1" position and observe the situation of 8 bit LED Display "0". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition.

Step 12: Record the results that you have observed in the following truth table.

Truth Table 3-3

Odd parity checker

Four bits received				Parity error check
x	y	z	p	c
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Discussion & Conclusion:
(On the basis of experimental results)

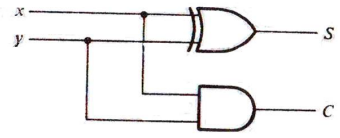
Session 5: Design and Implementation of Full-adder and Half-adder Circuits Using Basic Logic Gates

Session detail: Design and implementation of a Half-adder circuit using basic logic gates and cascade such two circuits to implement a Full-adder circuit.

Equipment Required:

1. AT-700 portable laboratory
2. 7408(AND), 7432(OR), 7486(XOR)

Circuit Diagram:



Truth table

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

FIG. Half-adder Circuit

Truth table

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

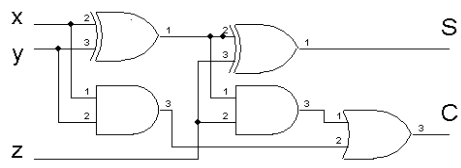
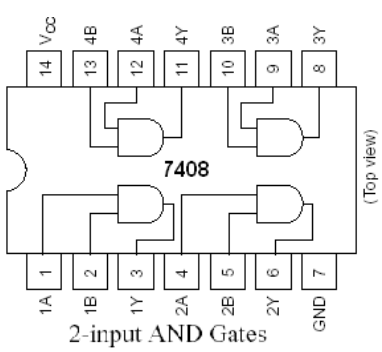
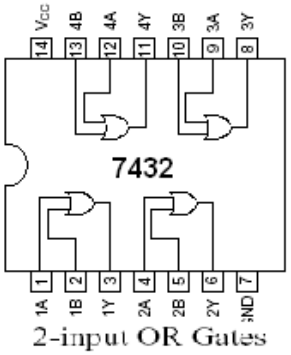
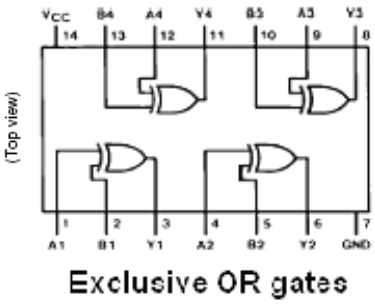


FIG. Full-adder circuit







Procedure:

Half-adder Circuit

Step 1: Install the components for the Half-adder circuit onto the breadboard of AT-700 and properly link the connections.

Step 2: Connect the Data switches "0", and "1" to point x and y of the circuit respectively. Then connect 8 bit LED Display's "0" and "1" to the points C and S respectively.

Step 3: Change Data Switches "0", and "1" between "0" and "1" position and observe the situation of 8 bit LED Display "0" and "1". Verify that the circuit realizes a Half-adder by constructing its truth table and comparing it to the one given in the figure.

Full-adder Circuit

Step 1: Install the components for the Full-adder circuit onto the breadboard of AT-700 and properly link the connections.

Step 2: Connect the Data switches "0", "1", and "2" to points x, y and z of the circuit respectively. Then connect 8 bit LED Display's "0" and "1" to the points C and S respectively.

Step 3: Change Data Switches "0", "1" and "2" between "0" and "1" position and observe the situation of 8 bit LED Display "0" and "1". Verify that the circuit realizes a Full-adder by constructing its truth table and comparing it to the one given in the figure.

Discussion & Conclusion:

(On the basis of experimental results)

Session 6: Design and Implementation of Decoder and Encoder Circuits Using Logic Gates

Session detail:

This experiment is intended for the Implementation of a 2-to-4 decoder and a 4-to-2 encoder circuits using logic gates.

Equipment Required:

1. AT-700 portable laboratory
2. 7404(NOT), 7408(AND), 7432(OR)

Circuit Diagram:

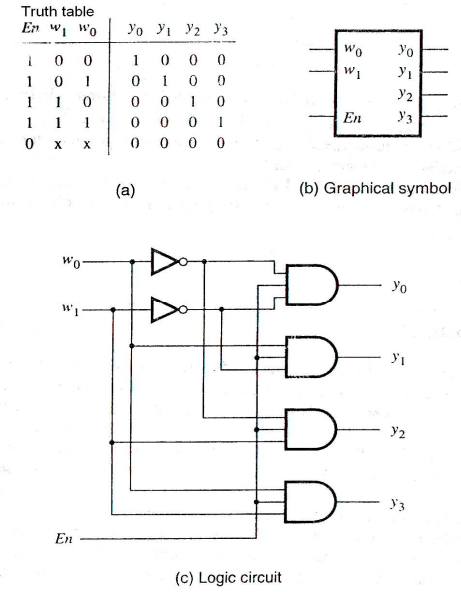


Fig. 8-1: a 2-to-4 Decoder circuit

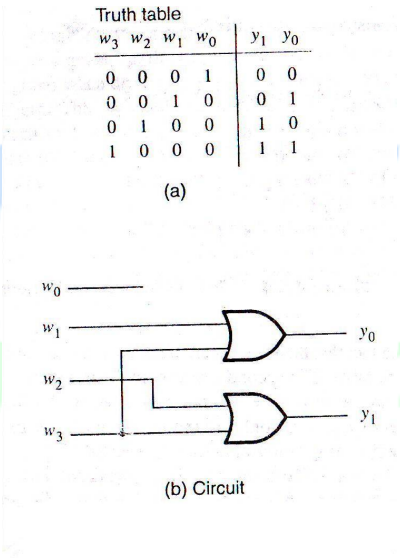
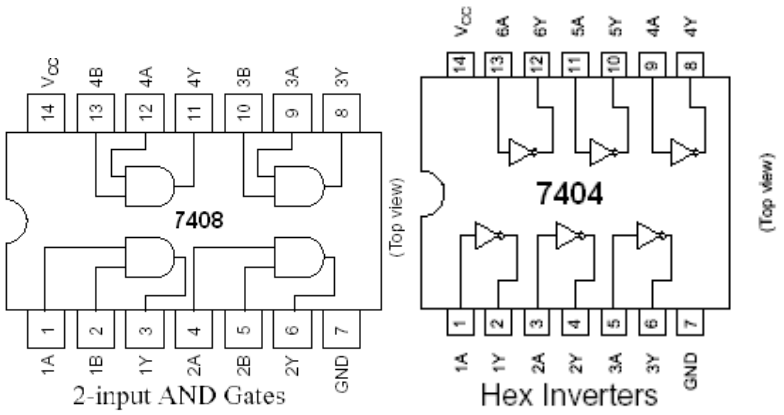
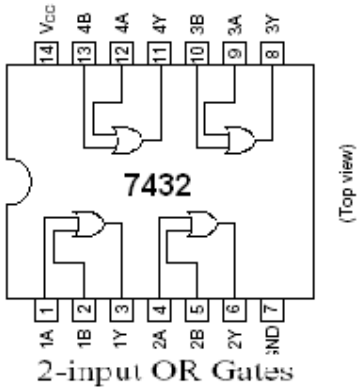


Fig. 8-2: a 4-to-2 Encoder circuit





Procedure:

Step 1: Install the components of Fig 8-1(c) onto the breadboard of AT-700 and properly link the connections. Use two 2-input AND gates to implement a 3-input AND gate. Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".

Step 2: Connect the Data switches "0", "1" and "2" to points *En, w0* and *w1* of fig. 8-1(c) respectively. Then connect 8 bit LED Display's "0", "1", "2" and "3" to the points Y0, Y1, Y2 and Y3 of Fig. 8-1(c) respectively.

Step 3: Change Data Switches "0", "1" and "2" between "0" and "1" position and observe the situation of 8 bit LED Display "0", "1", "2" and "3". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition. Reconstruct and verify the truth table of Fig. 8-1(c).

Step 4: Install the components of Fig 8-2(b) onto the breadboard of AT-700 and properly link the connections. Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".

Step 5: Connect the Data switches "0", "1", "2" and "3" to points *w0, w1, w2* and *w3* of fig. 8-2(b) respectively. Then connect 8 bit LED Display's "0" and "1" to the points Y0 and Y1 of Fig. 8-2(b) respectively.

Step 6: Change Data Switches "0", "1", "2" and "3" between "0" and "1" position and observe the situation of 8 bit LED Display "0" and "1". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition. Reconstruct and verify the truth table of Fig. 8-2(a).

Discussion & Conclusion:
(On the basis of experimental results)

Session 7: Design and Implementation of a Priority Encoder Using Basic Logic Gates

Session detail: To design and implement an 8-to-3 Priority Encoder (with ascending priority) using basic logic gates.

Required Instruments and ICs:

1. AT-700 Portable Analog/Digital Laboratory (or AT-800 Modular Lab, AT-701 Personal Lab)

2. 7404(NOT), 7408(AND), 7432(OR), 7411(3-input AND)

Circuit Diagram:

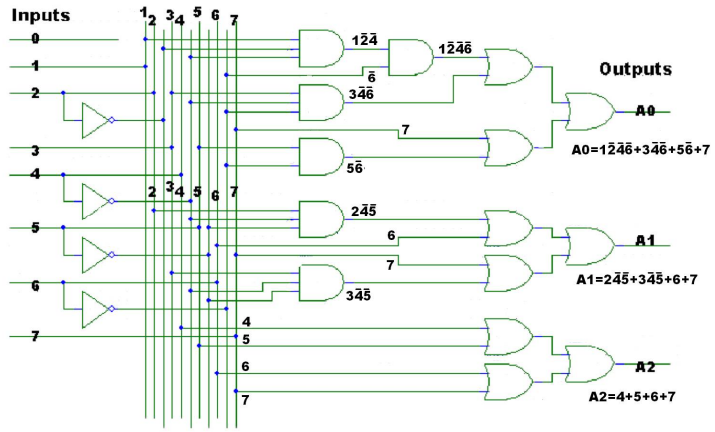
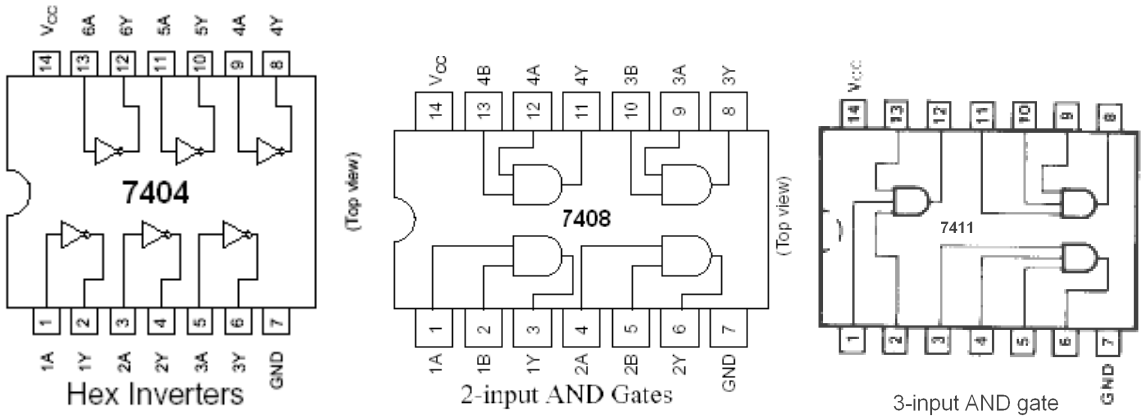


Fig 10-1: an 8-to-3 priority encoder



Procedure:

Step 1: Install the components of Fig 10-1 onto the breadboard of AT-700 and check properly the connections. Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".

Step 2: Connect the Data switches "0"-"7" to the Input lines "0"-"7" of Fig 10-1 respectively. Then connect the 8 bit LED Display's "0", "1" and "2" to the Outputs "A2", "A1" and "A0" of Fig 10-1 respectively.

Step 3: Starting from input "0", make each of the inputs exclusively 'HIGH' in succession. This will demonstrate the basic encoder functionality.

Step 4: Then starting from input "0" again, successively make all the inputs 'HIGH' while keeping the lower order inputs active. This will demonstrate the priority encoder functionality. Tabulate five different input combinations and corresponding encoder outputs.

Discussion & Conclusion:

(On the basis of experimental results)

Session 8: Design and Implementation of Multiplexers

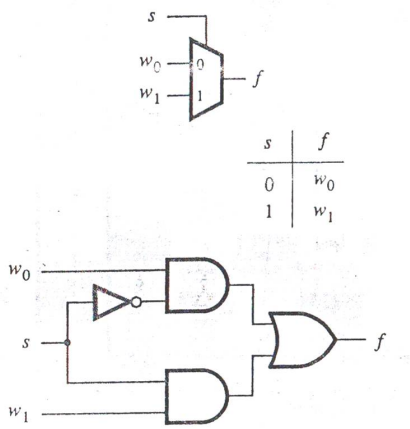
Session detail:

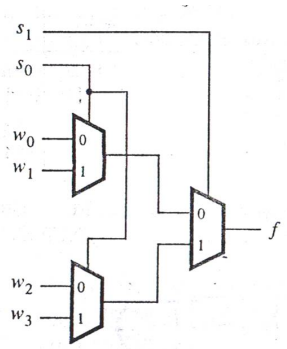
Design and implementation of a 2/1 Multiplexer using logic gates and hence design a 4/1 Multiplexer using 2/1 Multiplexer.

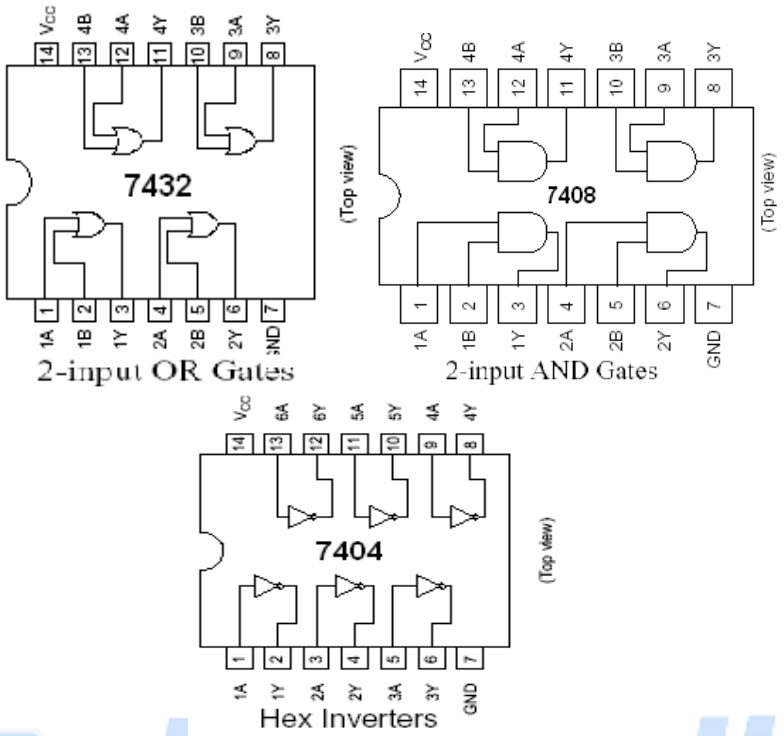
Equipment Required:

1. AT-700 portable laboratory
2. 7404(NOT), 7408(AND), 7432(OR)

Circuit Diagram:







Procedure:

Step 1: Install the components of Fig 10-1 onto the breadboard of AT-700 and properly link the connections. Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".

Step 2: Connect the Data switches "0", "1" and "2" to points *s, w0* and *w1* fig. 10-1 respectively. Then connect 8 bit LED Display's "0", to the point *f* of Fig. 10-1.

Step 3: Change Data Switches "0", "1" and "2" between "0" and "1" position and observe the situation of 8 bit LED Display "0". Verify that the output follows the correct inputs as selected by the selector input *s*.

Step 4: Install the components of Fig 10-2 onto the breadboard of AT-700 and properly link the connections. Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".

Step 5: Connect the Data switches to the inputs *s0, s1, w0, … w3* fig. 10-2. Then connect 8 bit LED Display's "0", to the point *f* of Fig. 10-2.

Step 6: Change Data Switches between "0" and "1" position and observe the situation of 8 bit LED Display "0". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that he output is in the logic 0 condition. Verify that the output follows the correct inputs as selected by the selector inputs *s0* and *s1*.

Discussion & Conclusion:
(On the basis of experimental results)

Session 9: Realization of Logic Function Using Multiplexers

Session detail:

Design and implementation of a circuit using a 4/1 MUX that realizes the logic function *F (A, B, C)* = ∑ *(1, 3, 5, 6)*.

Equipment Required:

1. AT-700 portable laboratory
2. 74153 4-to-1-Line Multiplexer, 7404(NOT)

Logic Diagram:

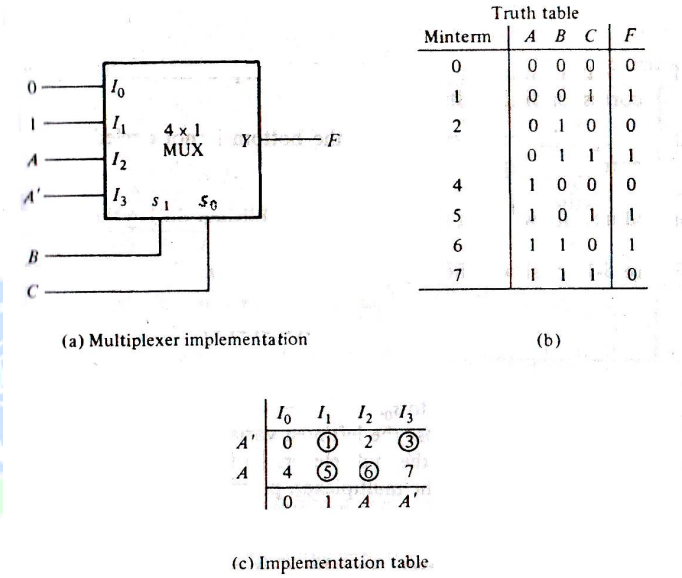


Fig. 11-1: Logic for implementing *F (A, B, C)* = *Σ (1, 3, 5, 6)* with a Multiplexer

Circuit Diagram:

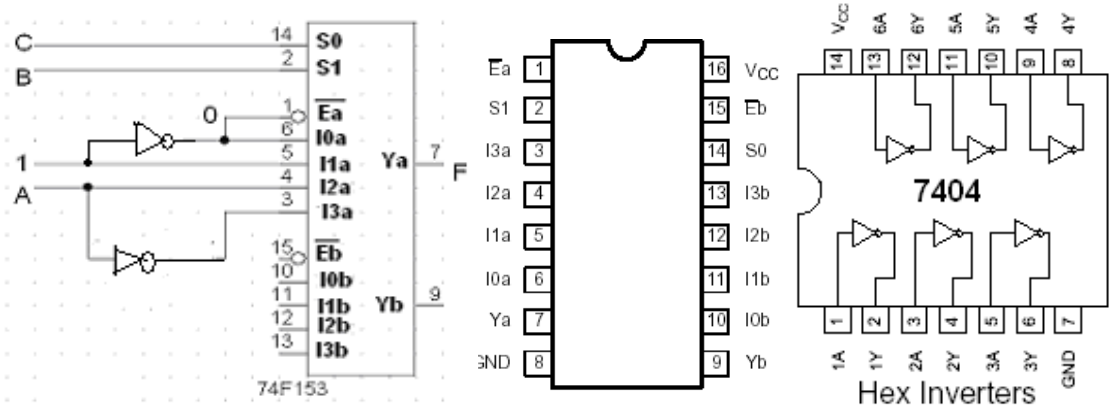


Fig. 11-2: Circuit for implementing *F (A, B, C)* = *Σ (1, 3, 5, 6)* with a Multiplexer

Procedure:

Step 1: Install the components of Fig. 11-2 onto the breadboard of AT-700 and properly link the connections.

Step 2: Connect the Data switches "0", "1", and "2" to point A, B and C of fig. 11-2 respectively. Connect Data switch "3" to point **1** in the figure and keep it at the "1" position. Then connect 8 bit LED Display's "0" to the point F of Fig. 11-2.

Step 3: Change Data Switches "0", "1" and "2" between "0" and "1" position and observe the situation of 8 bit LED Display "0". Verify that the circuit realizes the given function by reconstructing a truth table like that of fig. 11-1(b).

Discussion & Conclusion:
(On the basis of experimental results)

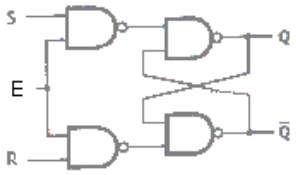
Session 10: Realization of SR Latch Using Integrated Circuit NAND and NOR gates

Session detail: To construct SR latch circuits using NAND and NOR gate ICs separately and verify the input-output relations for both circuits.

Equipment Required:

1. AT-700 portable laboratory
2. 7400(NAND), 7402(NOR)

Circuit Diagram:



Truth Table 4-1

E	S	R	Q(t + 1)
0	x	x	Q(t) (No change)
1	0	0	Q(t) (No change)
1	0	1	0
1	1	0	1
1	1	1	x

Fig. 4-1: SR latch using NAND gates

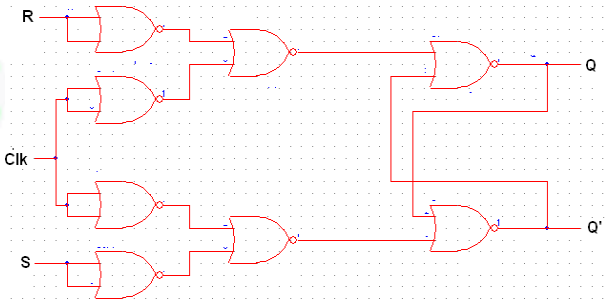
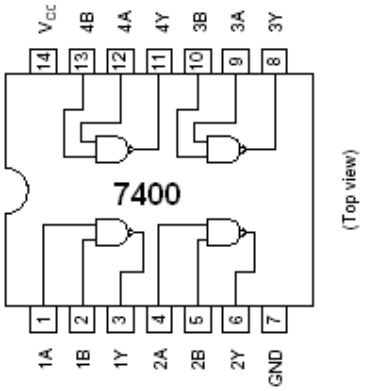
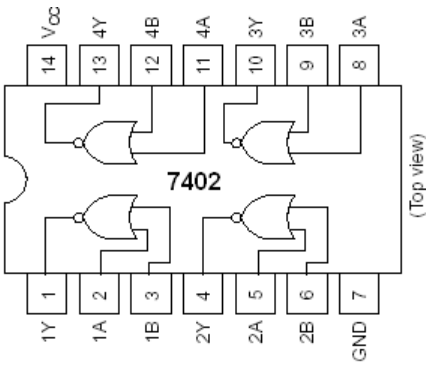


Fig 4-2: SR latch using NOR gates





Procedure:

Step 1: Install the components of Fig 4-1 onto the breadboard of AT-700 and properly link the connections. Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".

Step 2: Connect the Data switches "0", "1" and "2" to point E, S and R of fig. 4-1 respectively. Then connect 8 bit LED Display's "0", and "1" to the outputs Q and Q' of Fig. 4-1 respectively.

Step 3: Change Data Switches "0","1" and "2" between "0" and "1" position and observe the situation of 8 bit LED Display "0" and "1". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition.

Step 4: Record the results that you have observed in the following truth table.

Table 4

E	S	R	Q(t+1)
0	0/1	0/1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Step 5: Repeat **Step 1** to **Step 4** for the circuit of Fig 4-2.

Discussion & Conclusion:
(On the basis of experimental results)