THE UNIVERSITY OF
ALABAMA IN HUNTSVILLE
Department of Electrical and Computer Engineering

CPE 324 Advanced Logic Design Laboratory

Laboratory Assignment #7

Computer Display Interface

(10% of Final Grade)

The purpose of this laboratory project is to improve your basic understanding of computer display technology by developing the necessary logic configuration to drive a SVGA type video display in its 800 x 600 picture element resolution mode.

Background

The Video Graphics Array, VGA, is a video display standard developed by IBM corporation in the late 1980's. An extension of this standard was called the Super Video Graphics Array (SVGA), which supports a resolution of 800 by 600 picture elements (pixels). SVGA compatible monitors are driven in a raster scan manner using three separate analog red, green, blue video signals which are closely synchronized with the digital vertical and horizontal synchronization pulses. These signals were originally developed to drive color Cathode Ray Tube, CRT, monitors and are still often used to drive alternative compatible monitor devices that have been designed to conform to this standard (i.e. LCD flat screens, etc.).

A simplified view of the operation of a CRT is now presented to aid in describing the raster scan process. At one end of the CRT is the phosphor screen and at the other end is an electron gun that produces three beams of electrons that are directed toward the screen. During normal operation, magnetic and electrostatic fields cause the electron beams to leave the electron gun and be deflected to the desired position on the phosphor screen of the CRT resulting in that portion of the screen being illuminated in proportion to the intensity of the beams that strike the phosphor. To achieve color, three types of phosphor dots were placed on the screen near one another at each picture element (pixel) location, one for each of the primary colors of red, green, and blue. During normal operation the electron gun produces three beams that scans across the screen area of the CRT where they illuminate all three dots at various levels of intensity allowing for a wide range of colors to be created for each pixel. In the SVGA standard, these three electron beam intensities are controlled separately by applying the appropriate analog voltage level to the corresponding inputs of the monitor. Since there is a continuous range of voltage levels that are possible for each input the number of colors that can be displayed on the screen is virtually unlimited. In the case of the DE2-115 board, though, the output of three 8-bit digital to analog converter drives the monitor's RGB inputs so the numbers of possible colors is 2^8 x 2^8 x 2^8 = 16,777,216. To decrease the size and complexity of the digital electronics often a color palette is used. In such a case the range of colors that are possible for each pixel are limited (e.g. from 0 to 255 for 8 bits) and each of the color values correspond to specified Red/Green/Blue intensities. This is the method that is employed to represent colors on the DE2-115 in this laboratory.

The Raster Scan Process

Figure 1 shows the pixel configuration for a SVGA monitor. Notice that the pixels are arranged as a two dimensional array of 600 rows by 800 columns. During standard operation, the electron gun scans the screen in the left to right up to down direction to illuminate each of the pixels. As shown in the figure, it begins at the upper left had corner at pixel 0,0 and points to (and illuminates when directed) each pixel along the row going from the left to the right until it points to the last pixel in the row (pixel 799,0). It then should turn off its intensity and quickly retrace back to the left hand side of the screen (in saw-tooth wave manner) at which point it turns itself back on and starts illuminating the selected pixels from left to right along the second row. This process continues this way until all the pixels of the 600 rows have been illuminated in this manner (starting at pixel 0,0). This process is continuous, beginning each time at the upper left most screen postion.

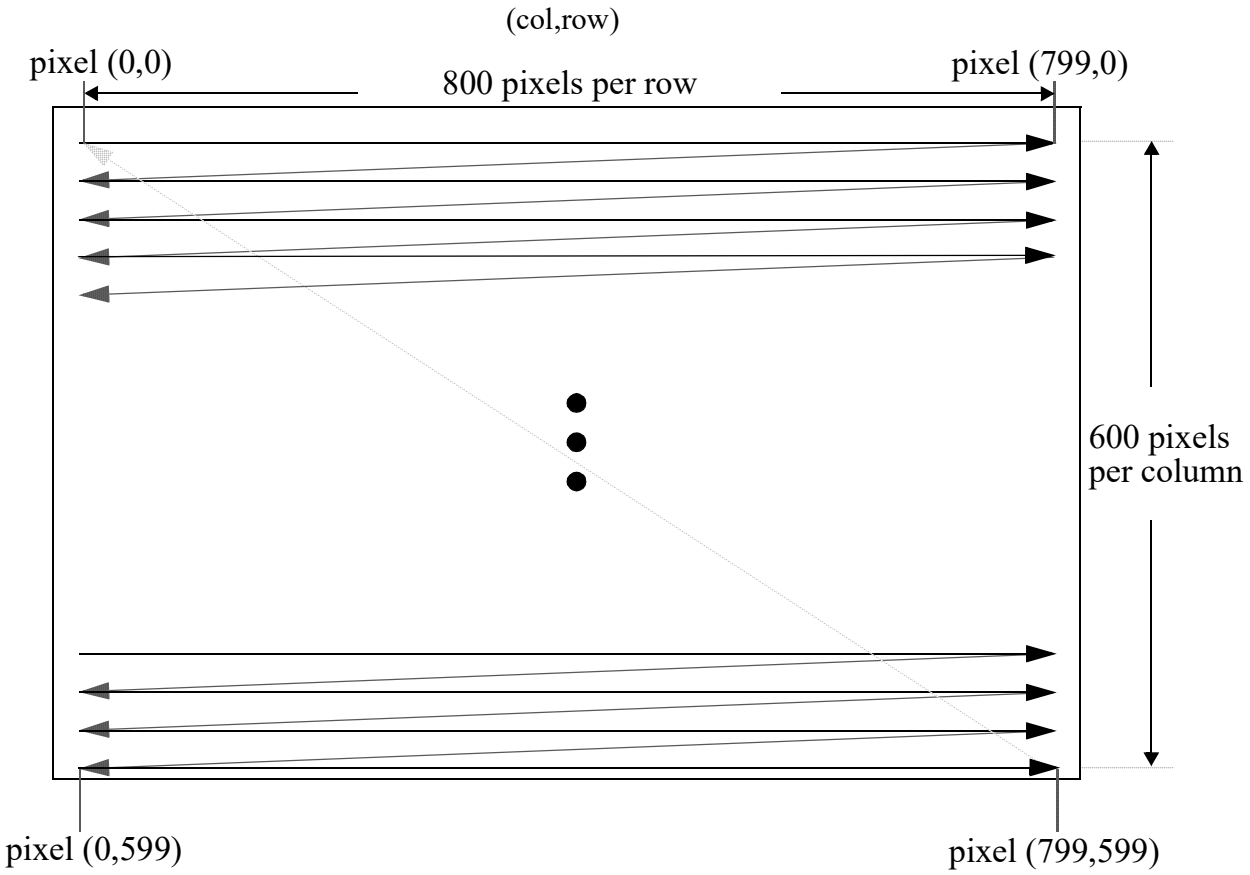
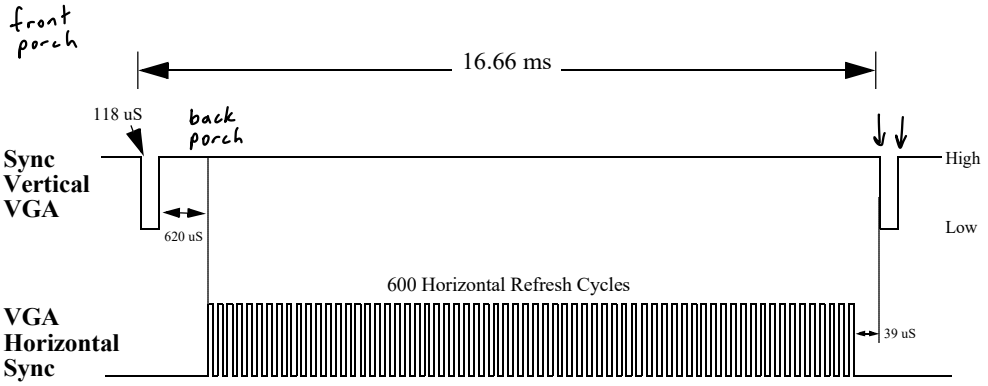


Figure 1: SVGA Pixel Layout and Tracing for 800 x 600 Resolution

All of this of course occurs at a rate that is much faster than the human eye can observe. In one of the SVGA standards the screen has a 60 Hz refresh rate which means that all pixels are updated once every 1/60 of a second. To do this the SVGA monitor uses two synchronization signals. One is the *Vertical Sync* signal which is used to signal the monitor that a new image (frame) is to be displayed and the other one is the *Horizontal Sync* which is used to inform the monitor that a new row is to be displayed. The timing for the corresponding vertical and horizontal refresh cycles are shown in Figures 2 and 3.

$(16666.\overline{6} - 620 - 118)/26.4 = 603$ $\quad 600 + \frac{39}{26.4} = 601$

$(16666.\overline{6} - 620)/26.4 = 608$ $\quad 600 + \frac{39+118}{26.4} = 606$



$\frac{1}{60}\ s = 16.\overline{6}\ ms$

Figure 2: VGA Vertical Refresh Cycle

The detailed timing for the vertical refresh cycle is shown in Figure 2 above. The cycle begins with a 118 us negative going vertical sync pulse, then after a 620 us (back porch) delay (for vertical blanking), and finally 600 horizontal refresh cycles occur one for each of the 600 rows to be displayed. After a 39 us (front porch) delay the cycle repeats itself.

$\frac{16.6\ ms}{26.4\ \mu s} \simeq 631$

Each horizontal refresh cycle, is in turn described by the timing diagram shown in Figure 3. Note that each cycle begins with a 3.2 us negative going horizontal sync pulse, which is followed (after a back porch delay of 2.2 us) by the pixel data. This data is the red/green/blue color intensity information for each of the 800 pixels that will be illuminated along the corresponding row. Note that this will be the RGB pixel intensity data that imparts the color information for each pixel. The rate at which the horizontal sync pulse is set is 37.87 Khz resulting in a pixel update rate that is 40 Mhz. Fortunately a 40 Mhz clock can be obtained by driving one of the Cyclone IV E Phase Lock Loop, PLL, clock inputs with the CLOCK_50 Signal that is on the DE2-115 board and configuring the PLL so that it performs a 4/5 frequency multiplication. During the horizontal sync phase, when the electronic beam is returning to the left-most column to begin the next line, all pixel data should be turned off to avoid seeing the horizontal and vertical retrace lines that are shown in Figure 1.

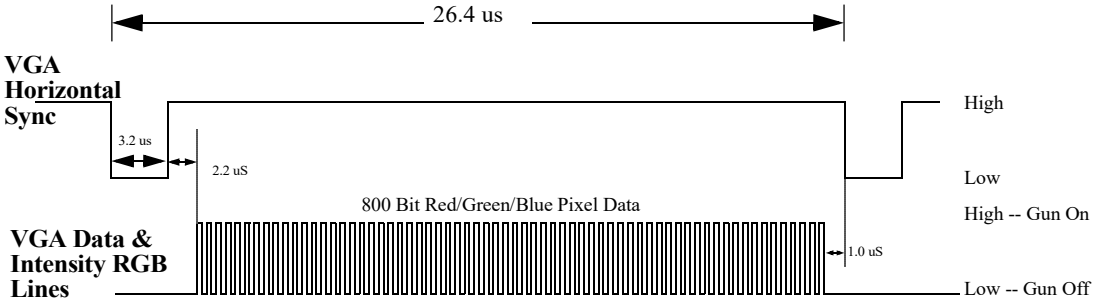


Figure 3: SVGA Horizontal Refresh Cycle

$f = 40\ mHz$

count n = time x frequency

$800 + 1 \times 40 = 840$

$800 + (3.2 + 1) \times 40 = 968$

$16.66\ (40) = 630$

Targeted Design

The design which is to be developed and implemented on the DE2-115 board should drive an SVGA display in a manner that will display a bit-mapped image. The image is a 256 color 256 row x 256 column image of the DE2-115 board. The final design should display a single copy of this image on the center of the 800 x 600 SVGA screen. The image should be transformable to four distinct orientations which are selected by pressing on one of the DE2-115 KEY buttons. When the button labeled KEY[1] is pressed a single copy of the image should appear centered on the SVGA monitor in its normal 256 x 256 pixel resolution. Whenever the KEY[0] key is pressed the same image should appear twice this size in a centered manner on the screen. Whenever the DE2-115 KEY[2] is pressed a centered 90 degree rotated form of the image should appear on the monitor, and whenever the KEY[3] button is pressed on the DE2-115 the same image should appear in normal resolution and centered but upside down (rotated 180 degrees).

Design Overview

A top-level design, shown in Figure 4, has been provided that is composed of five main modules. One of these modules is the *pll_clk_50_to_40* IP core module that is used to obtain a 40 Mhz pixel clock from the available 50 Mhz clock. This module utilizes one of the four Phase Locked Loop, PLL, elements that are present in the Cyclone IV E device. Another IP-core module in the design is *de2_picture* module. This module encapsulates the 256x256 pixel bit map of the DE2 image where each pixel has a 256 value color depth. The inputs to the *de2_picture* module are the pixel clock along with the row and column information that defines the pixel that is being scanned (the most significant 8 bits of the address bus that enter this module represent the row information while the lower least significant 8 bits represent the column information). The actual data that form the bit map gets loaded into the block RAM area of the FPGA on the DE2-115 during the configuration phase (programmer phase) of the process. The *de2_pict_hx.txt* file contains this 65536 bytes of data in a textual form which is encoded as hexadecimal numbers. The file represents the contents from byte location 0 to 65535 where a two dimensional array is created in a row-ordered manner. The *de2_picture* module provides the color information to the *color_palette* module which is used to produce the 256 levels of intensities for each of the red/green/blue components of the display. The 8-bit digital values for each component drives the three digital to analog converters in the DE2-115 strobing them at the pixel clock during the portion of this display cycle when display data is valid.

Note: the Quartus template contains this top-level SVGA Display design in the file lab6.v. The top level module is written in structural Verilog. In addition to the lab6.v, and the DE-2 image file de2_pict_hx.txt is also present in this template.

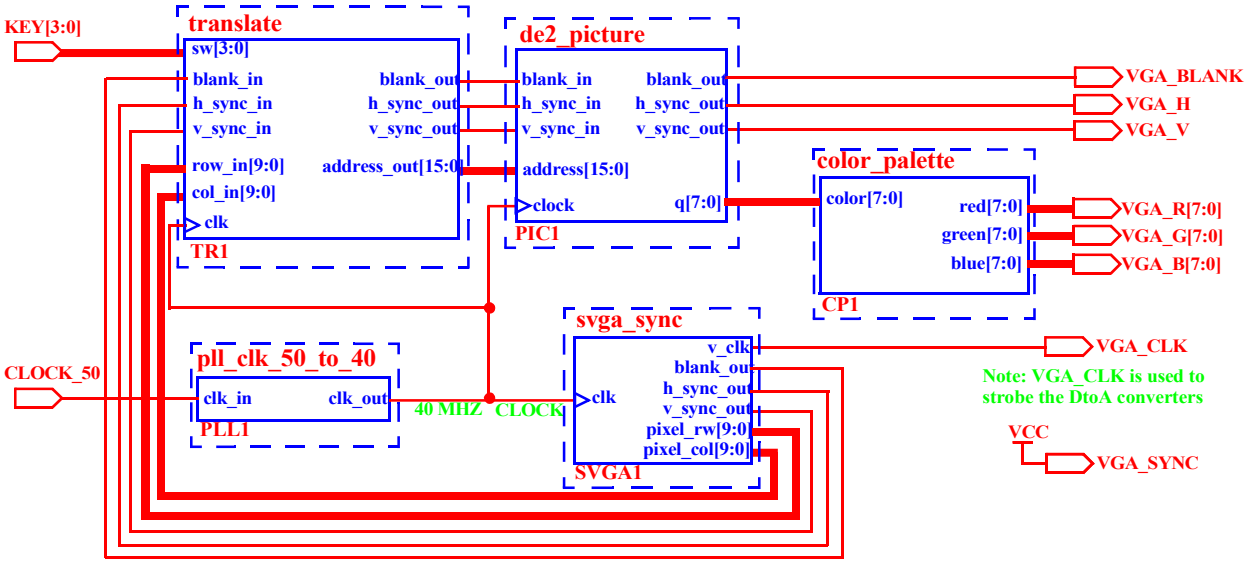


Figure 4: Block Diagram of SVGA DE2-115 Display Driver

The first module that must be completed by the students is the *svga_sync* module which is used to produce the current pixel row and column signals associated with the pixel that is being displayed. These signals are used externally to drive other components in the design and they are used internally to produce the vertical and horizontal synchronization pulses. The second module that must be completed by the students is the *translate* module. This module alters the ordering of the row/column address bus lines that enter the *de2_picture* module to allow the orientation of the image to be changed in four separate ways. The translate module has initially been configured as a stub module to pass and concatenate the 8 lower-order row with the 8 lower-order column lines to form the output that feeds into the *de2_picture* module.

Table 1 presents the DE2-115/Cyclone IV E pin connection information.

Table 1: DE2-115 Cyclone IV E Pin Connection Information

Signal Type	DE2-115 Pin Number(s)	Signal Type	DE2-115 Pin Number(s)
VGA Red (FPGA output)	VGA_R[0] = PIN_E12 VGA_R[1] = PIN_E11 VGA_R[2] = PIN_D10 VGA_R[3] = PIN_F12 VGA_R[4] = PIN_G10 VGA_R[5] = PIN_J12 VGA_R[6] = PIN_H8 VGA_R[7] = PIN_H10	**VGA Horizontal Sync (design output)** **VGA Vertical Sync (design output)**	VGA_H = PIN_G13 VGA_V = PIN_C13
VGA Green (FPGA output)	VGA_G[0] = PIN_G8 VGA_G[1] = PIN_G11 VGA_G[2] = PIN_F8 VGA_G[3] = PIN_H12 VGA_G[4] = PIN_C8 VGA_G[5] = PIN_B8 VGA_G[6] = PIN_F10 VGA_G[7] = PIN_C9	**DE2-115 Push Button Switches (design inputs)**	KEY[0] = PIN_M23 KEY[1] = PIN_M21 KEY[2] = PIN_N21 KEY[3] = PIN_R24
VGA Blue (FPGA output)	VGA_B[0] = PIN_B10 VGA_B[1] = PIN_A10 VGA_B[2] = PIN_C11 VGA_B[3] = PIN_B11 VGA_B[4] = PIN_A11 VGA_B[5] = PIN_C12 VGA_B[6] = PIN_D11 VGA_B[7] = PIN_D12	**DE2-115 50 Mhz Clock (FPGA input)**	CLOCK_50 = PIN_Y2
Additional DE2-115 ADV7123 10-Bit High Speed Video DAC Control Signals (FPGA output) VGA_BLANK = PIN_F11 VGA_SYNC = PIN_C10 VGA_CLK = PIN_A12			

Hardware Reference Documentation for IP Core Elements that are present on the Lab 4 class Canvas Web page.

Teriasic DE2-115 Board User Manual:
https://www.ti.com/lit/ug/tidu759/tidu759.pdf?ts=1677205557524&ref_url=https%253A%252F%252Fwww.google.com%252F

DE2-115 ADV7123 Data Sheet (for DAC used to drive the DE2-115 VGA)
http://www.eecg.toronto.edu/~tm4/ADV7123_a.pdf

Assignment Part 1

Complete the *svga_sync* module so that it implements the required timing functionality to drive the SVGA display in a manner that will display the image of the DE-2 multiple times on the screen. Do not modify the *translate* module at this point. The display should look similar to Figure 5.

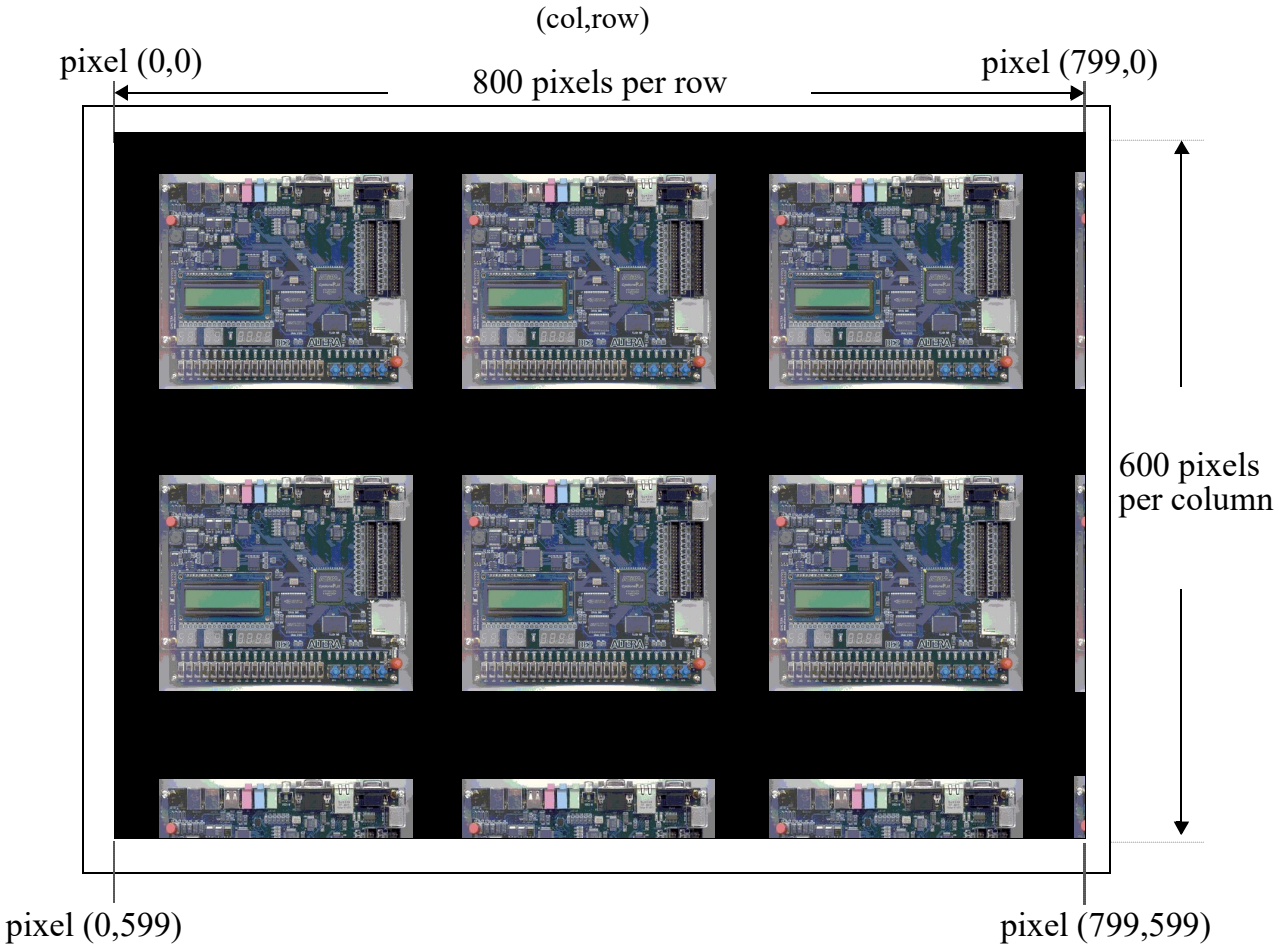


Figure 5: DE2-115 Image Display for Correctly Operating *SVGA_SYNC* Module

Assignment Part 2

After the completion of the *svga_sync* module, students are asked to modify the *translate* module so that it will respond to the *KEY[0]* -- *KEY[3]* buttons that are present on the DE2-115 board. The *translate* module should produce a single DE-2 image that is centered and with the display blanked, whenever the raster scan is not at a pixel location that corresponds to the region on the screen where the image is to be displayed. This can be accomplished by causing the *translate's BLANK_OUT* signal to be at a logic 0 for portions of the display that do not contain the image. The *KEY[0]* -- *KEY[3]* are momentary active low switches, which means that they are normally logical high until pressed. The design should respond to the pressing of these keys by changing the orientation in the following manner when the key is pressed. When the button labeled *KEY[1]* is pressed a single copy of the image should appear centered on the SVGA monitor in its normal 256 x 256 pixel resolution. Whenever the *KEY[0]* key is pressed the same image should again appear in the center of the screen but this time it should be twice its normal size. Whenever the DE2-115 *KEY[2]* is pressed a centered image should appear. This image should be rotated 90 degree counter-clockwise. Finally whenever the *KEY[3]* button is pressed on the DE2-115 the same image should appear in normal resolution and centered but upside down (rotated 180 degrees).

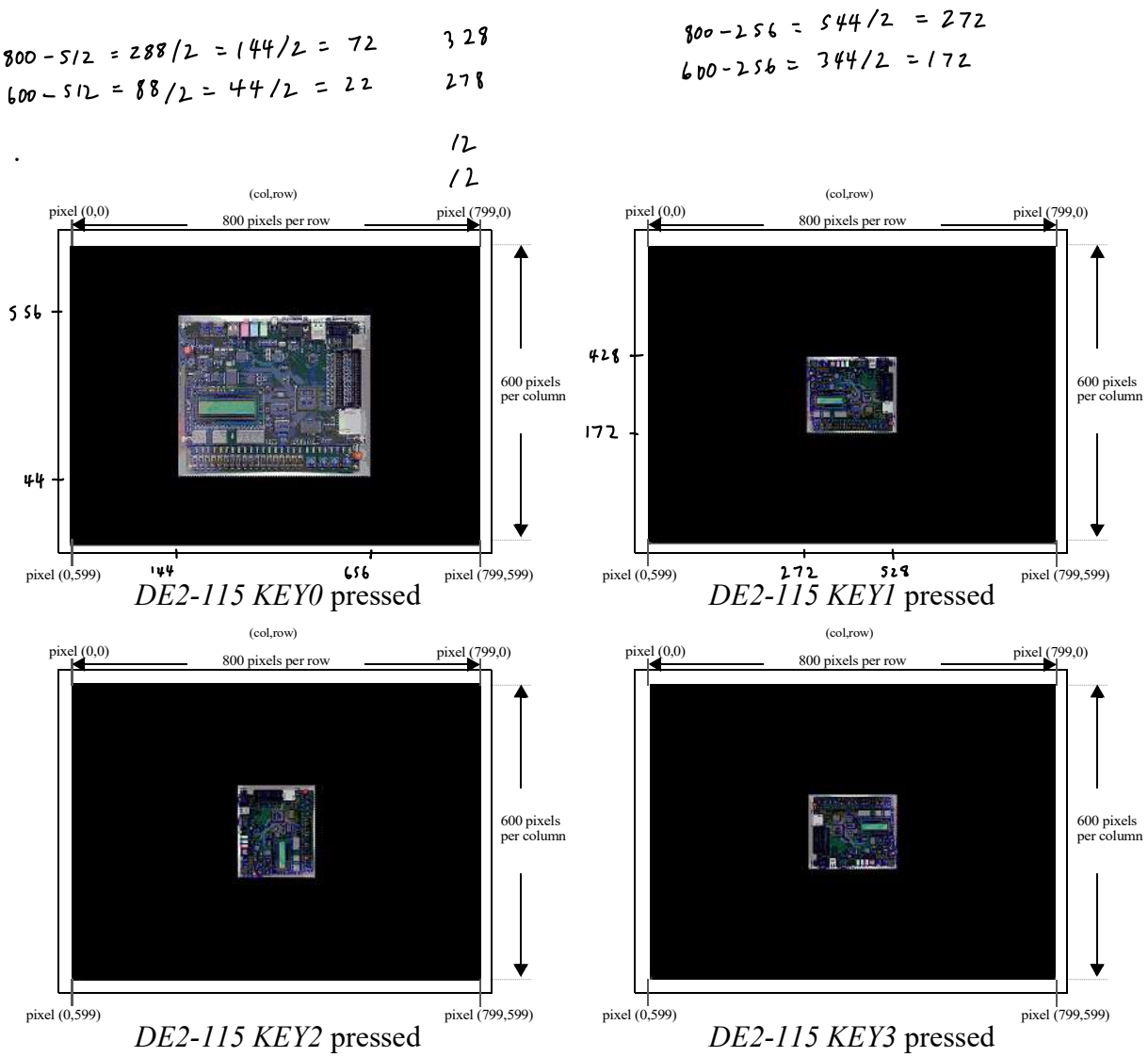


Figure 6: DE2-115 Image Translations supported by a Completed Correctly Operating SVGA DE2-115 Display Design

Students are to fully demonstrate each portion of their design to their laboratory instructor. A standard laboratory report should be completed which highlights the results of this laboratory as well as answers the following post laboratory questions. This report is due by the beginning of the next laboratory session or as directed by the laboratory instructor.

Post Laboratory Questions

Students are also expected to answer the following questions that reflect upon their laboratory experiences. The answers to these questions should be part of their laboratory report.

1. What kind of compilation errors or warnings did you encounter? How did you correct the errors and how did you determine which warnings could be ignored?
2. Explain briefly how a phase-lock-loop can be used to multiply and divide external clock frequencies that are used to drive logic within an FPGA such as the Cyclone IV E.
3. What is the purpose of the *pll_clk_50_to_40* IP core module that was incorporated in the design? Is it possible to generate a 40 Mhz clock signal from a 50 Mhz one that is present on the DE2-115? Could you module to create a 40 Mhz clock from a 27 Mhz clock if this clock speed was available on the DE2-115 board instead of the 50 Mhz clock? If so, explain how you would do this. If not explain why this is not possible.
4. What is the purpose and function of the *de2_picture* IP core module? From the reports generated by the Quartus compilation/synthesis/map/place/route process what are the type and number of FPGA internal resources that were used for this module? For the memory element(s) that were employed in the module did Quartus treat them as a combinational ROM type element or as a synchronous Block ROM? Explain your answer?
5. What is the purpose and function of the *color_palette* IP core module? From the reports generated by the compilation/synthesis/map/place/route process what are the type and number of FPGA internal resources that were used for this module? For the memory element(s) that were employed in the module did Quartus treat them as a combinational ROM type element or as a synchronous Block ROM? Explain your answer?