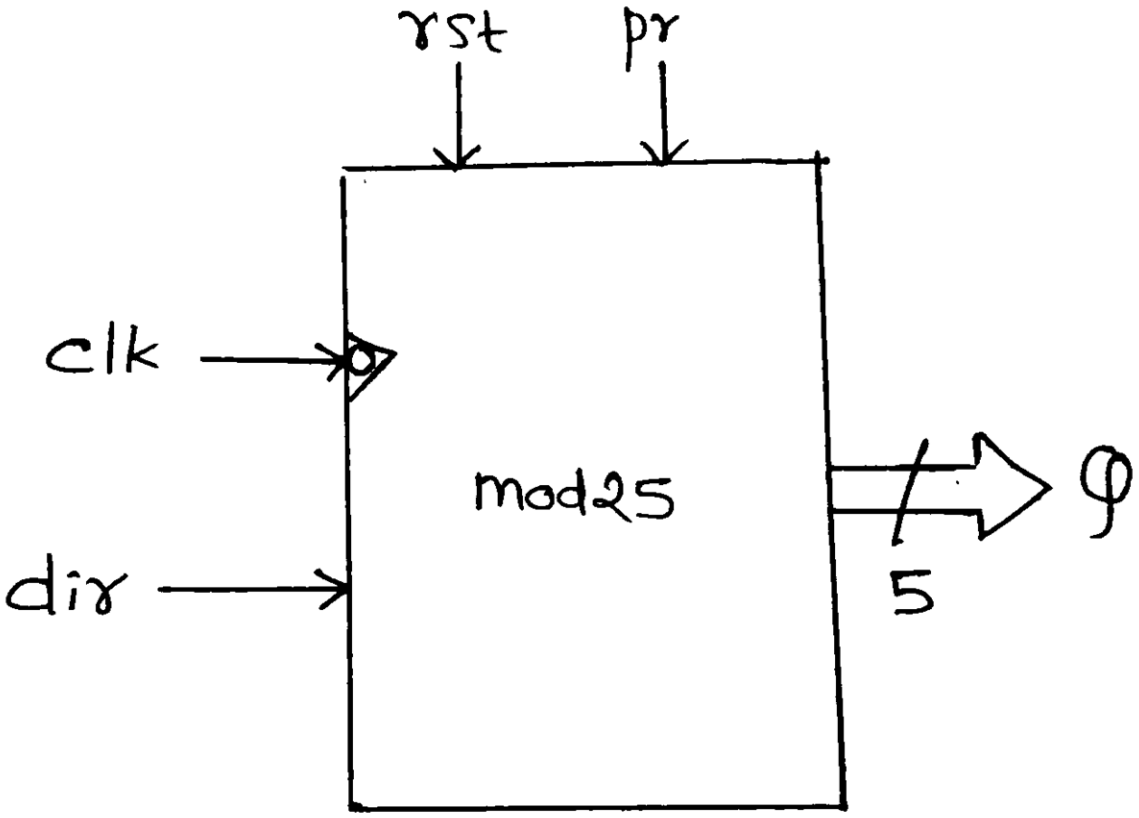
## BLOCK DIAGRAM




## FUNCTION TABLE

| rst | pr | clk | dir | $Q_{n+1}$ ( Next State ) | Operation |
|---|---|---|---|---|---|
| 1 | 0 | x | x | 00000 | Reset |
| 0 | 1 | x | x | 11111 | Set |
| 0 | 0 | ↓ | 1 | $Q_n + 1$ | With Counter Set to Q = 00000 $(0)_{10} \rightarrow (24)_{10}$ |
| 0 | 0 | ↓ | 0 | $Q_n - 1$ | With Counter Preset to Q = 11111 $(31)_{10} \rightarrow (7)_{10}$ |

**MAIN VHDL MODEL ( MVM ) / ARCHITECTURE BODY**

```
architecture mod25_arch of mod25 is

signal Qtemp : STD_LOGIC_VECTOR (4 downto 0) := "00000";

begin
        process(rst,pr,clk,dir)

        begin
                if rst ='1' then
                        Qtemp <= (OTHERS =>'0');
                elsif pr='1' then
                        Qtemp <= (OTHERS =>'1');
                elsif falling_edge(clk) then
                         if dir = '1' then
                                        if Qtemp < 24 then
                                                Qtemp <= Qtemp + 1;
                                        else
                                                Qtemp <= "00000";
                                        end if;
                                 else
                                        if Qtemp > 7 then
                                                Qtemp <= Qtemp - 1;
                                        else
                                                Qtemp <= "11111";
                                        end if;
                        end if;
                end if;

        end process;
        Q<=Qtemp;


end mod25_arch;
```