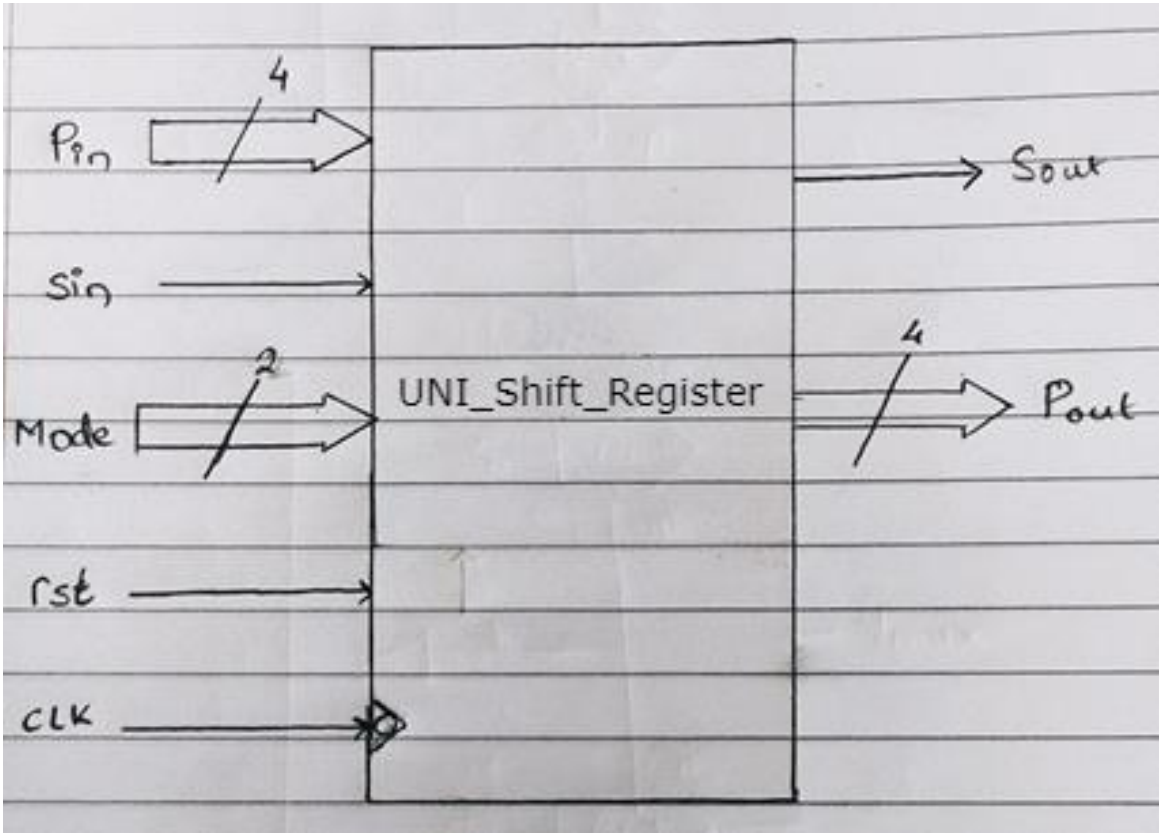
BLOCK DIAGRAM



FUNCTION TABLE

rst	clk	MODE		Output
		M(1)	M(0)	
1	X	X	X	X
0	↓	0	0	Serial In Serial Out (SISO)
0	↓	0	1	Serial In Parallel Out (SIPO)
0	↓	1	0	Parallel In Serial Out (PISO)
0	↓	1	1	Parallel In Parallel Out (PIPO)

MAIN VHDL MODEL (MVM) (ARCHITECTURE BODY)

```
architecture UNI_Shift_Register_arch of UNI_Shift_Register is
SIGNAL temp : STD_LOGIC_VECTOR (3 downto 0):="0000";
        begin
                PROCESS(rst, clk, mode, Sin, Pin)
                BEGIN
                        IF rst = '1' THEN
                                Pout <= "0000";
                                Sout <= '0';

                        ELSIF FALLING_EDGE(clk) THEN

                                CASE mode IS

                                        WHEN "00" =>
                                                temp(3 downto 1) <= temp(2 downto 0);
                                                temp(0) <= Sin;

                                                Sout <= temp(3);
                                                Pout <= "0000";

                                        WHEN "01" =>
                                                temp(3 downto 1) <= temp(2 downto 0);
                                                temp(0) <= Sin;
                                                Pout <= temp;
                                                Sout <= '0';

                                        WHEN "10" =>
                                                temp <= Pin;
                                                Sout <= temp(3);
                                                temp(3 downto 1) <= temp(2 downto 0);
                                                Pout <= "0000";

                                        WHEN OTHERS =>
                                                Pout <= Pin;
                                                Sout <= '0';

                                END CASE;
                        END IF;
                END PROCESS;

end UNI_Shift_Register_arch;
```