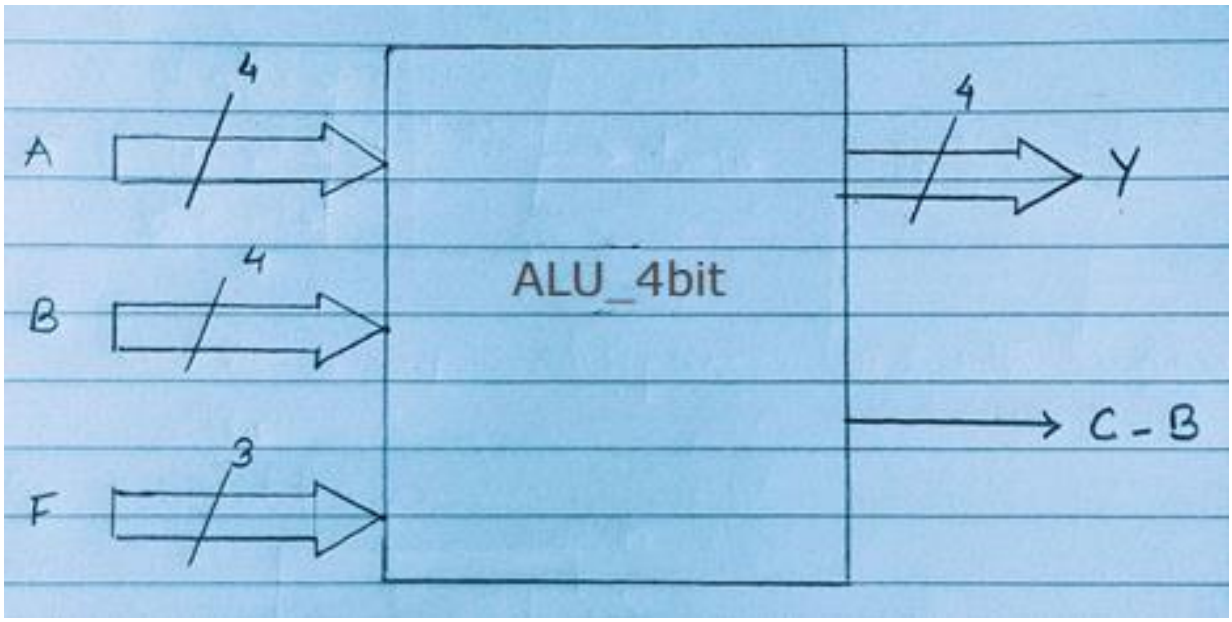
BLOCK DIAGRAM



FUNCTION TABLE

F			Y	C_B
F(2)	F(1)	F(0)		
0	0	0	A.B	0
0	0	1	$\overline{A.B}$	0
0	1	0	A+B	0
0	1	1	$A \oplus B$	0
1	0	0	$\overline{A \odot B}$	0
1	0	1	$\overline{A+B}$	0
1	1	0	ADDITION $A + B$	carry
1	1	1	SUBTRACTION $A - B$	borrow

MAIN VHDL MODEL (MVM) (ARCHITECTURE BODY)

```
architecture ALU_4bit_arch of ALU_4bit is

signal result:STD_LOGIC_VECTOR(4  downto 0):="00000";

begin

process(A,B,F)
begin

   CASE F IS

      when "000" =>
         result <= '0' & (A AND B);

      when "001" =>
         result <= '0' & (A NAND B);

      when "010" =>
         result <= '0' & (A OR B);

      when "011" =>
         result <= '0' & (A XOR B);

      when "100" =>
         result <= '0' & (A XNOR B);

      when "101" =>
         result <= '0' & (A NOR B);

      when "110" =>
         result <= ('0' & A)+('0' & B);

      when others =>
         if A < B then
            result <= '0' & (NOT B);
            result <= result+1;
            result <= ('0' & A) + result;
            result <= (NOT result) +1;
            result <= (NOT(('0' & A) + ('0' &(NOT B)) + 1))+1;
         else
            result <=('0' & A)-('0' & B);
         end if ;

   end CASE;
end process;
Y <= result(3 downto 0);
C_B <= result(4);

end ALU_4bit_arch;
```