VLSI Design Tools & Technology (VDTT) Programme

Dated: 30.11.2021

Subject: Minutes of VDTT PEC meeting held on November 30, 2021 at 3.30 pm online through MS-Teams

Short-listing criteria in the MS-R programme of VLSI Design Tools and Technology *(JVY)*

The Programme Executive Committee (PEC) of the VDTT programme met on 30th November 2021 at 3.30 pm for short-listing of MS(R) applications.

VDTT is a fully sponsored programme, and the sponsors will have to interview the candidates. As such direct admission through GATE score does not apply to the VDTT programme.

The following short listing criteria were decided over and above the minimum eligibility condition as laid out in the prospectus. The short-listing criteria and admission procedure are identical for the MS-R programme.

i) **Direct admission (Full time with GATE): Nil**

ii) **Call for interview (Full time with GATE):**

GATE Discipline	**Minimum GATE Score**		
	GE, OBC, GEN-EWS	**SC, ST, PwD**	**Minimum degree performance**
EC	830	730	**Minimum 6.0/10 CGPA or 60% for GE/OBC/EWS, 5.5 CGPA or 55% for SC/ST/PwD**
EE	830	730	
CS	700	600	
IN	930	800	
Others	930	800	
IIT and CFTIs B.Tech	-	-	CGPA ≥ 8.0/10

iii) **Call for interview for Full-Time sponsored, Part-Time Regular & Part-Time Industry sponsored candidates (Part-time):**

A. Candidates should be an employee of a sponsoring company with a signed MoU with the VDTT programme, or a written commitment to the effect that a MoU would be signed in due course.

B. He/She should have a minimum of 1 year experience.

C. He/she should have a minimum 85% or 8.5 CGPA in UG.

The candidates will be screened by IITD faculty on December 09, 2021, followed by an interview of the shortlisted candidates with the sponsors on December 11, 2021.

Submitted for your kind approval.

S. Chatterjee

(Prof. Shouri Chatterjee)
Coordinator, VDTT Programme

✓ **Dean (Academics)**

Copy to PEC members