VLSI DESIGN TOOLS AND TECHNOLOGY (VDTT) PROGRAMME

Dated: 15.5.17

The following full time candidates have been tentatively short-listed for interview with the sponsors on 16th May 2017. All the candidates are required to report to Room No. LHC-410 at 9:15 AM tomorrow.

Full Time:

Application No.	Name
14900	Alok Keshattiwar
4741	Abhimanyu Sharma
23236	Akashdeep Singh
24694	Ashish Gusain
27710	Ayush Jain
6733	Karan Goyal
11886	Kaustubh Dave
15280	Manish Kumar
9964	Rupesh Pandey
3560	Sanchar Palit
6371	Saurabh Gupta
9244	Saurabh Mathur
7149	Sharij Kumar
6629	Shashank Varshney
18988	Srishti Gupta
7087	Suraj Panwar
6436	Surajit Ghosh
5490	Tanya Gupta
6748	Vaibhav Gupta
6649	Vijay Sharma
19960	Vitthal Sharma
11953	Yash Bansal

Part Time:

5995	Deep Narula

The list is arranged in alphabetical order of the names of short listed candidates and does not reflect the merit list.

(Prof. Jayadeva)
Coordinator, VDTT Programme