VHDL Assignment-2

1. Develop a sequential circuit and VHDL code that has a single data input S, and produce output Y. The output is 1 whenever S has the same value over three successive clock cycles, and 0 otherwise. Assume that the value of S for given clock cycle is defined at the time of rising clock edge at the end of the clock cycle. Also find out the number of clock cycle required in pipeline circuit to get output from input.
2. Suppose a factory has a VAT with a sensor that output 1 when the VAT is empty, 0 otherwise. The VAT also has a pump to empty it and a control switch to active the pump. Devise a circuit that turns the pump on when the switch is set to activate the pump and the VAT is not empty. Design the code using VHDL behavioral and data flow model on the circuit you have drawn.
3. Design a BCD to 7 segment display by AND OR logic and write the same first by data flow model and then by structural model.
4. Design a 3 bit 2 to 1 MUX using VHDL
5. Develop a VHDL code of a 4 to 1 MUX that selects among four unsigned 6 bit integer.
6. Develop a VHDL behavioral model of an Adder/subtracter for 12 bit unsigned binary number. The circuit has data input x and y, a data output s, a control input mode that is 0 for addition and 1 for subtraction. Also choose a bit for addition overflow or subtraction underflow.
7. Develop a VHDL model to convert a 4 bit Gray code to a 4 bit unsigned binary integer.
8. Write a code for the following testing algorithm- Identify two unsigned binary number for which a ripple carry adder exhibits its worst delay.
9. Develop a VHDL code by using behavioral and data flow model for a pipe line circuit that computes the average of corresponding values in three streams of input values a,b,c. The condition in pipeline is , it consists of three stages : the first stage sums value a and b and saves the value c; the second stage adds on the saved value of c; third stage divides the three. Input and output are all signed fixed point number indexed from 5 downto – 8.
10. Write a code in VHDL for a free running counter that counts 32 clock cycle and produce control, signal that is 1 during every 4^{th}, 20^{th} and 24 th cycle.
11. Develop a VHDL model of a debouncer for push button switch that use debounce interval of 10ms. System clock frequency is 50MHz.