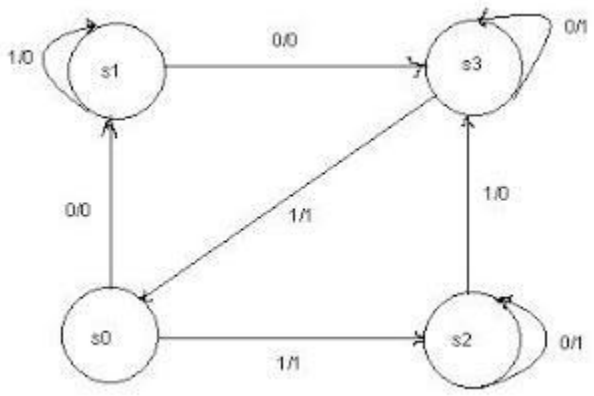
Assignment -3

1. The state machine bubble diagram in the below figure shows the operation of a four-state machine that reacts to a single input "input" as well as previous-state conditions. Write the code.



2. Write a test bench code for simple vending machine.

3. A Cyclic Redundancy Check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. There are many CRC polynomials available, used depending on the specific application. write the code for 8 bit in size known as CRC-8-CCITT. Also write the test bench of this CRC code.

4. Write a VHDL code to find out **square root** of a unsigned number

5. Write a Test bench for N bit serial adder

6. Write a VHDL code that can count number of one in a 16 bit binary number.

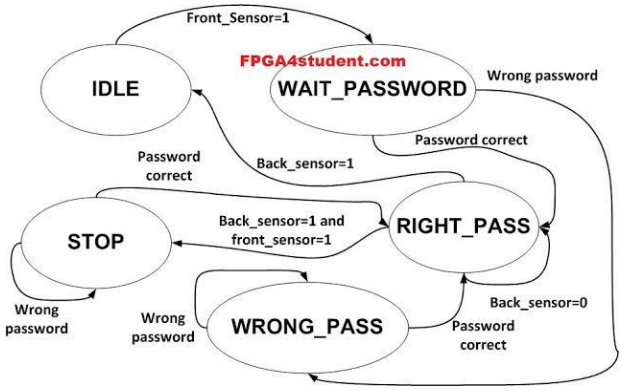
7. Write a VHDL code for 8-bit bus that feeds and receives feedback from bidirectional pins.

8. Write a code on 8-bit signed multiplier by using VHDL.

9. Design a Sequence Recognizer where you need to build a finite state machine that will recognize the sequence x = 0110 and output the sequence z = 0001 as this sequence occurs. In other words, output z = 0 when first receiving x = 0. Then output z = 0 if the next bit of x = 1; output z = 0 again if the following bit of x = 1. Finally, if the last (fourth) bit of x = 0, output z = 1. More simply, output z = 0 until the sequence x = 0110 is received, at which time output z = 1.

10. Implement the logic of Tug of War game and write the code by using VHDL.

11. The car parking system in VHDL operates under the control of a Finite State Machine (FSM) as follows. Write the code in VHDL

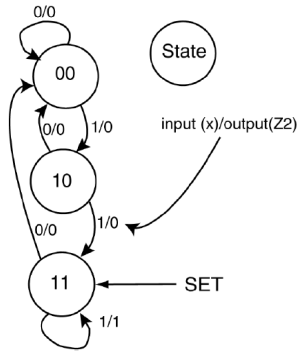


12. Develop a VHDL code for pipelined circuit that computes the average of corresponding values in three streams of input values a,b, c. The pipeline consists of three stages: the first stage sums value of a,b and save the value of c; the second stage adds on the saved value of c; and the third stage divides by three. The input and output are all signed fixed point number indexed from 5 down to -8.

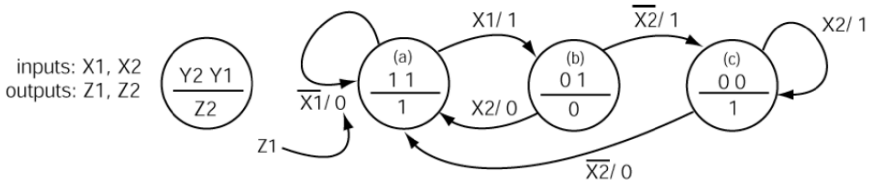
13. Design and write the code that counts 16 clock cycle and produce a control signal - CTRL that is 1 during every eight and twelfth cycle.

14. Write a VHDL model for a 12 bit register that stores an unsigned integer value.

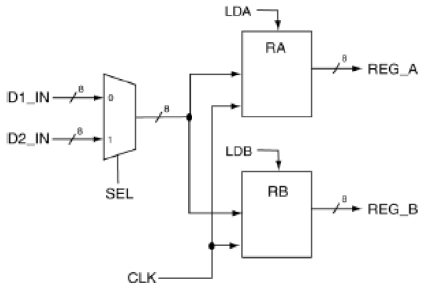
15. Write the code in VHDL for the following FSM - Use a dependent PS/NS coding style . Consider the state variables as output of the FSM.



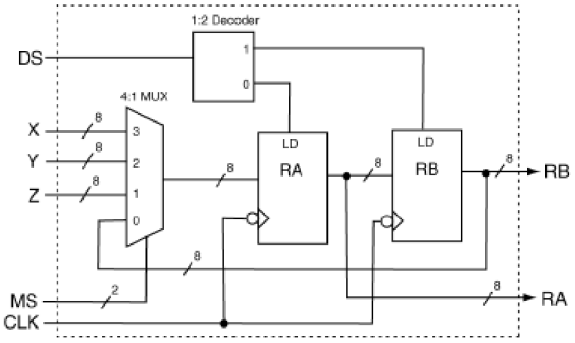
16. Write the VHDL code of following FSM



17. Use VHDL behavioral modeling to design the circuit shown on the right. Consider both the loading signals to be active high. Consider the circuit to be synchronized to the rising edge of the clock signal. It includes two 8-bit registers and a 2:1 MUX. This is an example of a bus-based data transfer in the output of the MUX that is connected to the inputs of the two registers.



18. Provide a VHDL model that can be used to implement the following circuit.



19. Write some programme on Test Bench (from assignment -1)