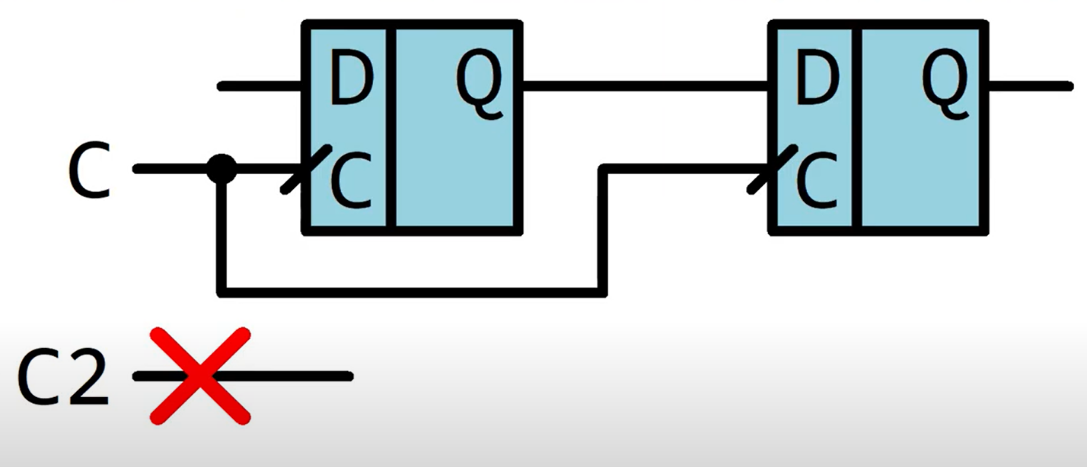
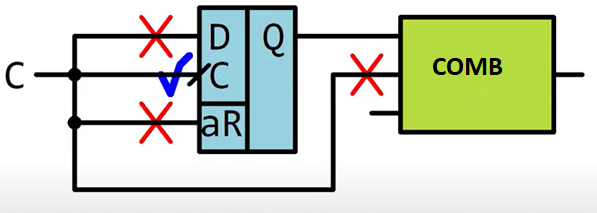
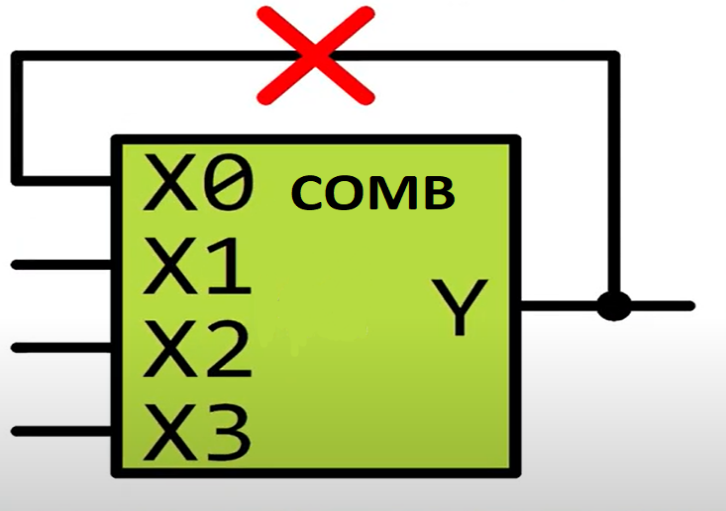
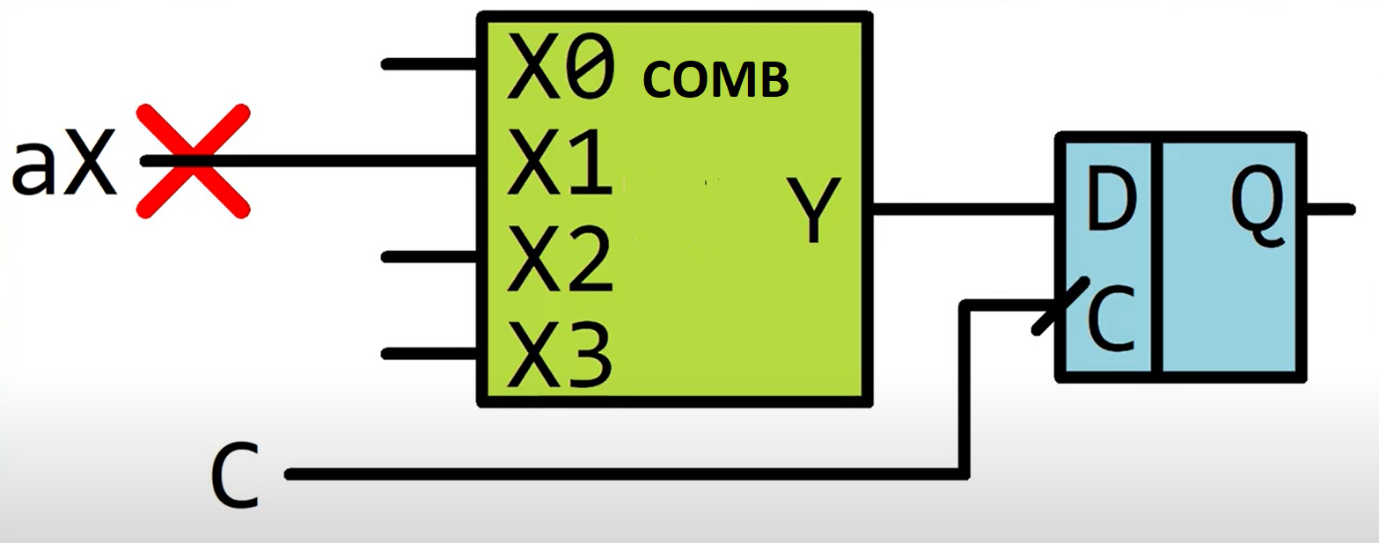
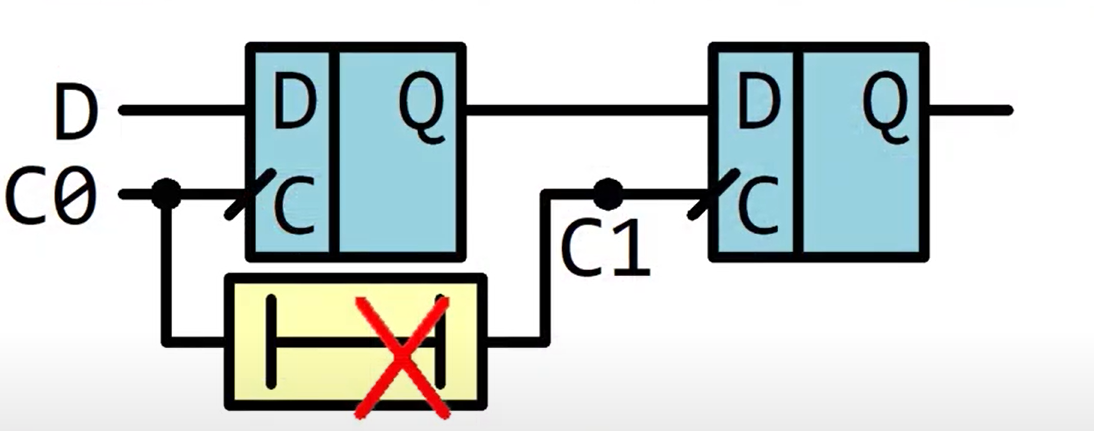
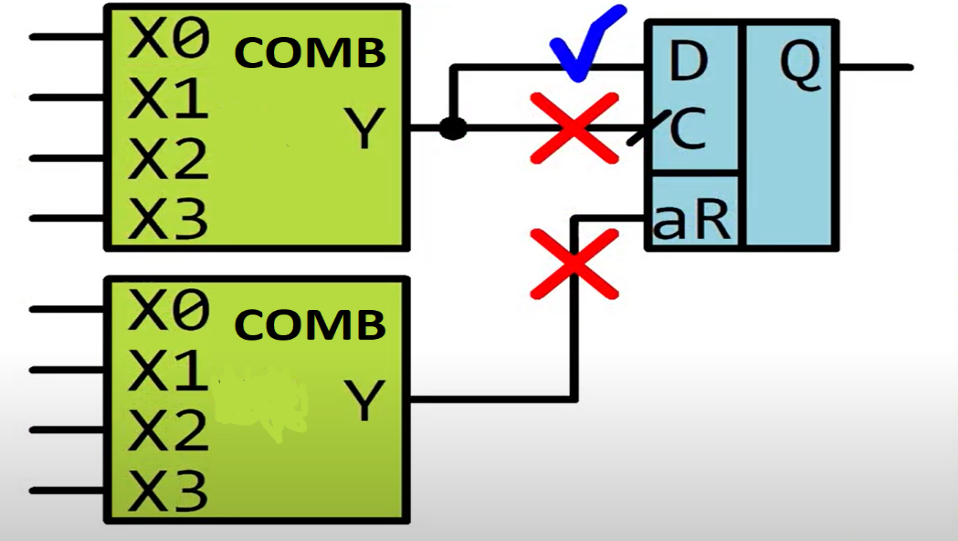
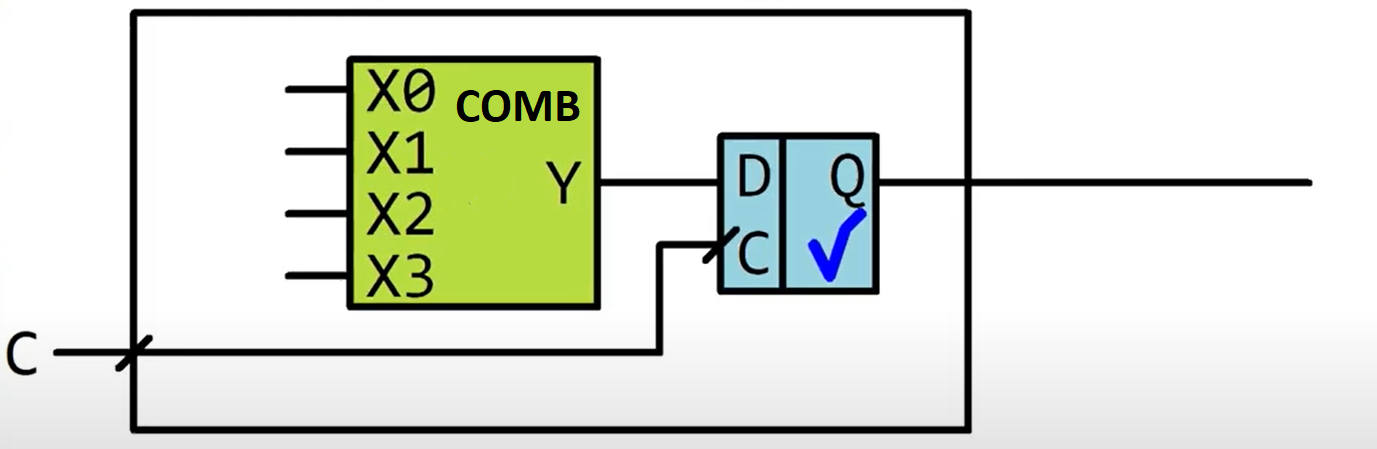
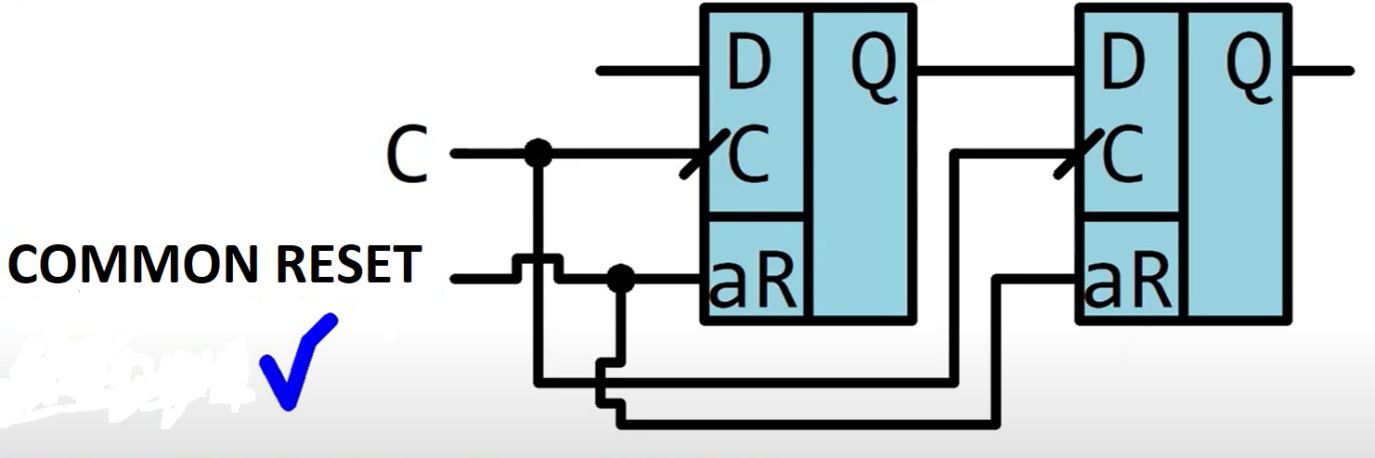
**8 principles of programming on FPGA**

1. **MAXIMUM COMMON CLOCKS.** All clocked elements such as registers, counters, FSM, individual triggers and RAM should be clocked with a common sync signal.
2. **CLK TO CLK.** Apply a sync signal only to the sync inputs of triggers and nowhere else.
3. **COMBINATION LOOPS.** Feedbacks in combinational circuits are prohibited.
4. **ASYNCHRONOUS SIGNALS.** Do not use asynchronous signals. All asynchronous signals entering the circuit must be synchronized using at least 2 flip-flops.
5. **CLOCKS THE SAME TIME**. The clock signal for all clocked elements must arrive at the same time.

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1. **COMB TO TRIG.** Connect the combinational circuit only to the D input of the trigger and nowhere else.
2. **REG OUTPUT.** The output of the combinational circuit arriving at the external device is passed through the trigger.
3. **ASYNCHRONOUS RESETS.** Use asynchronous flip-flop resets only for general circuit reset.