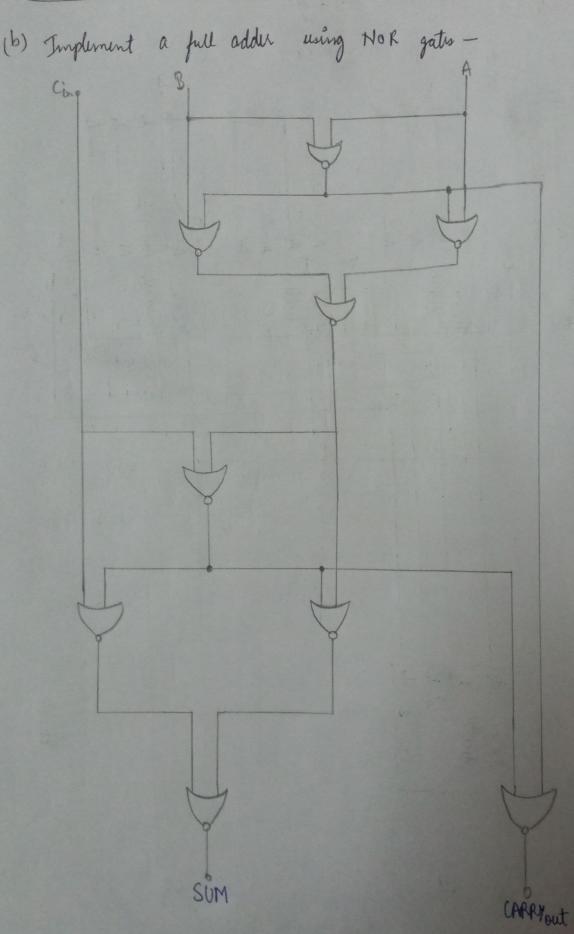
Name: SRADHA KEDIA Date and time: 30/03/2021, 9:30 AM to 12:30 AM Examination Roll no: 20234757053 Name of the brogsamme: MCA Semester: I Unique Paper Code: 223401104 Email ID: 200083@cs.du.oc, in Mobile no : 8840502121 Total no of pages: 05

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A full adder takes 3 input and gives 2 output sum 4 carry In this circuit diagram, A full adder using nor gates has been implemented.

There are three inputs Sin, A and B

4 bit combinational circuit using NAND gates:

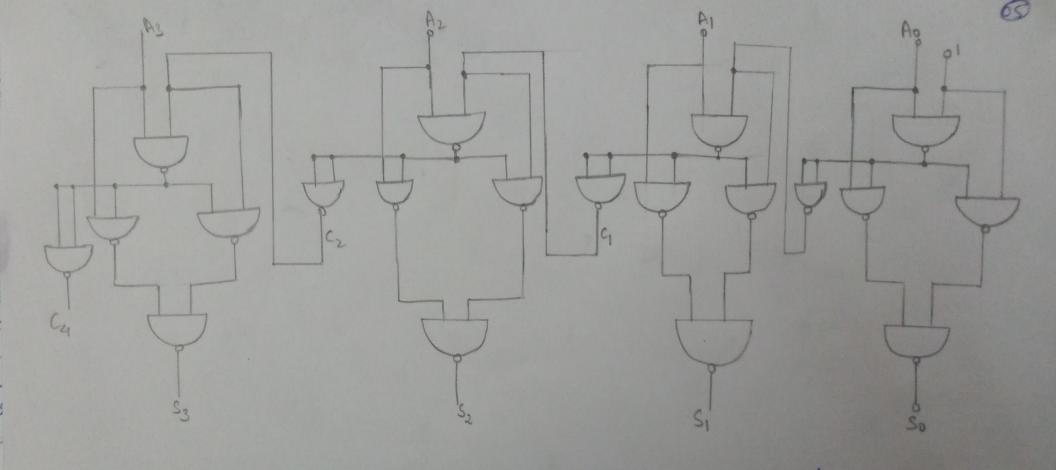
4 half adders (using NAND gotts) is used in this circuit diagram to implement a 4 bit combinational circuit.

In a half adder there are two inputs, x andy, which returns two outputs, hum and earry.

Let us consider, the binary value is stored in a register A. now, we have used 4 kay adders for 4 bit incrementer and we will pass one bit in each half adder in one input, say (n), and for first half adder (in which we are passing to, we will pass I in its second input y.

Now, the carry from previous half adder is passed to next half adder's y-input.

for, last half adder carry from it represent if the incrementation caused overflow or not.



4- bit Combinational circuit using NAND gates