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Subject

System Device & IC Lab

Class

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Semester

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1.	DC and Parametric analysis of NMOS and PMOS.	23.8.22	27.8.22	
2.	Simulation & analysis of resistive load CS amplifier.	30.8.22	30.8.22	<u>Gm (1)</u>
3.	Simulation & analysis of diode connected PMOS load.	6.9.22	6.9.22	<u>Gm (1) 2nd</u>
4.	Simulation & analysis of degenerate resistance.	13.9.22	13.9.22	
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6.	Simulation & analysis of Common Gate amp.	11.10.22	11.10.22	
7.	Simulation & analysis of Source follower amp.	18.10.22	18.10.22	

I N D E X

Experiment No. 1

Aim: Simulation and analysis of nMOS and pMOS.

Tools Required: Work Cadence

Formulae:

- For nMOS Region For pMOS

$$V_{GS} < V_T \leftarrow \text{Cut-off} \rightarrow V_{GS} > V_T$$

$$V_{GS} - V_T > V_{DS} \leftarrow \text{Linear} \rightarrow V_{DS} > V_{GS} - V_T$$

$$V_{GS} - V_T \leq V_{DS} \leftarrow \text{Saturation} \rightarrow V_{DS} < V_{GS} - V_T$$

- In Cut-off I_D (drain Current) = 0

- In Linear / Triode mode $I_D = \frac{k_n}{2} [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$

- In Saturation region $I_D = \frac{k_n}{2} (V_{GS} - V_T)^2$
[if $\lambda = 0$]

$$\text{where } k_n = \mu_n C_{ox} \frac{W}{L}$$

$$C_{ox} = \epsilon \frac{C_{ox}}{t_{ox}} F/cm^2$$

$$\frac{W}{L} = \text{Aspect Ratio}$$

- CIRCUIT:

NMOS

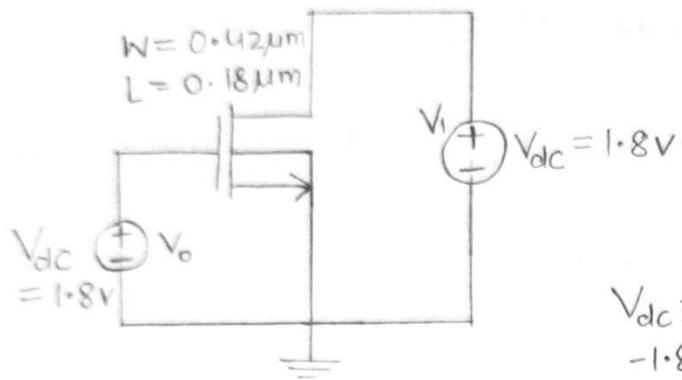


FIG: NMOS WITH DC BIASING

PMOS

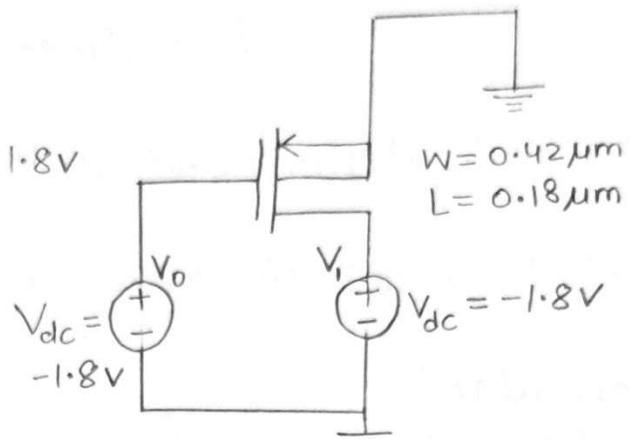


FIG: PMOS WITH DC BIASING

- SIMULATIONS:

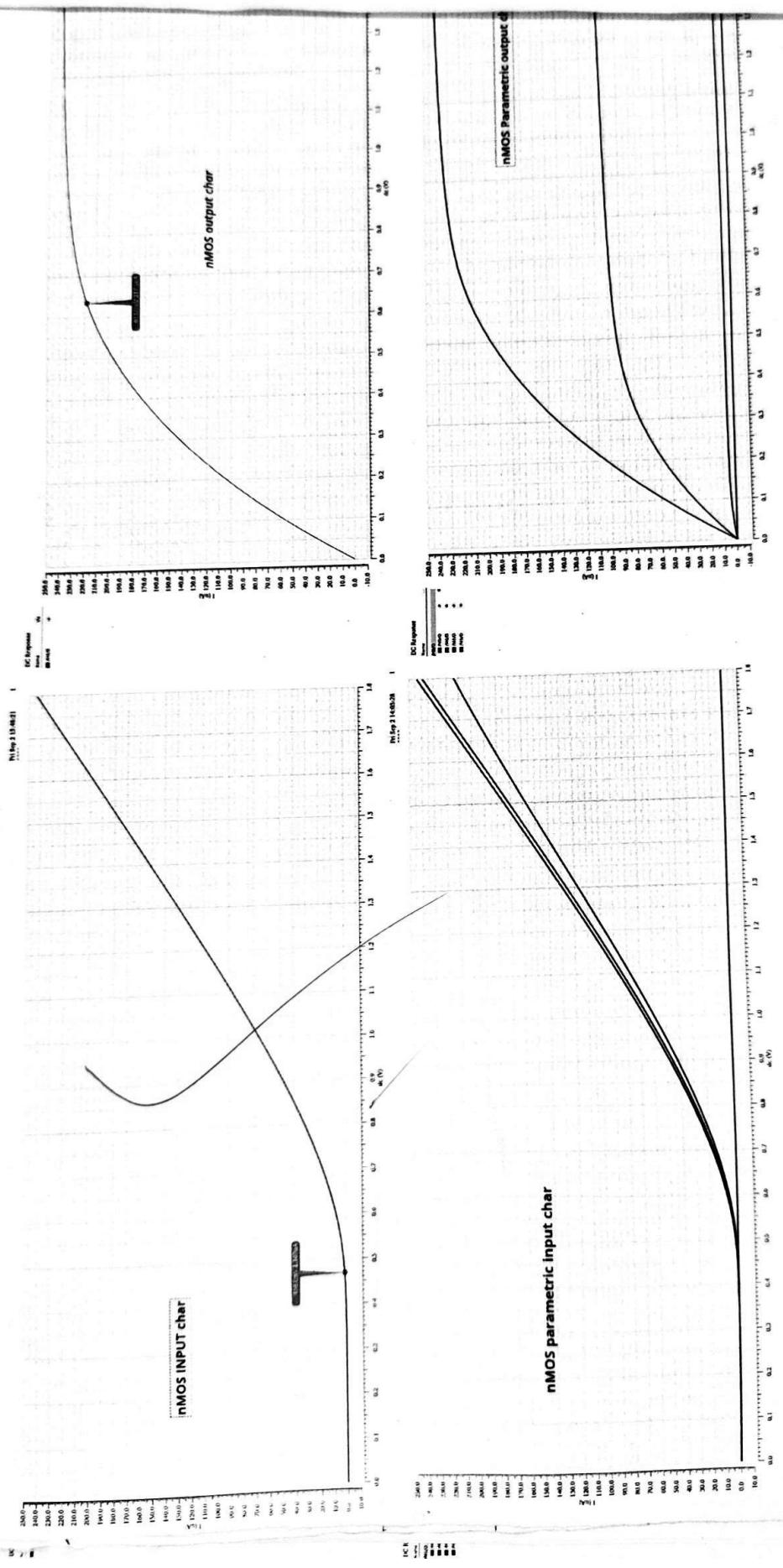
1. DC ANALYSIS: Both nMOS and pMOS Transistors are operating in Region 2 [Saturation].

→ I_d vs V_{gs} and I_d vs V_{ds} are plotted.

2. PARAMETRIC ANALYSIS:

→ I_d vs V_{gs} with different Values of V_{ds} is plotted.

→ I_d vs V_{ds} with different values of V_{gs} is plotted.

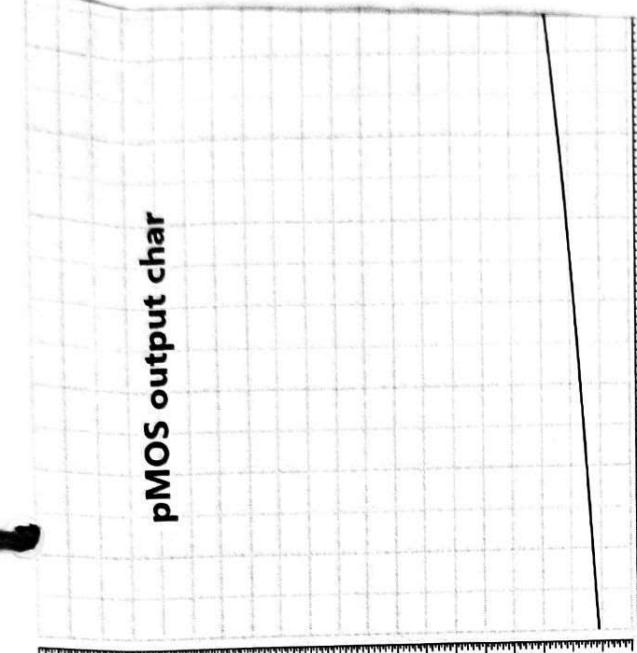




pMOS output char

pMOS parametric input char

pMOS parametric output char



pMOS output char

Results: we have successfully performed DC and parametric analysis for nMOS and pMOS for $L = 180 \text{ nm}$ technology.

Experiment No. 2

Aim: Simulation and analysis of resistive load common source amplifier.

Tools Required: Work Cadence.

Calculations:

Design Specifications - $|AV| = 10$, $V_T = 0.49$
 $L = 180 \text{ nm}$, $I_D = 50 \mu\text{A}$, $k'_n = 300 \mu\text{A}/\sqrt{\text{V}}$, $V_{DD} = 1.8 \text{ V}$
 $V_D = 0.9 \text{ V}$

- Drain Resistance / Load $R_D = \frac{V_{DD} - V_{DS}}{I_D}$

$$V_{DS} = V_D \quad \therefore R_D = \frac{1.8 - 0.9}{50 \times 10^{-6}} \Rightarrow \underline{\underline{R_D = 18 \text{ k}\Omega}}$$

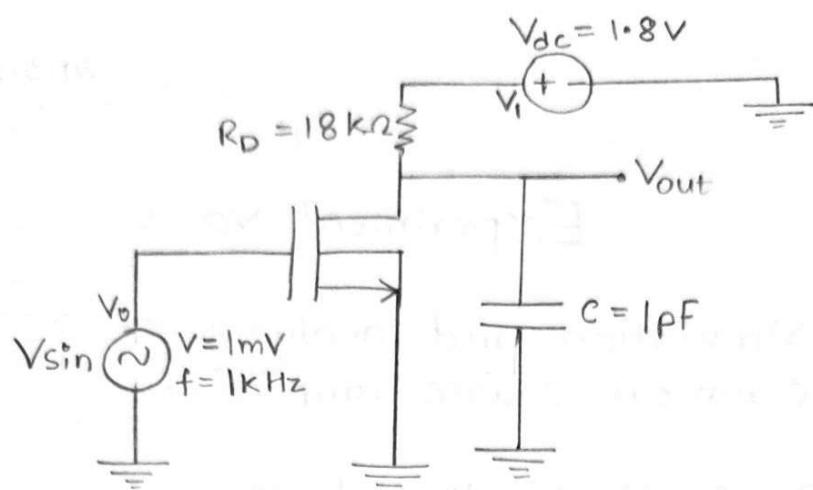
- Transconductance $g_m = \frac{|AV|}{R_D}$ [for CS amp]

$$\therefore \underline{\underline{g_m = \frac{10}{18} \text{ mV} = 0.55 \text{ mV}}}$$

- Aspect Ratio $\frac{W}{L} \rightarrow g_m = \sqrt{2 k'_n \frac{W}{L} \cdot I_D}$

$$\therefore \frac{W}{L} = \frac{g_m^2}{2 k'_n I_D} = \frac{(0.55 \times 10^{-3})^2}{2 \times 300 \times 10^{-6} \times 50 \times 10^{-6}} = \underline{\underline{10.28}}$$

CIRCUIT:

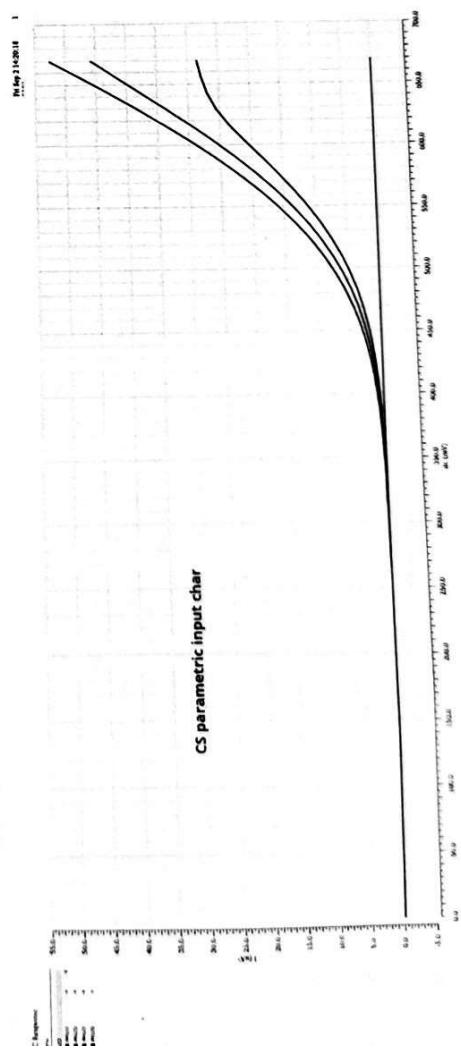
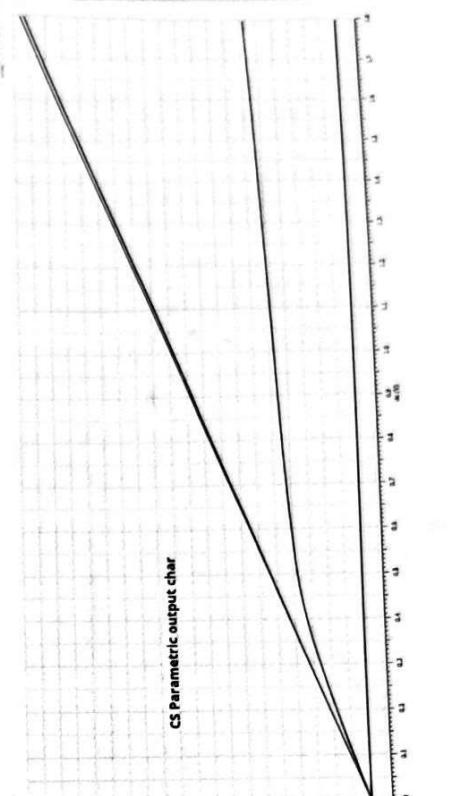
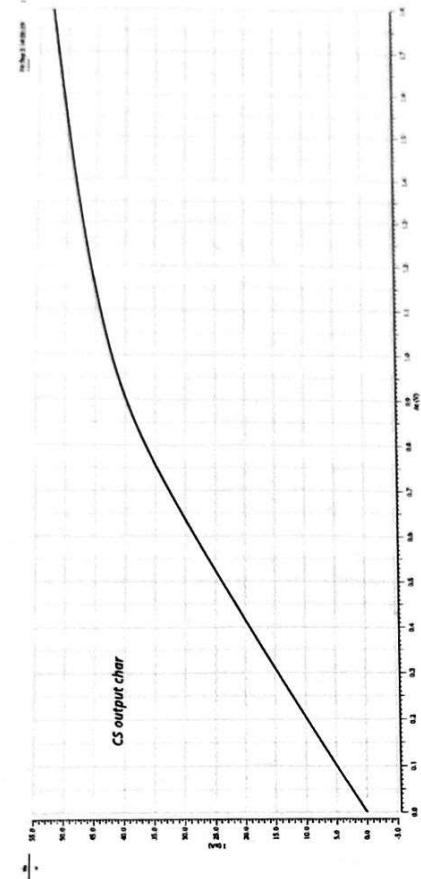


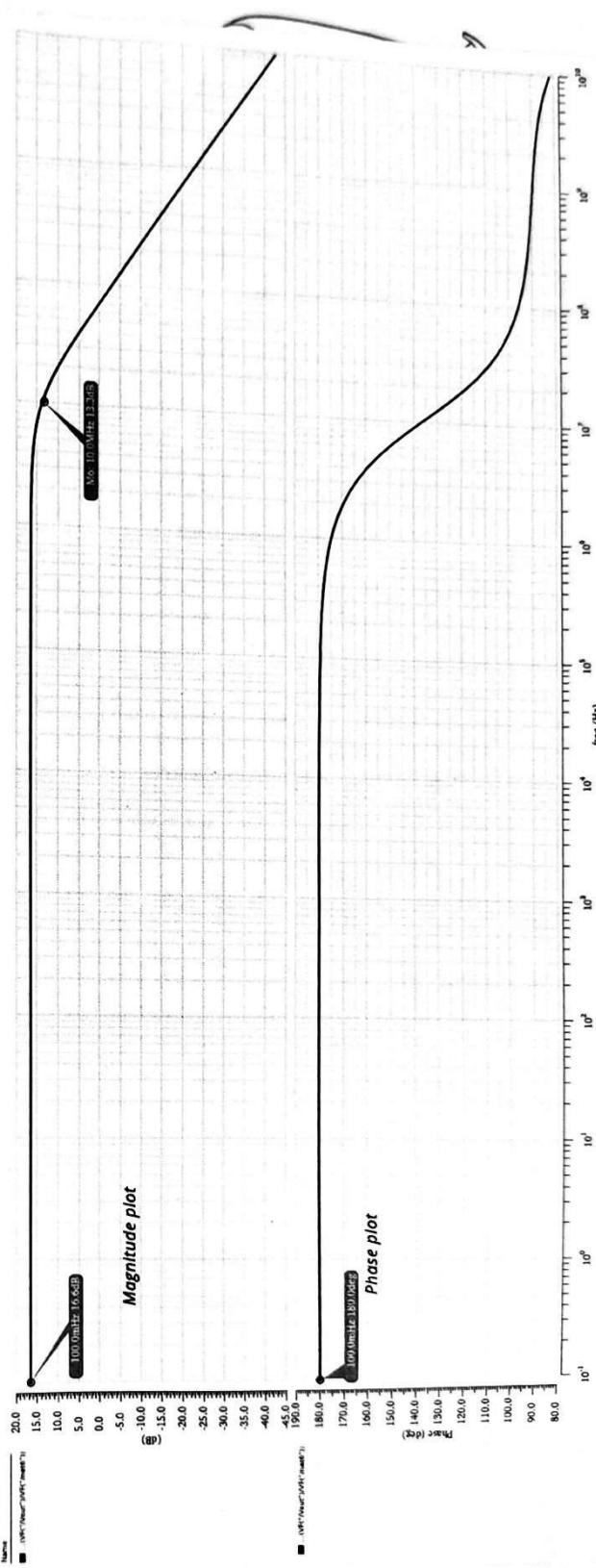
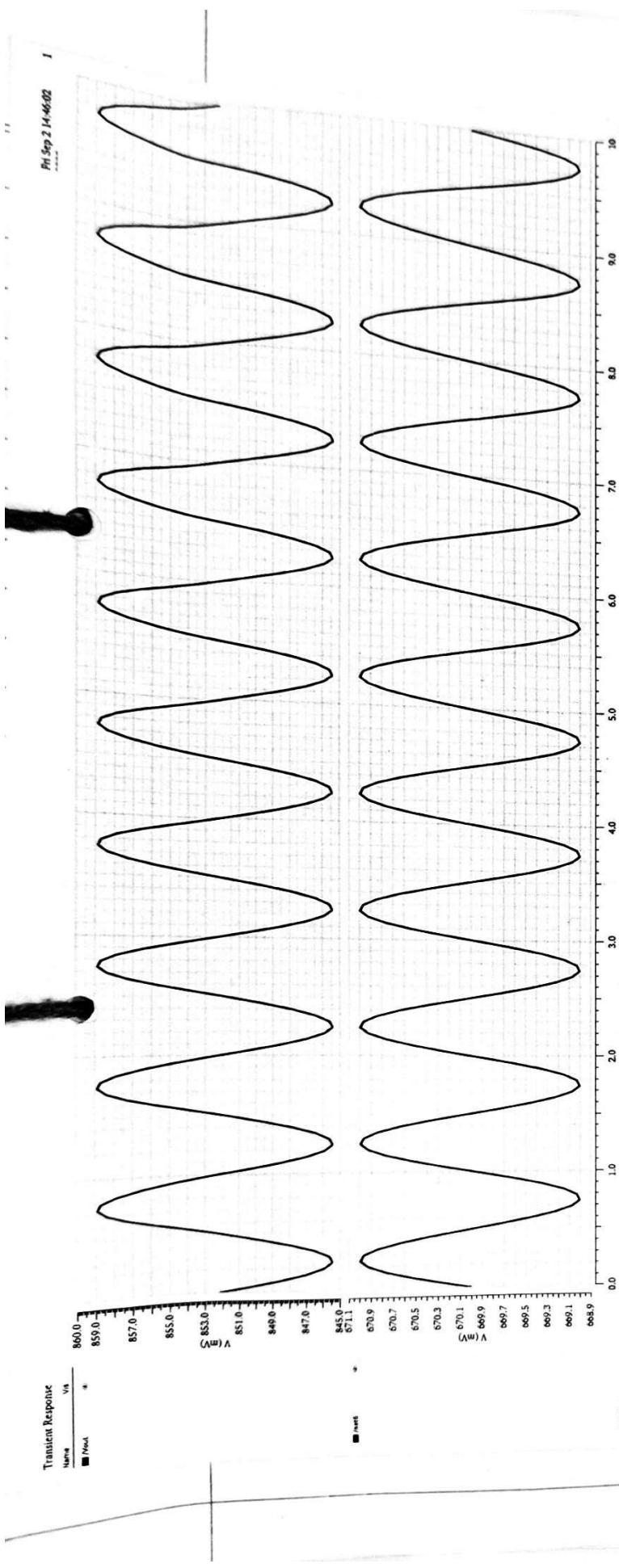
SIMULATIONS:

- PARAMETRIC ANALYSIS:

Sweep	0	0.6	1.2	1.8
Region	0	2	1	1
R_{out}	$293\text{ G}\Omega$	$151.55\text{ k}\Omega$	686.59Ω	392.51Ω
I_D	7.25 pA	$28.75\mu\text{A}$	$96.62\mu\text{A}$	$97.859\mu\text{A}$
g_m	230.12 pV	$332.79\mu\text{V}$	$125.59\mu\text{V}$	$45.77\mu\text{V}$
V_{TH}	0.48 V	0.487 V	0.496 V	0.496 V
V_{DS}	1.8 V	1.282 V	60.82 mV	37.09 mV
V_{GS}	0 V	0.6 V	1.2 V	1.8 V

- DC ANALYSIS: Transistor operating in Region 2.
- AC ANALYSIS: Gain vs freq. & Phase vs freq. are plotted.





$$\therefore L = 180 \text{ nm} \quad \therefore W = 10.28 \times 180 \text{ nm}$$

$$\text{or } L = 0.18 \mu\text{m} ; \quad W = \underline{1.85 \mu\text{m}}$$

- Input Voltage $V_{in} \rightarrow$

$$I_D = \frac{k_n'}{2} \left(\frac{W}{L} \right) (V_{in} - V_T)^2$$

$$\therefore 50 \times 10^{-6} = \frac{300 \times 10^{-6}}{2} \times 10.28 (V_{in} - 0.49)^2$$

$$\Rightarrow V_{in} = \underline{0.67 \text{ V}}$$

Results: We have successfully performed dc, ac, transient and parametric analysis for resistive load common source amplifier.

Experiment No. 3

Aim: Simulation and analysis of diode connected PMOS load common source amplifier.

Tools Required: Work Cadence (Virtuoso)

Calculations:

Design specifications — $|A_v| = 2$, $V_d = 0.9$, $k'_n = 300 \mu A/V^2$
 $V_{DD} = 1.8 V$, $I_D = 50 \mu A$, $k'_p = 60 \mu A/V^2$, $V_{thp} = |V_{thn}| = 0.45 V$,
 $V_g = 0.8 V$.

- $\frac{(W/L)_n}{(W/L)_p} = ?$, • $V_{gs} = ?$

- $|A_v| = g_m_1 \left(\frac{1}{g_m_2} // r_o_2 \right) \quad [\because r_o_2 = \infty] \Rightarrow |A_v| = \frac{g_m_1}{g_m_2}$

$$\therefore g_m_1 = \sqrt{2 k'_n (W/L)_n I_D} \quad \therefore |A_v| = \sqrt{\frac{k'_n (W/L)_n}{k'_p (W/L)_p}} = 2$$

$$g_m_2 = \sqrt{2 k'_p (W/L)_p I_D}$$

$$\Rightarrow \frac{300 \times 10^{-6} (W/L)_n}{60 \times 10^{-6} (W/L)_p} = 4 \Rightarrow \frac{(W/L)_n}{(W/L)_p} = 0.8 = \underline{\underline{\frac{4}{5}}}$$

$$\therefore L_n = L_p = 0.18 \mu m \Rightarrow W_n = 0.72 \mu m ; W_p = 0.9 \mu m$$

- $\therefore I_{D1} = I_{D2} \Rightarrow \frac{k'_n}{2} \left(\frac{W}{L} \right)_n (V_{in} - 0.45)^2 = \frac{k'_p}{2} \left(\frac{W}{L} \right)_p (1.8 - 0.9)^2$

$$300 \times 10^{-6} \times 4 (V_{in} - 0.45)^2 = 60 \times 10^{-6} \times 5 (0.9 - 0.45)^2$$

$$\Rightarrow \underline{\underline{V_{in} = 0.675 V}}$$

CIRCUIT:

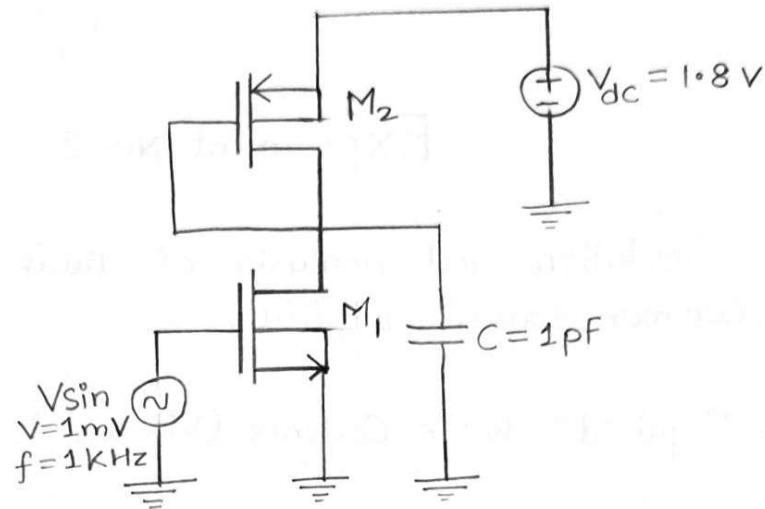


FIG : DIODE CONNECTED PMOS LOAD
CS AMPLIFIER

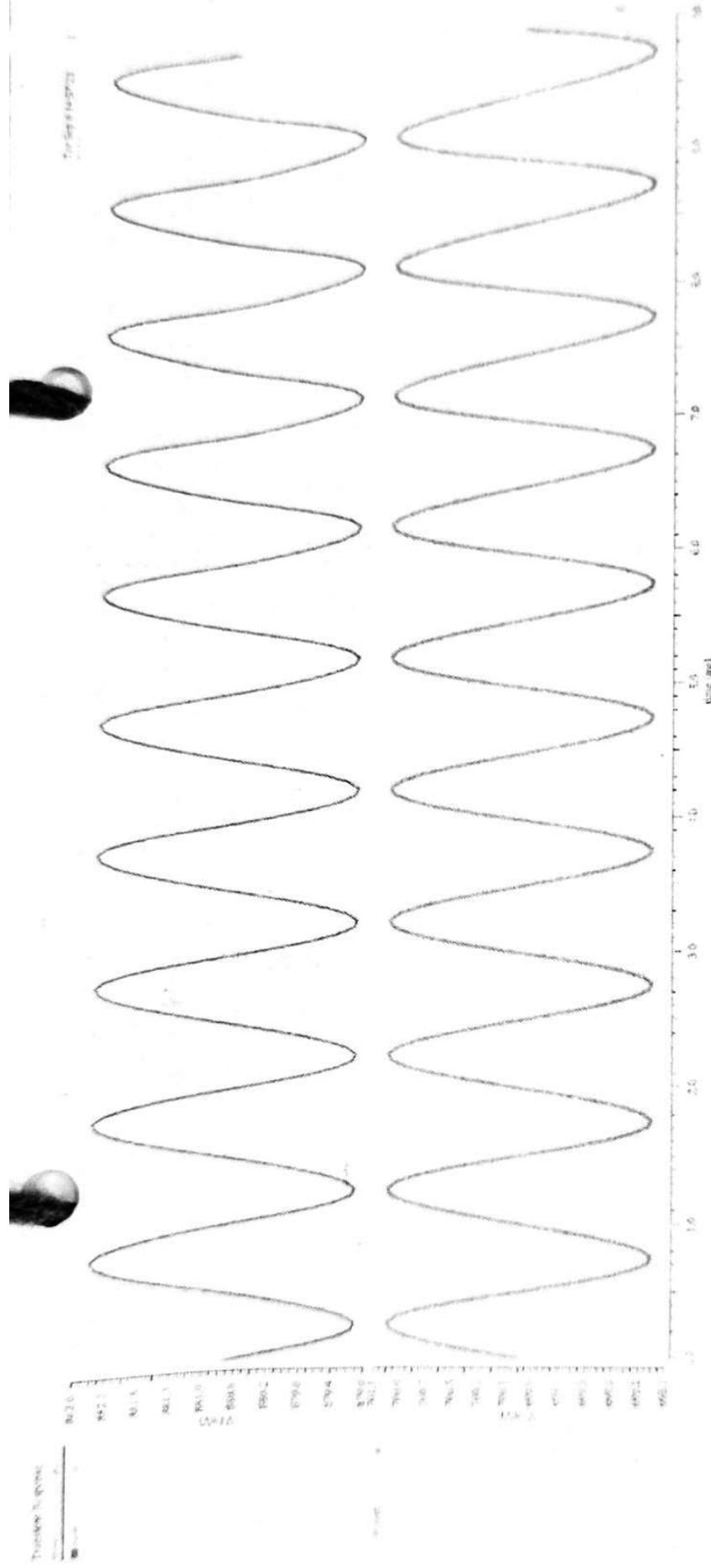
SIMULATIONS:

• PARAMETRIC ANALYSIS:

Sweep	0	0.6	1.2	1.8
Region	0	2	1	1
Rout	293.006G	151.551K	686.595	392.511
ID	7.2543p	28.7547μ	96.6207μ	97.8599μ
gm	230.126p	332.79μ	125.598μ	45.772μ
Vth	483.34m	487.121m	496.094m	496.128m
Vds	1.8	1.28241	60.8201m	37.0909m
Vgs	0	0.6	1.2	1.8

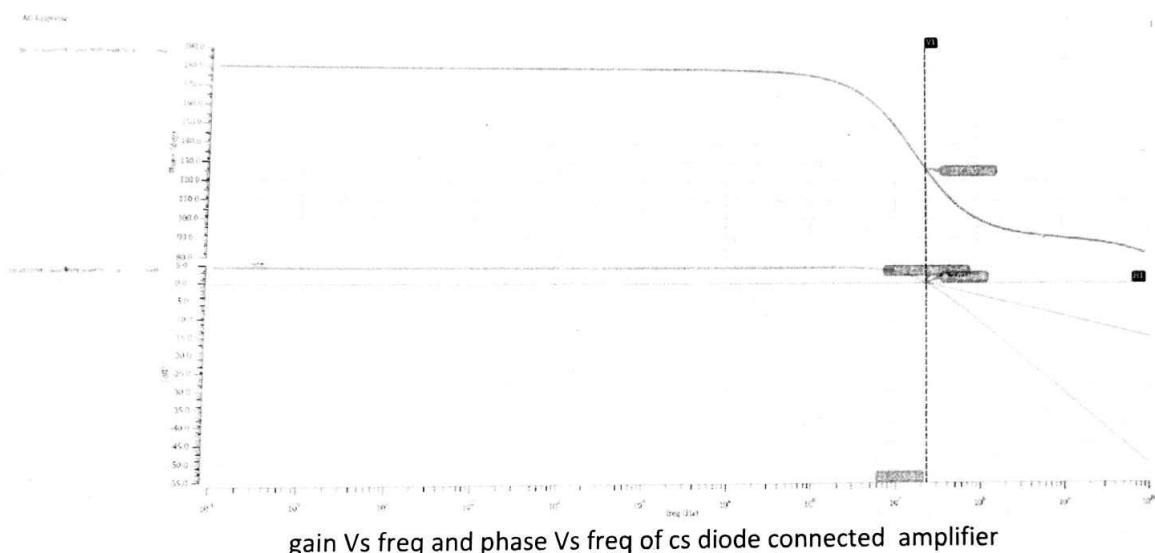
- DC ANALYSIS: Transistor operating in Region 2.

- AC ANALYSIS: Gain vs Freq. and Phase vs Freq. are plotted.



Transient response of cs diode connected

Result: we have successfully performed DC, AC, transient and parametric analysis for diode connected common source amplifier.



Experiment No. 4

Aim: Simulation and analysis of common source having degenerate resistance.

Tools Required: Work Cadence (Virtuoso)

Calculations:

Design specifications — $V_{DD} = 1.8V$, $V_S = 0.3V$, $V_D = 0.9V$
 $|A_V| = 2$, $BW = 2 \text{ MHz}$, $k'_n = 200 \mu\text{A}/\text{V}^2$, $I_D = 50 \mu\text{A}$, $V_{th} = 0.3V$

Find R_D , R_S , g_m , V_{in} and $\frac{W}{L}$?

- $\because V_{DD} = V_D + I_D R_D \Rightarrow R_D = \frac{1.8 - 0.9}{50 \mu} \Rightarrow \underline{\underline{R_D = 18 \text{ k}\Omega}}$

- $V_S = I_D R_S \Rightarrow \underline{\underline{R_S = \frac{0.3}{18 \times 50 \mu} = 6 \text{ k}\Omega}}$

- $|A_V| = \frac{g_m R_D}{1 + g_m R_S} \Rightarrow 2 = \frac{g_m (18 \text{ k})}{1 + g_m (6 \text{ k})}$

$$\Rightarrow g_m (6 \text{ k}) = 2 \Rightarrow \underline{\underline{g_m = 0.333 \text{ m}\text{V}}}$$

- $g_m = \sqrt{2 k'_n \frac{W}{L} I_D} \Rightarrow (0.33 \times 10^{-3})^2 = 2 \times 200 \mu \times 50 \mu \times \frac{W}{L}$

$$\Rightarrow \frac{W}{L} = 5.445, \quad \because L = 0.18 \mu\text{m}$$

$$\therefore W = 0.98 \mu\text{m}$$

CIRCUIT:

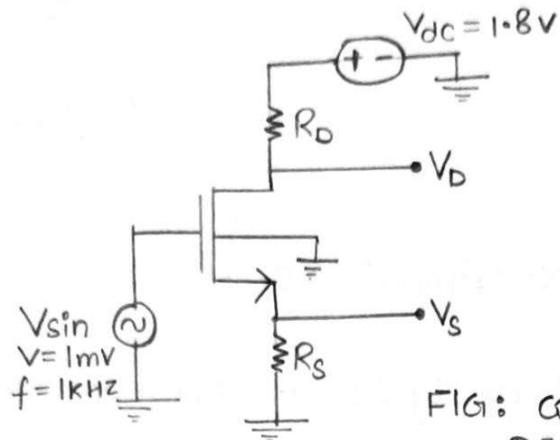


FIG: COMMON SOURCE AMPLIFIER WITH DEGENERATE RESISTANCE

SIMULATIONS:

• PARAMETRIC ANALYSIS:

Sweep	0	0.3	0.6	0.9	1.2	1.5	1.8
Region	0	3	2	2	2	1	1
R _{out}	882.614G	78.567M	529.665K	158.27K	42.556K	2.329K	1.206K
I _D	2.549p	32.35n	7.2506μ	30.52μ	57.157μ	69.724μ	71.74μ
g _m	84.907p	898.255n	108.858μ	258.477μ	317.438μ	148.57μ	77.383μ
V _{th}	490.234m	490.297m	500.27m	530.599m	562.919m	577.476m	579.798m
V _{ds}	1.8	1.79925	1.62502	1.06737	428.223m	126.604m	78.174m
V _{gs}	-26.7054m	299.812m	556.216m	716.843m	857.056m	1.03165	1.36954

• DC ANALYSIS: Transistor operating in Region 2.

• AC ANALYSIS: Gain vs freq. and Phase vs Freq. graphs

$$V_{in} = V_{gs} + V_s = V_{gs} + 0.3$$

$$\text{and } I_D = \frac{k_n}{2} \frac{W}{L} (V_{gs} - V_{th})^2 \Rightarrow V_{gs}$$

$$50\mu = \frac{200\mu}{2} \times 5.445 (V_{gs} - 0.3)^2$$

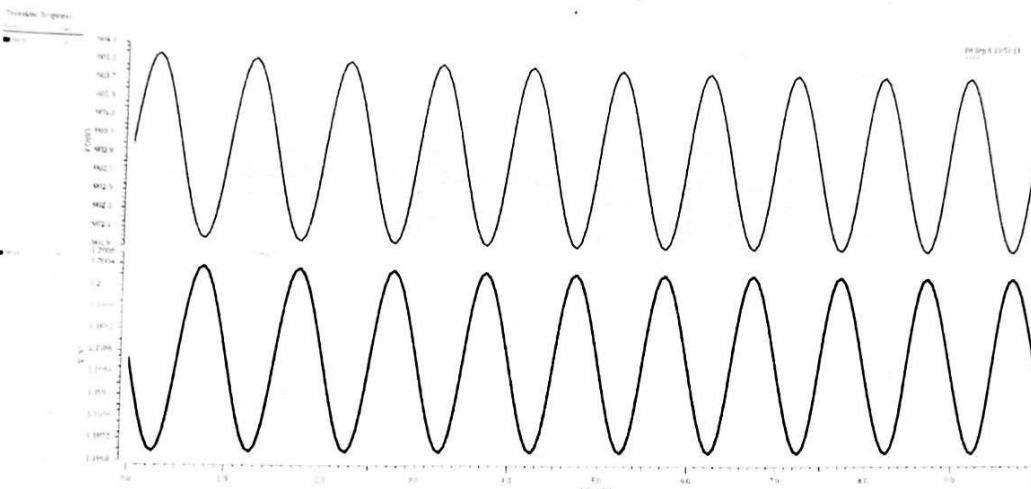
$$\Rightarrow V_{gs} = 0.603V \therefore \underline{V_{in} = 0.903V}$$

Result: DC, AC, transient and parametric analysis for common source amplifier with degenerate load resistance has been performed successfully.

$$V_{in} = V_{gs} + V_s = V_{gs} + 0.3$$

$$\text{and } I_D = \frac{k'n}{2} \frac{W}{L} (V_{gs} - V_{th})^2 \Rightarrow V_{gs}$$

$$50\mu = 200\mu \cdot 5.445 (V_{gs} - 0.3)^2$$

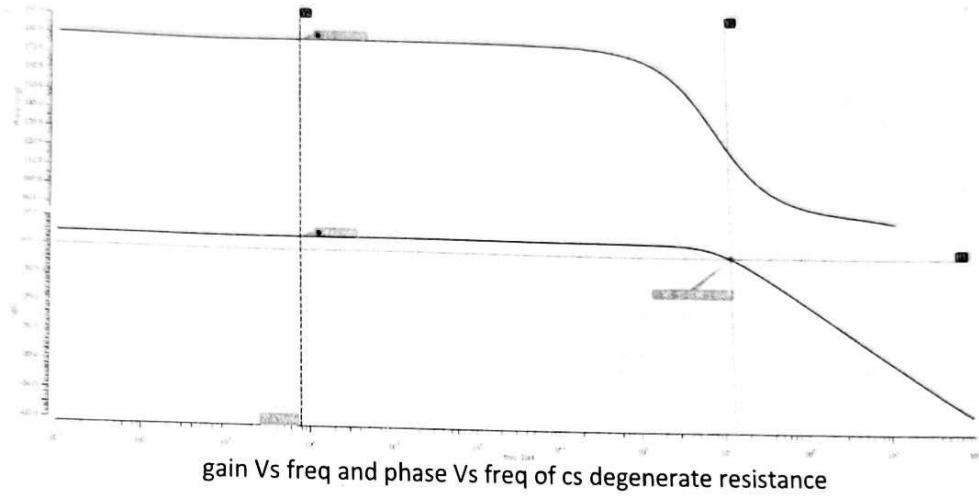


Transient response of cs degenerate resistance

$$V_{in} = V_{gs} + V_s = V_{gs} + 0.3$$

$$\text{and } I_D = \frac{k_n}{2} \frac{W}{L} (V_{gs} - V_{th})^2 \Rightarrow V_{gs}$$

$$f_{011} = 200\mu \cdot 5.445 (V_{ds} - 0.3)^2$$



Experiment No. 5

Aim: Simulation and analysis of common source amplifier with current source load.

Tools Required: Work Cadence (Virtuoso)

Calculations:

Design Specifications — $V_{DD} = 1.8V$, $|A_V| = 20$, $r_{O_1} = 80k\Omega$,
 $r_{O_2} = 120k\Omega$, $V_b = 1V$, $|V_{thn}| = |V_{thp}| = 0.45V$, $I_D = 100\mu A$,
 $k_n' = 300 \mu A/V^2$, $k_p' = 100 \mu A/V^2$

$$\left(\frac{W}{L}\right)_n, \left(\frac{W}{L}\right)_p, g_m, V_{in} = ?$$

- $I_D = \frac{k_p'}{2} (1.8 - 1 - 0.45)^2 \times \left(\frac{W}{L}\right)_p = \frac{100\mu}{2} \times \left(\frac{W}{L}\right)_p (0.1225)$

$$\left(\frac{W}{L}\right)_p = \frac{2}{0.1225} \Rightarrow \underline{\underline{\left(\frac{W}{L}\right)_p}} = \underline{\underline{16.3265}}, \quad \therefore L_p = 0.18\mu m, \quad W_p = 2.93\mu m$$

- $|A_V| = g_m, (r_{O_1} \parallel r_{O_2}) \Rightarrow 20 = g_m, (80k \parallel 120k)$

$$\therefore \underline{\underline{g_m}} = \underline{\underline{0.4167 mV}}$$

- $g_m, = \sqrt{2 k_n' \left(\frac{W}{L}\right)_n I_D} \Rightarrow (0.4167m)^2 = 2 \times 300\mu \times 100\mu \times \left(\frac{W}{L}\right)_n$
 $\Rightarrow \underline{\underline{\left(\frac{W}{L}\right)_n}} = \underline{\underline{2.893}} \quad \therefore L_n = 0.18\mu m, \quad W_n = 0.52\mu m$

CIRCUIT:

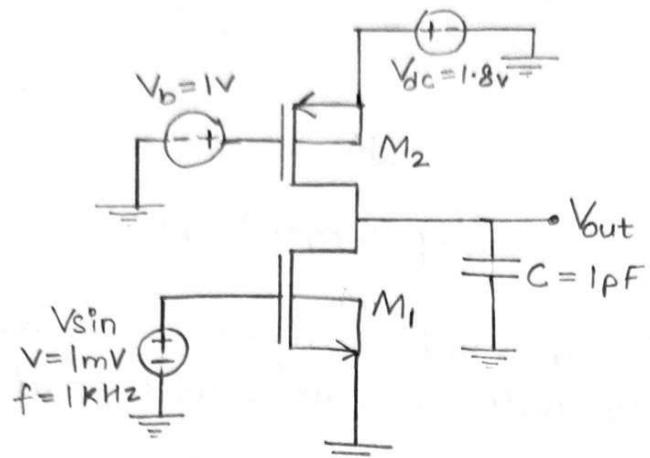


FIG: COMMON SOURCE AMPLIFIER WITH CURRENT SOURCE LOAD.

SIMULATIONS:

• PARAMETRIC ANALYSIS:

Sweep	0	0.3	0.6	0.9	1.2	1.5	1.8
Region	0	3	2	2	1	1	1
R _{out}	1.6527G	128.76M	684.877K	281.172K	3.9029K	2.1363K	1.6837K
I _D	1.56772P	21.3196n	8.3960μ	53.9168μ	68.5429μ	69.417μ	69.783μ
g _m	57.293P	606.316n	92.313μ	205.435μ	186.538μ	61.439μ	38.272μ
V _{ds}	1.8	1.79993	1.77258	1.24892	195.162m	128.159m	101.67m
V _{th}	476.392m	476.397m	476.529m	479.04m	484.095m	484.17m	484.54m
V _{gs}	-2.449n	300m	600m	900m	1.2	1.5	1.8

DC ANALYSIS: Transistor operating in Region 2.

AC ANALYSIS: Gain vs freq. and phase vs freq. graphs are plotted.

- $\therefore V_{in} = V_{gsn}$

$$\therefore I_D = \frac{k_n'}{2} \times \left(\frac{W}{L}\right)_n (V_{gsn} - V_{thn})^2$$

$$\Rightarrow 100\mu = \frac{300\mu}{2} \times 2.893 (V_{gsn} - 0.45)^2$$

$$\Rightarrow V_{gsn} = 0.93v = \underline{\underline{V_{in}}}$$

Results: we have successfully performed DC, AC, transient and parametric analysis of common source amplifier with current source load.

CIRCUIT:

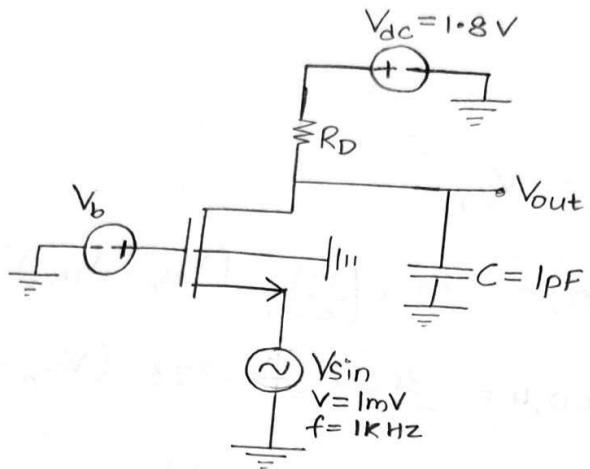


FIG: COMMON GATE AMPLIFIER

Experiment No. 6

Aim: Simulation and analysis of common gate amplifier.

Tools Required: Work Cadence (Virtuoso)

Calculations:

Device design specifications — $L = 180\text{nm}$, $|A_V| = 5$.

$V_{DD} = 1.8\text{V}$, $V_{in} = 0.6\text{V}$, $C = 1\text{pF}$, $BW = 1\text{MHz}$, $k'_n = 300\text{mA/V}^2$.

$V_d = 0.5\text{V} = V_{out}$, $I_D = 50\mu\text{A}$, $V_{th} = 0.5\text{V}$

$$R_D = ? , g_m , \frac{W}{L} , V_b = ?$$

- $\therefore V_{DD} = V_d + I_D R_D \Rightarrow R_D = \frac{1.8 - 0.5}{50\mu\text{A}} , R_D = 26\text{k}\Omega$

- $|A_V| = g_m R_D \Rightarrow 5 = g_m (26\text{k}) \Rightarrow g_m = 0.192\text{mV}$

- $g_m = \sqrt{2 k'_n \frac{W}{L} I_D} \Rightarrow (0.192\text{m})^2 = 2 \times 300\mu\text{A} \times 50\mu\text{A} \times \frac{W}{L}$

$$\Rightarrow \underline{\underline{\frac{W}{L}}} = 1.23 \quad \because L = 0.18\mu\text{m}$$

$$\therefore W = 0.22\mu\text{m}$$

- $\therefore V_{gs} = V_b - V_{in} \quad \therefore I_D = \frac{k'_n}{2} \left(\frac{W}{L} \right) (V_{gs} - V_{th})^2$

$$\Rightarrow 50\mu\text{A} = \frac{300\mu\text{A}}{2} \times 1.23 (V_b - 0.6 - 0.5)^2 \Rightarrow \underline{\underline{V_b = 1.62\text{V}}}$$

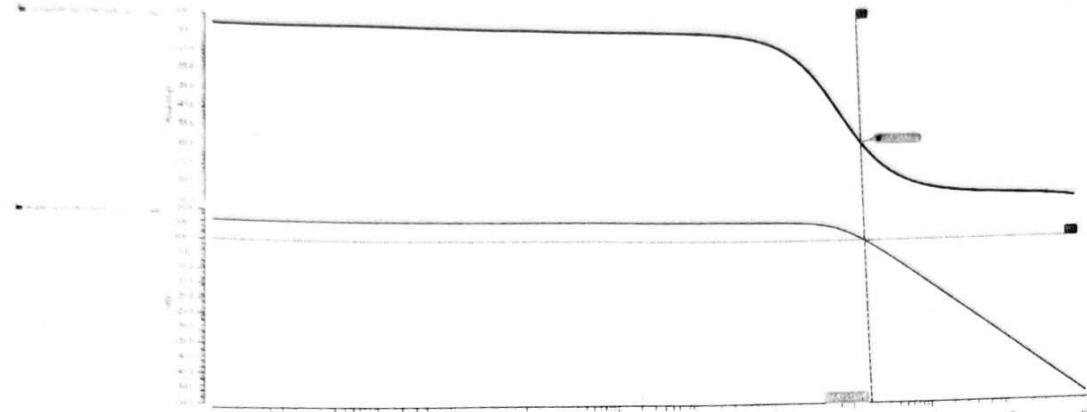
SIMULATIONS:

• PARAMETRIC ANALYSIS:

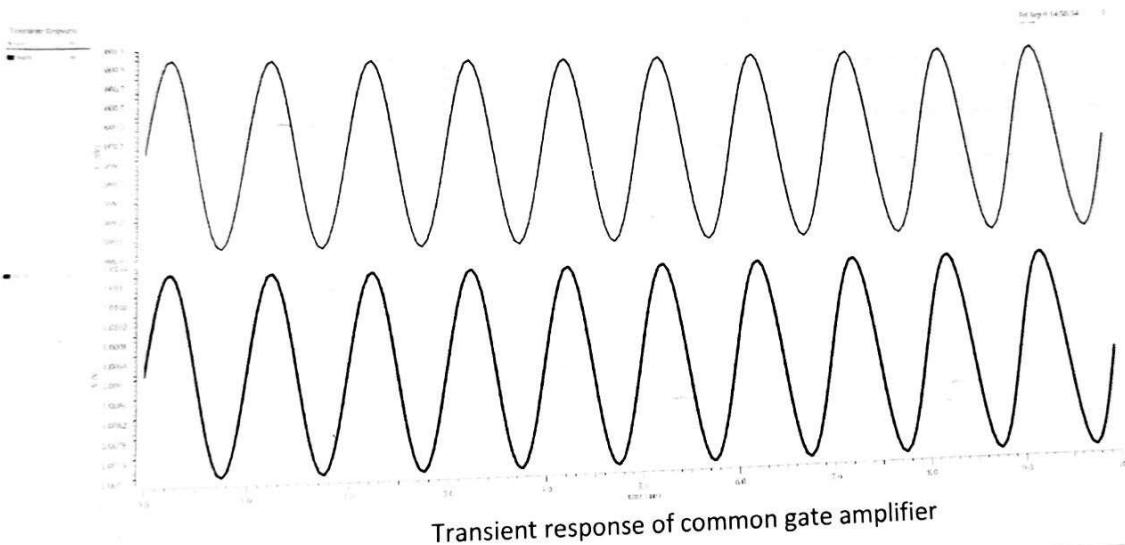
Sweep	0	0.3	0.6	0.9	1.2	1.5	1.8
Region	0	1	1	2	3	0	0
R _{out}	2.3202K	3.5250K	11.7073K	392.14K	235.158n	15.325T	48.669A
I _D	64.2355μ	57.9788μ	37.3887μ	6.4249μ	4.8558n	57.191f	166.287A
G _m	46.4649μ	54.5787μ	109.729μ	74.773μ	157.797n	1.977P	33.503Y
V _{th}	476.54m	532.308m	576.149m	607.335m	636.269m	667.178m	693.327m
V _{ds}	129.877m	148.76m	227.893m	732.95m	599.874m	300m	-46.804n
V _{gs}	1.62	1.32	1.02	720m	420m	120m	-100m

- DC ANALYSIS: Transistor operating in Region 2
- AC ANALYSIS: Gain vs Freq. and phase vs freq. graphs are plotted.

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gain Vs freq and phase Vs freq of common gate amplifier



Transient response of common gate amplifier

CIRCUIT:

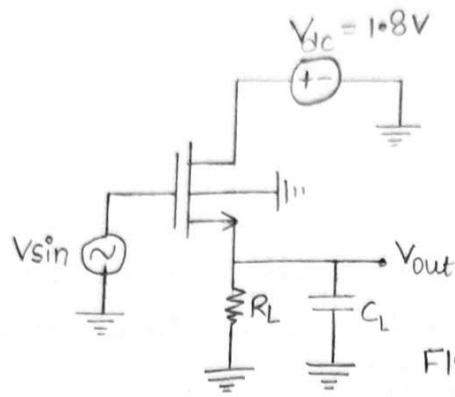


FIG: SOURCE FOLLOWER AMPLIFIER

SIMULATIONS:

• PARAMETRIC ANALYSIS:

Sweep	0	0.3	0.6	0.9	1.2	1.5	1.8
Region	0	3	3	2	2	2	2
R _{out}	64.35 G	7.78 M	206.49 k	78.37 k	45.03 k	29.99 k	21.26 k
I _D	30.25 p	266.3 n	12.05 μ	32.93 μ	36.0 μ	89.09 μ	104.75 μ
g _m	951.71 p	7.422 μ	236.2 μ	529.15 μ	770.82 μ	963.8 μ	1.113 m
V _{th}	0.473	0.4733	0.479	0.534	0.569	0.599	0.627
V _{DS}	1.8	1.797	1.679	1.470	1.239	0.999	0.752
V _{gs}	-320.58 n	0.297	0.479	0.570	0.639	0.699	0.752

• DC ANALYSIS: Transistor operating in Region 2.

• TRANSIENT ANALYSIS: $V_{in\ pp} = 2 \text{ mV}$ $V_{out\ pp} = 1.55 \text{ mV}$
 $A_v = 0.775$

• AC ANALYSIS: Gain vs freq. and phase vs freq. graphs are plotted.

$$\text{Gain} = -2.17099 \text{ dB} \Rightarrow \text{Gain} = 0.778$$

Transient response of source follower

