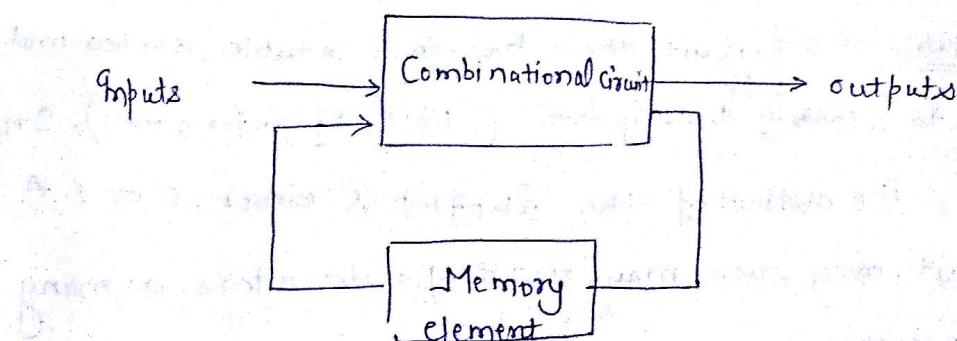


A Sequential circuit is a logic circuit whose output depends not only present value of its input signals but also on the sequence of past inputs. It is a combination of combinational circuit and a storage element. The storage elements are devices capable of storing binary information. The binary information stored in these elements at any given time defines the state of the sequential circuit at that time.

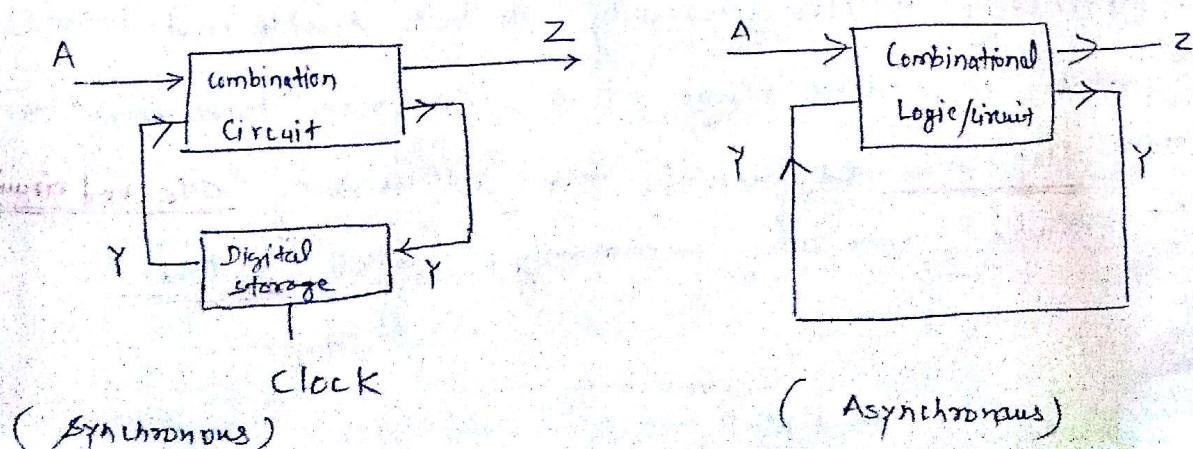
The sequential circuit receives binary information from external inputs that, together with present state of the storage elements, determine the condition binary value of the outputs.



Type:

Synchronous sequential circuit -:

Asynchronous sequential circuit -:



Storage elements: Latch; Flipflop.

Latch

- 1. It is level sensitive device.
- 2. It is based on enable function input.
- 3. It is sensitive to duration of the pulse.
- 4. Useful for design of asynchronous sequential circuit.

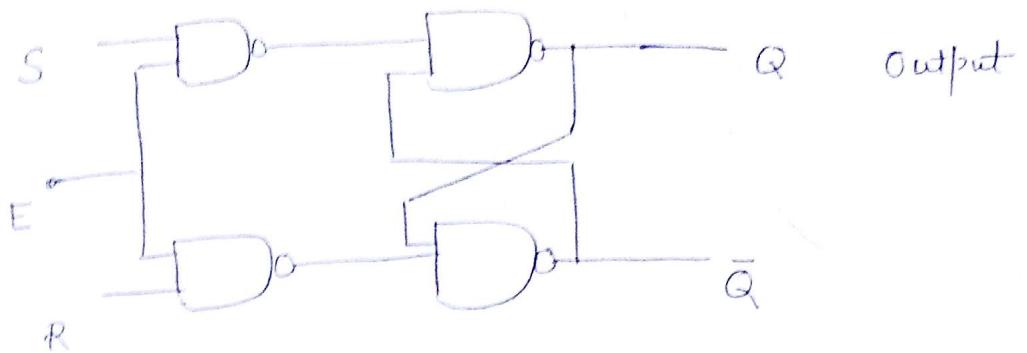
Flipflop

- It is edge sensitive device.
- It works on the basis of clock pulses.
- It is sensitive to signal change.
- useful for the design of synchronous sequential circuit.

Flip-flop or Latch is a circuit that has two stable states and can be used to store ^{1-bit} binary data (1 bit of information). In a stable state, the output of the flipflop is either 0 or 1. A sequential circuit may use many flipflops to store as many bits as necessary.

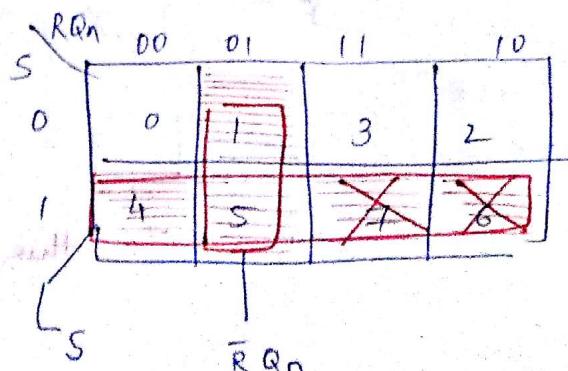
- * A flipflop is a bistable multivibrator.
- * Flip-flop can be either simple (transparent or opaque) or clocked (synchronous or edge-triggered). Although the term flipflop has historically referred generically to both simple and clocked circuits, in modern usage it is common to reserve the term flip-flop exclusively for discussing clocked circuits. The simple ones are commonly called latches.

SR Latch



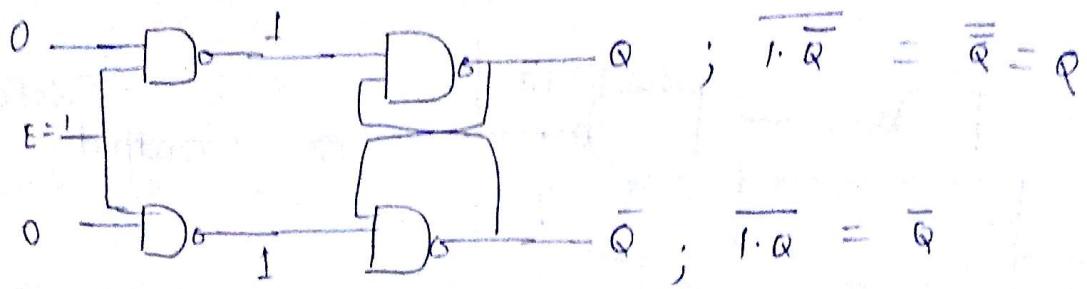
E	S	R	Q (next state)	\bar{Q} (next state)	Comment
0	X	X	NC	NC	No change
1	0	0	NC	NC	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	-	-	Indeterminate/Avoid this

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

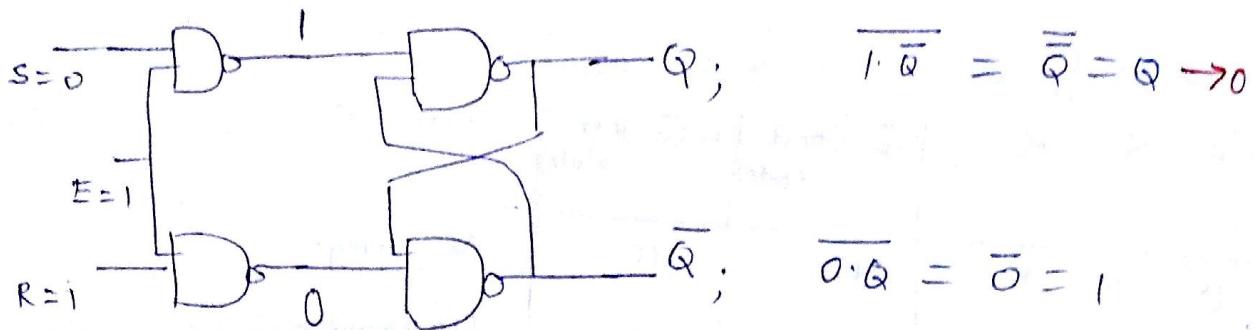


$$Q_{n+1} = S + \bar{R}Q_n$$

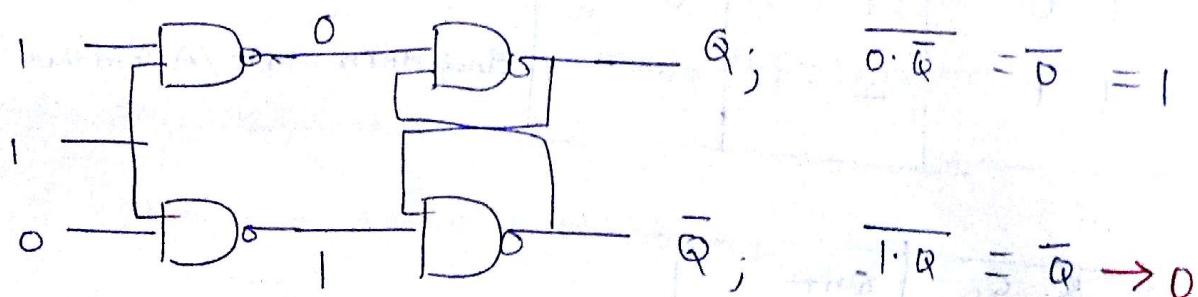
$$S=0 \quad R=0$$



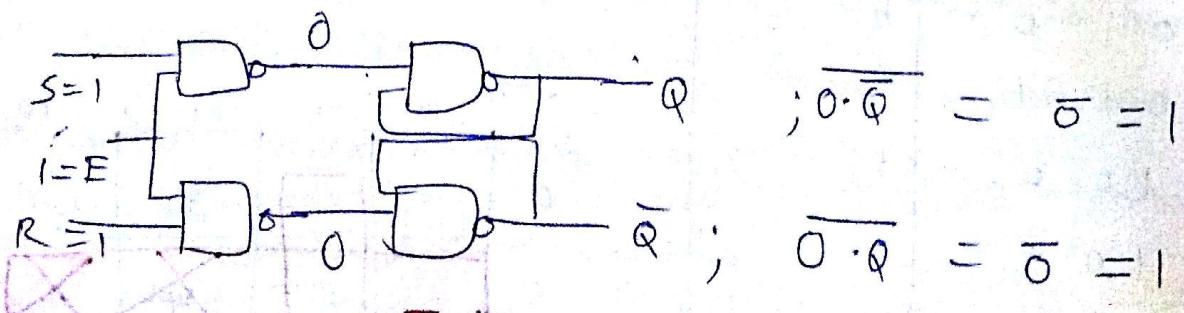
$$S=0 \quad R=1$$



$$S=1 \quad R=0$$

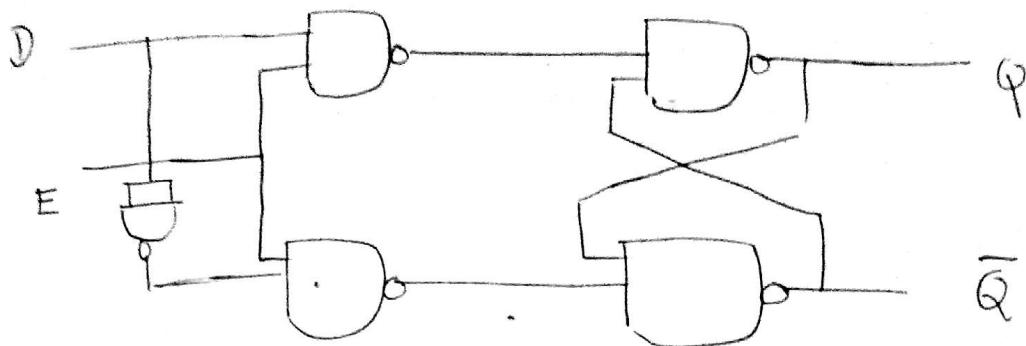


$$S=1 \quad R=1$$



To this is indeterminate state.

D Latch: One way to eliminate the undesirable condition of the indeterminate state in SR latch is to ensure that inputs S and R are never equal to 1 at the same time. This is done in D-latch.



E	D	Q (next state)	\bar{Q}	Comment
0	X	No change	N.C	No change
1	0	0	1	Reset
1	1	1	0	Set

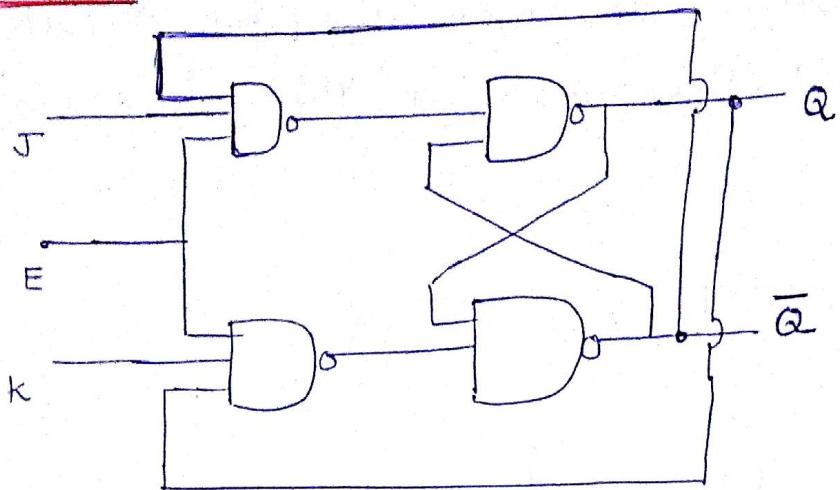
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$$Q_{n+1} = D\bar{Q}_n + DQ_n$$

$$Q_{n+1} = D(\bar{Q}_n + Q_n)$$

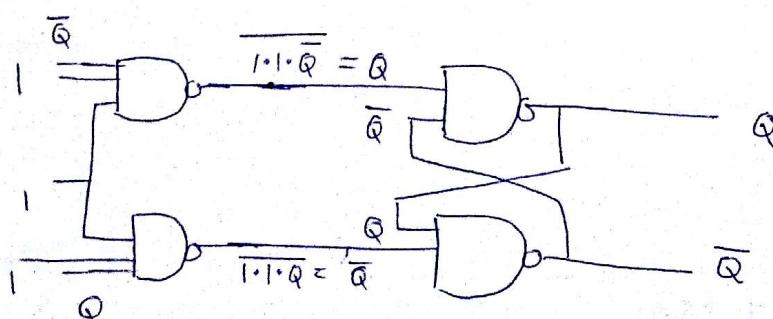
$$Q_{n+1} = D$$

JK Latch



E	J	K	Q_{n+1}	\bar{Q}_{n+1}	Comment
0	X	X	.NC	.NC	No change
1	0	0	$NC(Q_n)$	$NC(\bar{Q}_n)$	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	-	-	Race around condition

$$E = 1 \quad J = 1 \quad K = 1$$



J	K	Q_n	Q_{n+1}
0	0	0	0
0	1	1	1
1	0	0	0
1	1	1	0
1	1	0	1
1	0	1	1
1	1	1	0

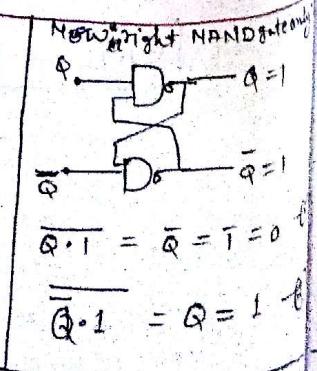
J	K	Q_n	0	1	1	0	1
0	0	0	0	1	1	0	1
0	1	1	0	0	0	1	0
1	0	0	1	0	0	1	1
1	1	1	1	1	0	0	0

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

$$Q_{n+1} = (\overline{J \cdot 1 \cdot \bar{Q}}) \cdot \bar{Q} = \overline{Q \cdot \bar{Q}} = 1$$

$$\bar{Q}_{n+1} = (\overline{J \cdot 1 \cdot Q}) \cdot Q = \overline{\bar{Q} \cdot Q} = \bar{Q} = 0$$

In JK Latch when both inputs J and K are 1 then the Old Q^{old}

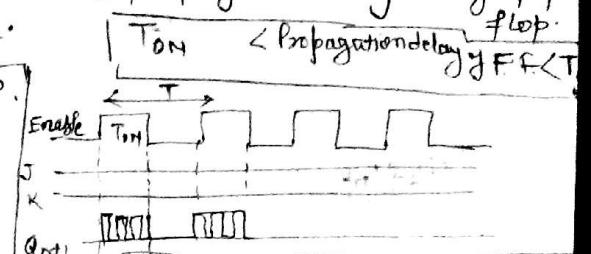


Q is not stable. It will move from 1 to 0 and 0 to 1 when $J=K=1$. This situation is called Race around condition. This is due to feedback connections in the Gate. To avoid this, clock pulses must have a time duration which is shorter than the propagation delay through flip-flop.

How to avoid race around condition -,

1. Using edge triggered JK flip flop.

2. Using master-slave JK flip flop.



Edge triggered flip flop: An edge triggered flip flop is one that is activated by rising edge or falling edge of the clock (synchronizing signal).



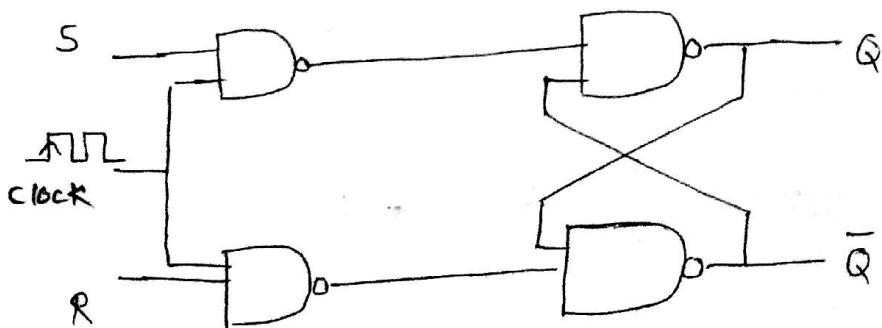
zero to one



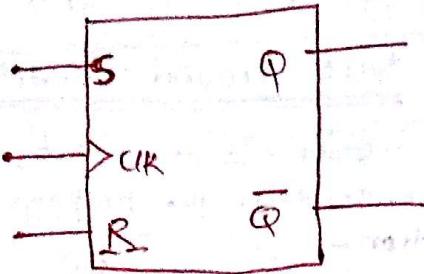
one to zero



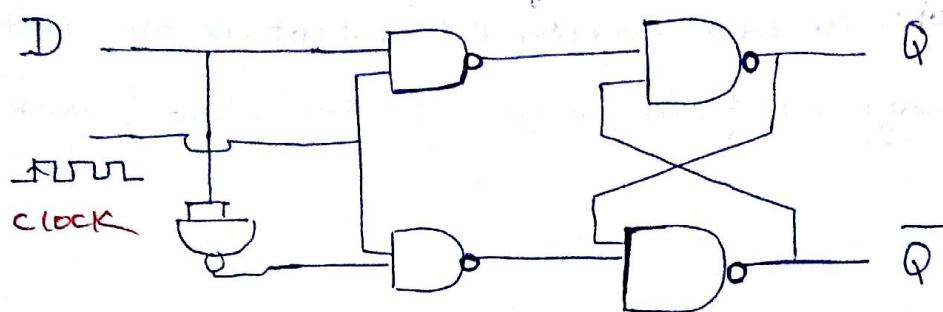
SR- flip flop:



Clock	S	R	Q_{n+1}	\bar{Q}_{n+1}	Comment
X	X	X	Q_n	\bar{Q}_n	No change
↑	0	0	Q_n	\bar{Q}_n	No change
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	-	-	Indeterminate

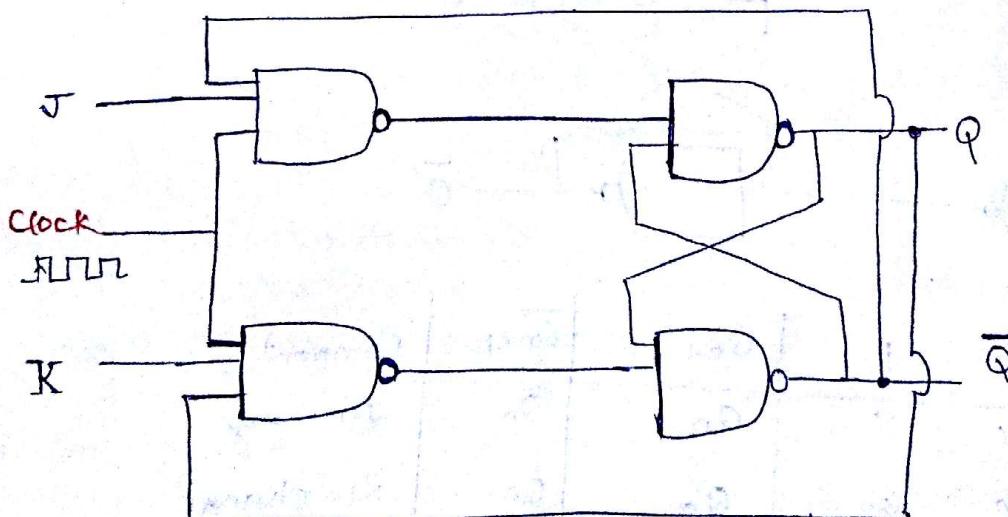


D Flipflop



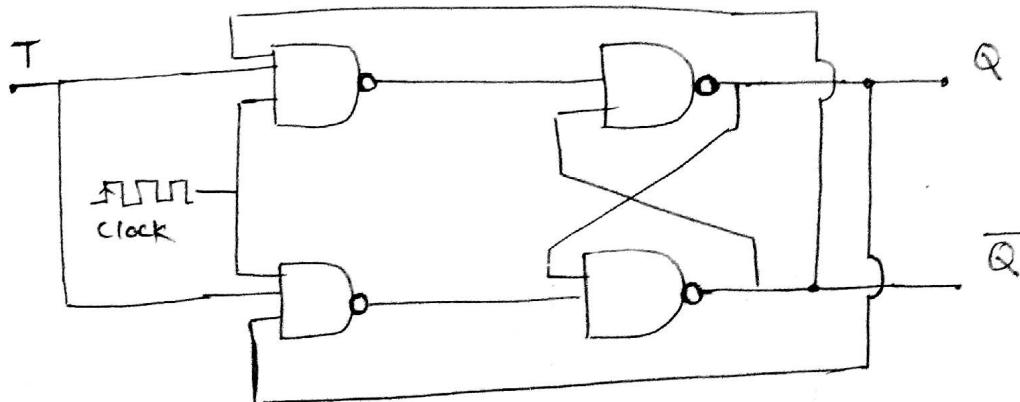
CLOCK	D	Q_{n+1}	\bar{Q}_{n+1}	
X	X	Q_n	\bar{Q}_n	No change
↑	0	0	1	Reset
↑	1	1	0	Set

JK Flipflop :



Clock	J	K	Q_{n+1}	\bar{Q}_{n+1}	Comment
x	x	x	Q_n	\bar{Q}_n	No change
↑	0	0	Q_n	\bar{Q}_n	No change
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	\bar{Q}_n	Q_n	Toggle

T (Toggle flipflop):



Clock	T	Q_{n+1}	\bar{Q}_{n+1}	Comment
x	x	Q_n	\bar{Q}_n	No change
↑	0	Q_n	\bar{Q}_n	No change
↑	1	\bar{Q}_n	Q_n	Toggle

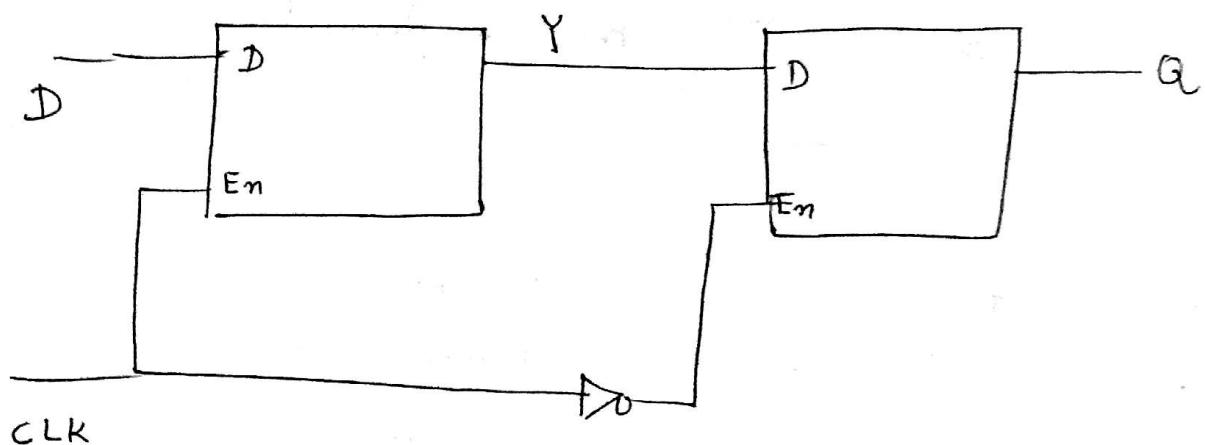
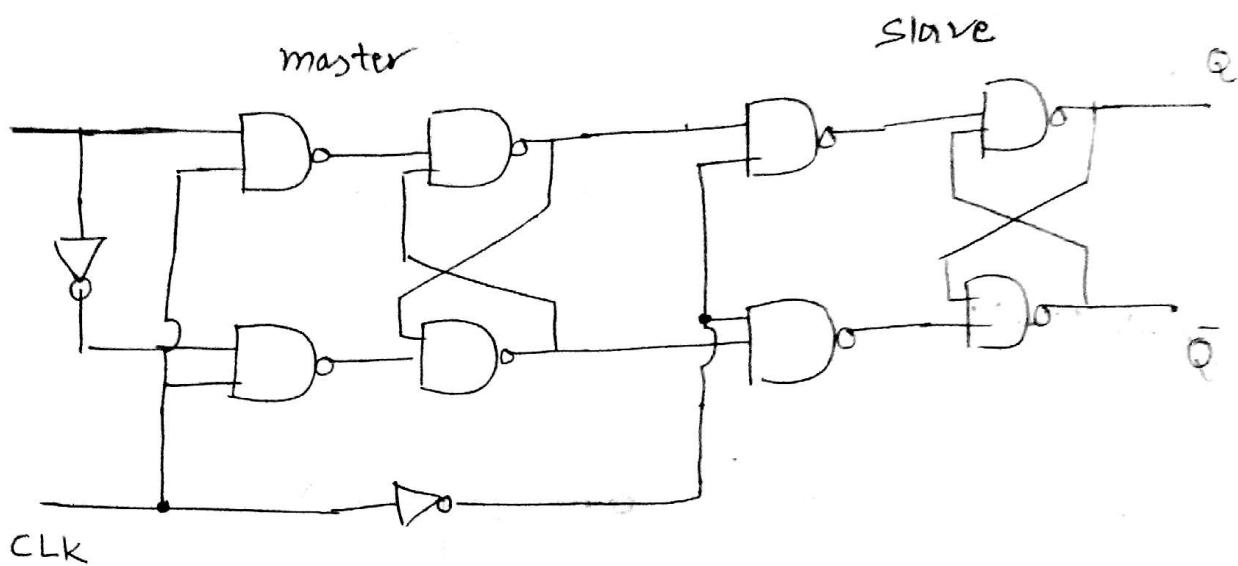
T	Q_n	Q_{n+1}
0	0	0 (NF)
0	1	1 (NF)
1	0	1
1	1	0

$$\therefore Q_{n+1} = \bar{T}Q_n + T\bar{Q}_n$$

$$Q_{n+1} = T \oplus Q_n$$

Master-Slave D flip flop..

The first latch is called master and second the slave.

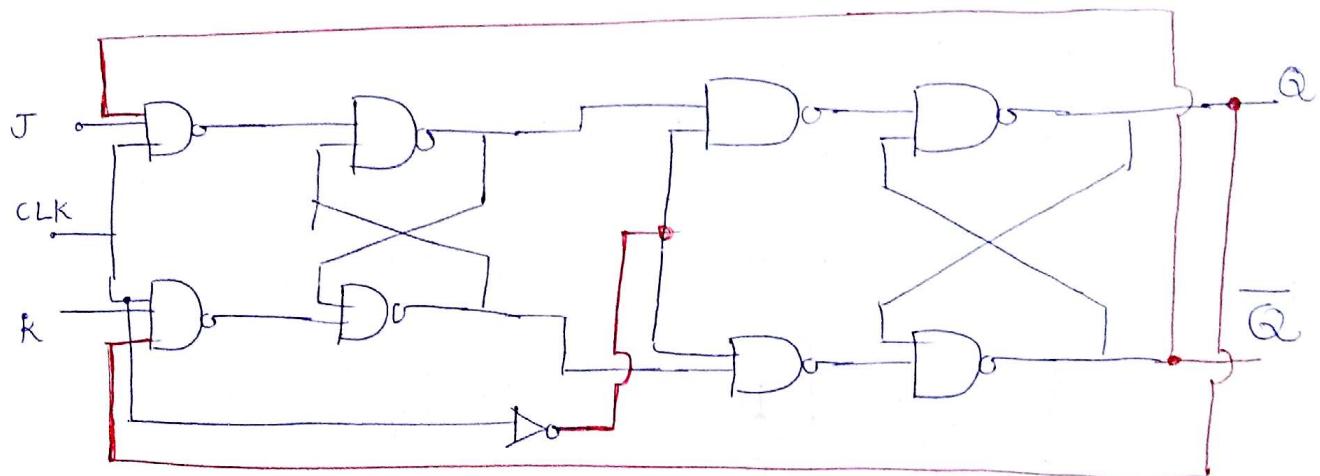


- (i) When $CLK=0$, slave latch is enabled and its output Q is equal to master output Y . Master latch is disabled (because $CLK=0$)
- (ii) When $CLK=1$ The master latch is enabled and slave latch is disabled. The external D input are transferred to master. Thus any change in the input changes the master output at Y but cannot affect the slave output. When the clock pulse

return to zero, the master is disabled and is isolated from D input. At the same time, the slave is enabled and the value of T is transferred to the output of the flip flop at Q.

Thus a change in the output of the flip flop can be triggered only by and during the transition of the clock from 1 to 0.

Master Slave JK flip flop -



(characteristic equation)

$$Q_{n+1} = S + \bar{R} Q_n$$

$$Q_{n+1} = J \bar{Q}_n + \bar{K} Q_n$$

$$Q_{n+1} = D$$

$$Q_{n+1} = T \oplus Q_n$$

Excitation table

(i)

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

(ii)

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(iii)

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

(iv)

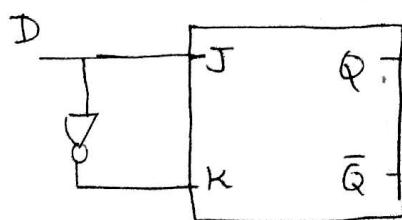
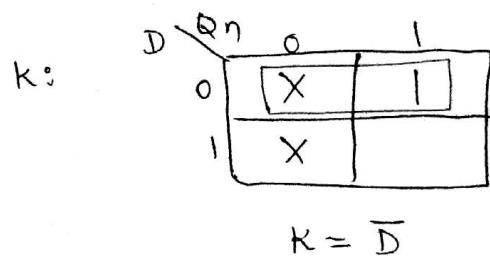
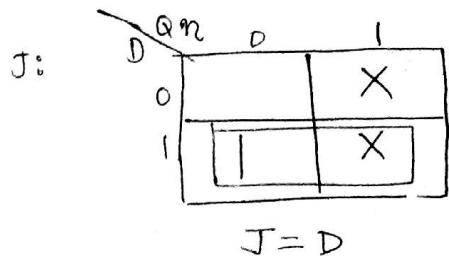
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Conversion from one flipflop to another flipflop:

- Required flipflop characteristic table.
- Available flipflop excitation table.
- Write excitation equation.

JK to D

D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0



JK to SR:

S	R	Q_n	Q_{n+1}	J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	0	X	X	X
1	1	1	X	X	X

J:

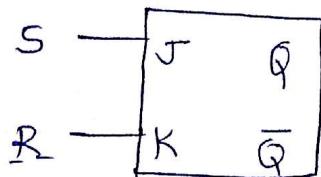
$S \setminus R_{Q_n}$	00	01	11	10
0	X	X		
1		X	X	X

$$J = S$$

K:

$S \setminus R_{Q_n} \setminus Q_n$	00	01	11	10
0	X			
1	X		X	X

$$K = R$$



(iii)

$JK \rightarrow T$

T	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

J:

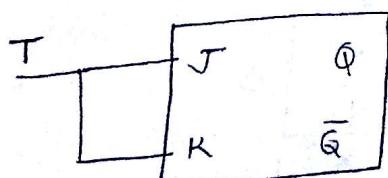
$T \setminus Q_n$	0	1
0		X
1	X	X

$$J = T$$

K:

$T \setminus Q_n$	0	1
0	X	
1	X	1

$$K = T$$



* JK flip-flop is universal flipflop.

JK to D:

$$J = D$$

$$K = \bar{D}$$

JK to SR:

$$J = S$$

$$K = R$$

JK to T:

$$J = T$$

$$K = T$$

SR to D :

$$S = D$$

$$R = \bar{D}$$

SR to JK:

$$S = J\bar{Q}_n$$

$$R = K$$

SR to T :

$$S = T\bar{Q}_n$$

$$R = T$$

$$D \text{ to SR} : D = S + \bar{R}Q_n$$

$$D \text{ to JK} : D = J\bar{Q}_n + \bar{K}Q_n$$

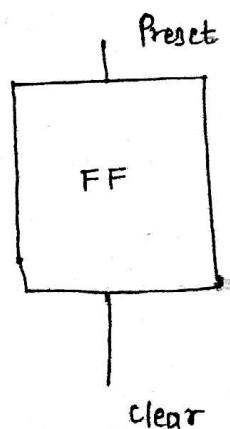
$$D \text{ to T} : D = T \oplus Q_n$$

$$T \text{ to SR} : T = S\bar{Q}_n + RQ_n$$

$$T \text{ to JK} : T = J\bar{Q}_n + \bar{K}Q_n$$

$$T \text{ to D} : T = D \oplus Q_n$$

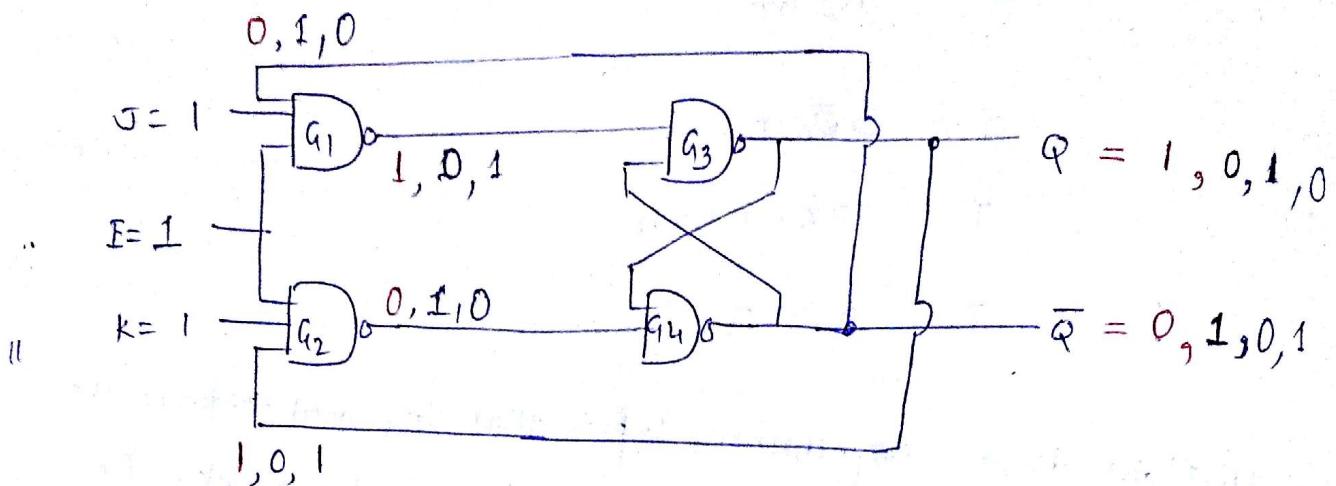
Note: Some flipflops have asynchronous inputs that are used to force the flipflop to a particular state independently of the clock. The input that sets the flipflop to 1 is called preset or direct set. The input that clears the flipflop to 0 is called clear or direct reset. When power is turned on in a digital system, the state of the flipflop is unknown. The direct inputs are useful for bringing all flipflops in the system to a known starting state prior to the clocked operation.



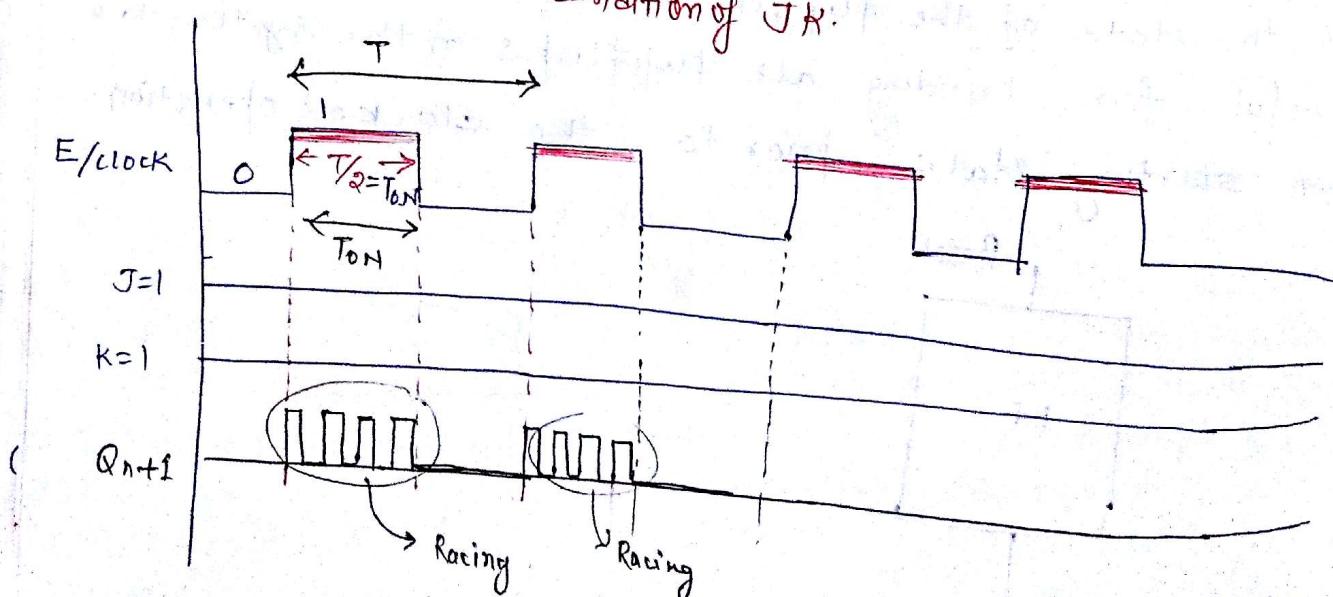
\bar{Q}_n

Q_n

Note Race around condition in JK Latch:



Let initially $Q=1$ and $\bar{Q}=0$. Then output of G_1 will be 1 and G_2 will be 0. Output of G_3 will be 0 and output of G_4 will be 1. Thus output Q has been changed from 1 to 0 and so on. This situation is called race-around condition of JK.



To avoid race-around condition: (conditions to overcome racing)

1. $T_{on} < \text{Propagation delay of FF} < T$
2. Edge trigger JK flipflop
3. Master Slave JK flipflop.