Paper Code: REC-301 Roll No.

B. TECH.
(SEM-III) ODD SEMESTER EXAMINATION2018-19
DIGITAL LOGIC DESIGN

Time: 3.0 Hours **Maximum Marks: 70**

Note: Attempt all questions. All questions carry equal marks.

Q.1. Attempt all parts of the following:- **(3.5x4=14)**

(a) (i) What is the exact number of bytes in a system that contains 32K bytes and 64M bytes.
(ii) Convert the following numbers with the indicated bases to decimal: $(4310)_5$,$(198)_{12}$.
ADD and Multiply without converting them into decimal: hexadecimal 2E and 34.

(b) Draw a NAND logic diagram that implements the complement of the following function:
$F(A,B,C,D) = \sum(0, 1, 2, 3, 6, 10, 11, 14)$

(c) Write first 20 numbers in radix-5. Convert the following to the other canonical form:-
$F(x, y, z) = \sum(1, 3, 5)$

OR

What is a reflected code? Write about reflected codes by giving examples. Also obtain 9's and 10's complement of the following decimal numbers 09900, 10000, 00000.

(d) The Hamming code 010110110 is received at the receiving end. Correct the received data if there is any error.

OR

Realize Ex-OR gate operation with minimal number of NAND gates.

Q.2. Attempt all parts of the following:- **(7x2=14)**

(a) (i) Implement the following using a multiplexer $F(w,x,y,z) = \sum m(0,1,2,3,4,9,13,14,15)$.
(ii) Draw the logic diagram of 8:1 MUX with active low enable input using NAND gates.

(b) Implement the following using a decoder $F(A,B,C,D) = \sum(0,1,4,7,9,12,14)$.

OR

Realize a combinational logic circuit for converting a BCD number to a seven segment display.

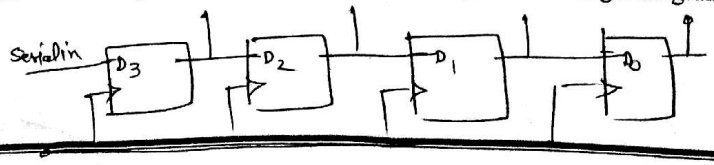
Q.3. Attempt all parts of the following: **(7x2=14)**

(a) The content of a 4-bit register is initially 1101. The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift?

OR

Draw the logic diagram of a four bit binary ripple counter and explain its operation.

(b) Explain the working of serial in parallel out shift register with logic diagram and waveforms.



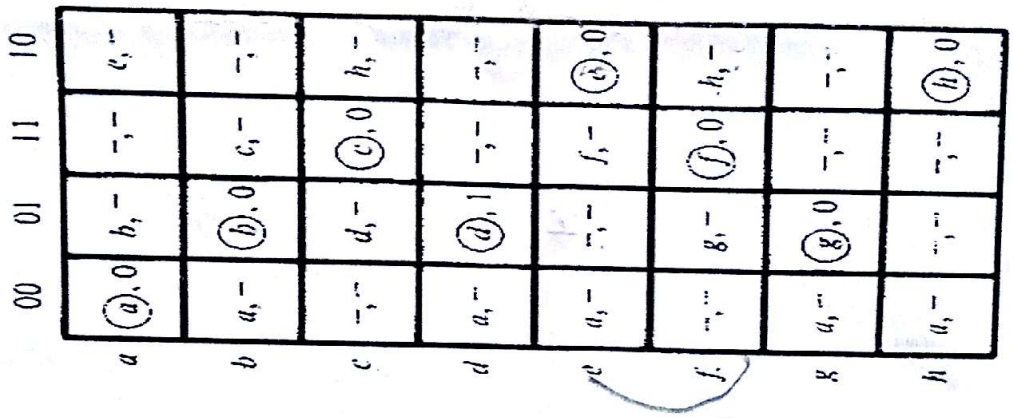
Q.4. Attempt all parts of the following: **(7x2=14)**

(a) An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the circuit are as follows:

$$Y_1 = x_1x_2 + x_1y'_2 + x'_2y_1$$
$$Y_2 = x_2 + x_1y'_1y_2 + x'_1y_1$$
$$Z = x_2 + y_1$$

(i) Draw the logic diagram of the circuit.
(ii) Derive the transition table and output map.
(iii) Obtain a flow table for the circuit.

(b) Merge each of the primitive flow tables shown in Fig.(a) Proceed as follows:



(i) Find all compatible pairs by means of an implication table.
(ii)Find the maximal compatibles by means of a merger diagram.
(iii)Find a minimal set of compatibles that covers all the states and is closed.

OR

Design a circuit that has no static hazards and implements the Boolean function as given below:
$F(w, x, y, z) = \sum(0, 2, 6, 8, 10, 12)$

Q.5. Attempt all parts of the following: **(7x2=14)**

(a) Draw an inverter circuit using a BJT and Explain it's working using numerical values of R_C = 1KΩ, R_B = 22KΩ, h_{FE} = 50, Vcc = 5V V_H = 5V and V_L=0.2V.

(b) Write all the characteristics of digital logic families with diagrams.

OR

(i) Classify the various types of semiconductor memories in short.
(ii) Implement the following function with a PLA:

$$F = \sum (0, 5, 6, 7)$$

1-(a) (i) 32×1024 byte = 32768 bytes

$64 \times 1024 \times 1024$ byte = 67,108,864 bytes

(ii) $(4310)_5 = 4 \times 5^3 + 3 \times 5^2 + 1 \times 5^1 + 0 \times 5^0$

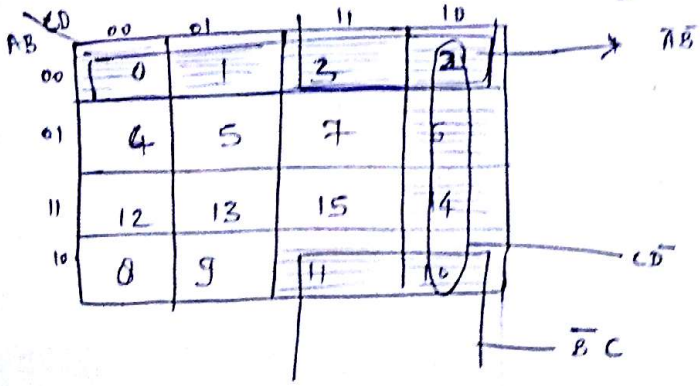
$= 4 \times 125 + 3 \times 25 + 5 + 1 = 580$

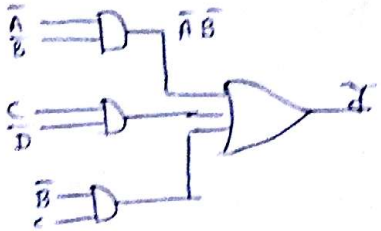
$(198)_{12} = 12^2 + 9 \times 12^1 + 8 \times 12^0 = 144 + 108 + 8 = 260$

2E
2,4
62 Hexadecimal

2E
×31
4×2 4E
3×2 3×E
9 5 8

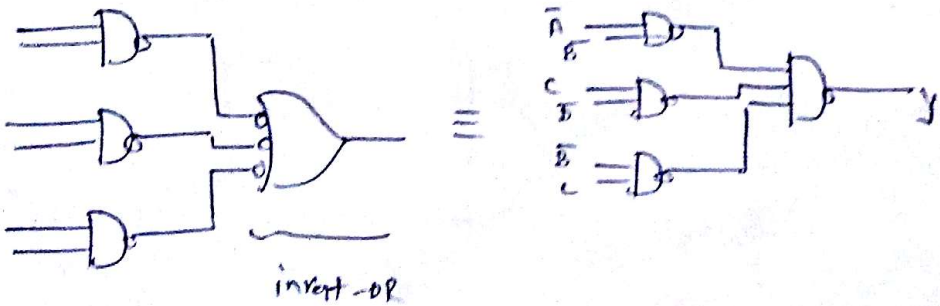
(b) $F(A,B,C,D) = \Sigma(0,1,2,3,6,10,11,14)$





$F = \bar{A}\bar{B} + C\bar{D} + \bar{B}C$

$\bar{F} = (\bar{A}\bar{B} + C\bar{D} + \bar{B}C)' = (A+B)\cdot(C\bar{C}+D)\cdot(B+\bar{C})$



(c)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	decimal
0	1	2	3	4	10	11	12	13	14	20	21	22	23	24	30	31	32	33	34	40	Base-5 (radix 5)

$F(x, y, z) = \Sigma(1, 3, 5)$

$= \Pi[0, 1, 2, 4, 6, 7]$

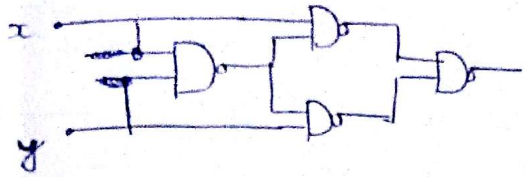
Reflected : It is same as gray code.

0000 —gray→ 0000
0001 —gray→ 0001
0010 —gray→ 0011
0011 —gray→ 0010

99999 −09900 90099	99999 10000 09999	99999 00000 99999	[9's comp

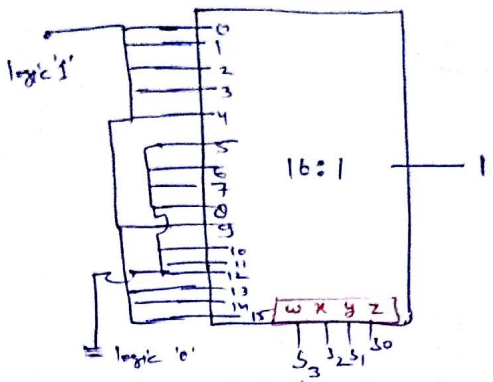
90099 +1 90100	09999 +1 90000	99999 +1 100000

(d) Hamming code



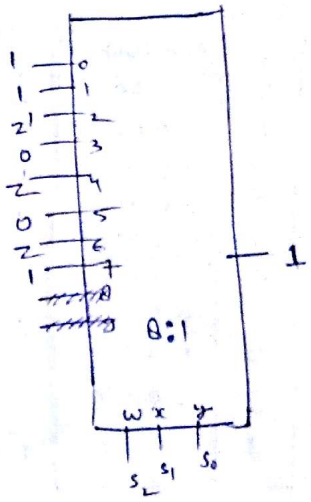
2-(a) $F(w,x,y,z) = \Sigma m(0,1,2,3,4,9,13,14,15)$

Method-I



Method-II

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{z}$	(0)	(2)	(4)	6	8	10	12	(14)
z	(1)	(3)	5	7	(9)	11	(13)	(15)
	1	1	$\bar{z}$	0	z	0	z	1

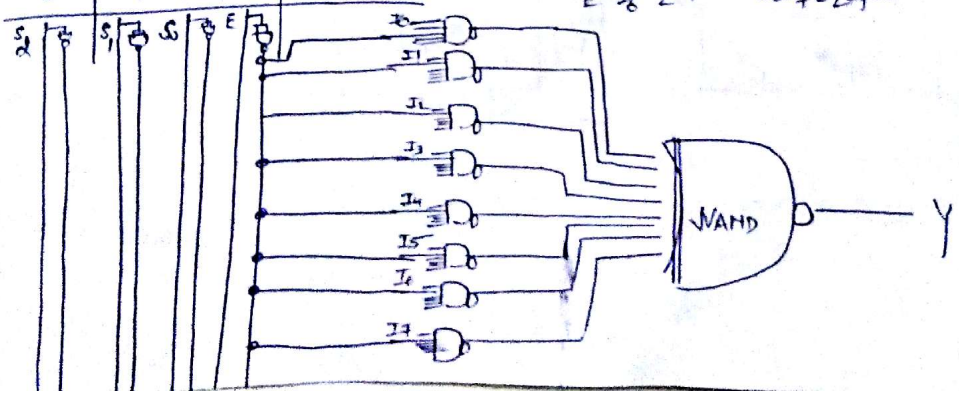


w x y

2(ii)

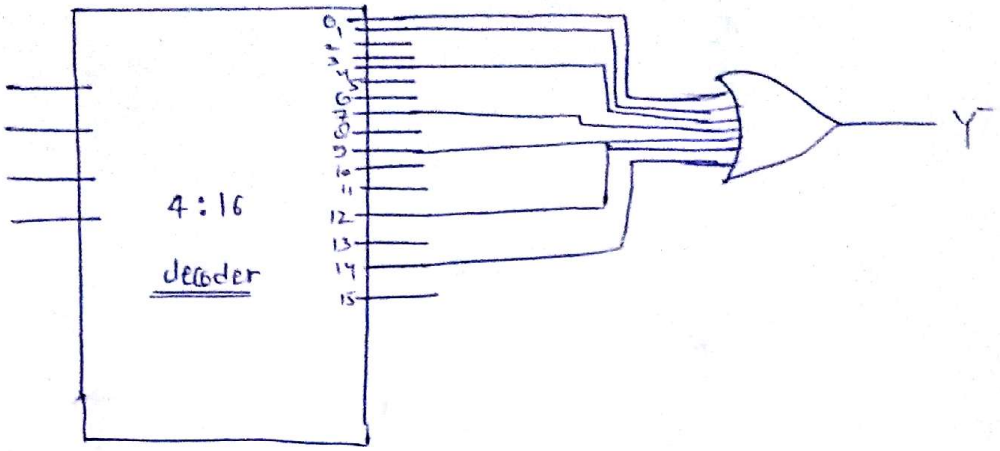
E	S_2	S_1	S_0	Y
0	0	0	0	I_0
0	0	0	1	I_1
0	0	1	0	I_2
0	0	1	1	I_3
0	1	0	0	I_4
0	1	0	1	I_5
0	1	1	0	I_6
0	1	1	1	I_7

$Y = \bar{E}I_0\bar{S}_2\bar{S}_1\bar{S}_0 + \bar{E}I_1\bar{S}_2\bar{S}_1S_0 + \bar{E}I_2\bar{S}_2S_1\bar{S}_0$
$\bar{E}I_3\bar{S}_2S_1S_0 + \bar{E}I_4S_2\bar{S}_1\bar{S}_0 + \bar{E}I_5S_2\bar{S}_1S_0$
$\bar{E}I_6S_2S_1\bar{S}_0 + \bar{E}I_7S_2S_1S_0$



Page(4)

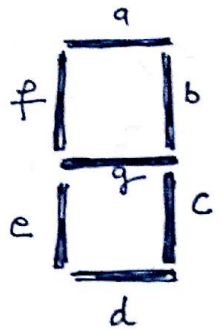
2-(b) $F(A,B,C,D) = \Sigma(0,1,4,7,9,12,14)$



OR

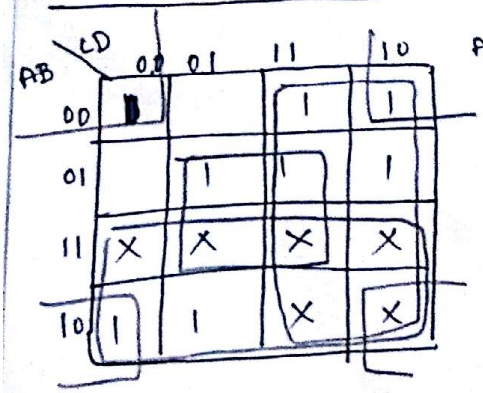
BCD to 7 Segment display :→

Digit	BCD input	a	b	c	d	e	f	g
0	0 0 0 0	1	1	1	1	1	1	0
1	0 0 0 1	0	1	1	0	0	0	0
2	0 0 1 0	1	1	0	1	1	0	1
3	0 0 1 1	1	1	1	1	0	0	1
4	0 1 0 0	0	1	1	0	0	1	1
5	0 1 0 1	1	0	1	1	0	1	1
6	0 1 1 0	1	0	1	1	1	1	1
7	0 1 1 1	1	1	1	0	0	0	0
8	1 0 0 0	1	1	1	1	1	1	1
9	1 0 0 1	1	1	1	1	0	1	1

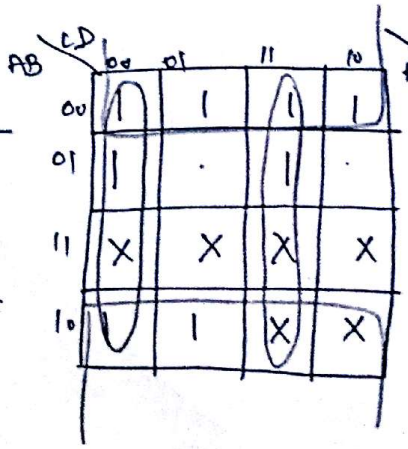


Seven segment display

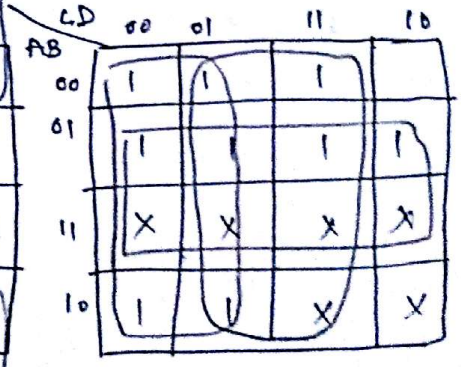
K-map simplification:



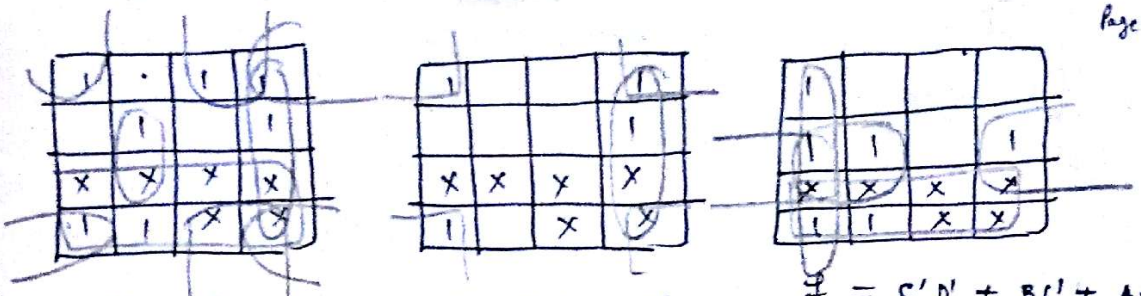
$a = A + C + BD + B'D'$



$b = B' + C'D' + CD$



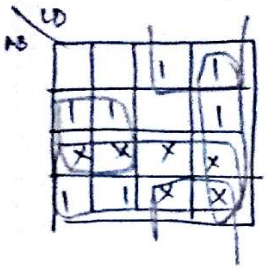
$c = B + C' + D$



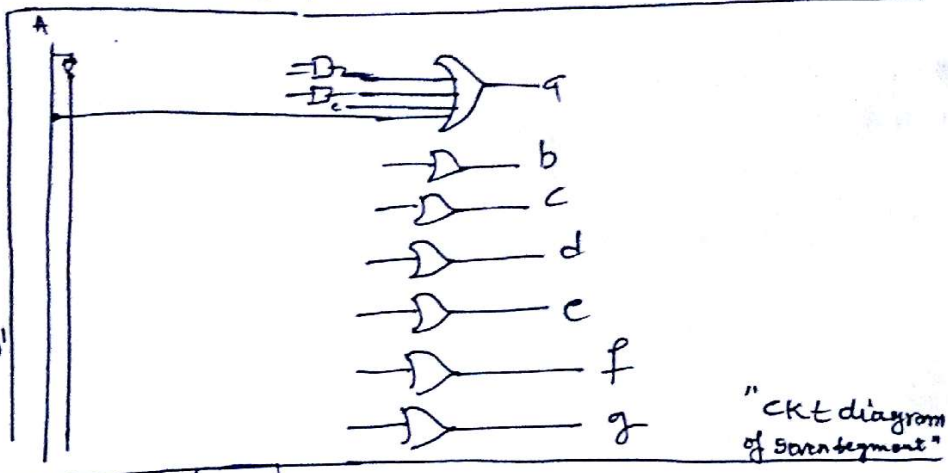
$d = B'D' + CD' + BC'D + B'C + A$

$e = B'D' + CD'$

$f = C'D' + BC' + A + BD'$



$g = A + BC' + B'C + CD'$



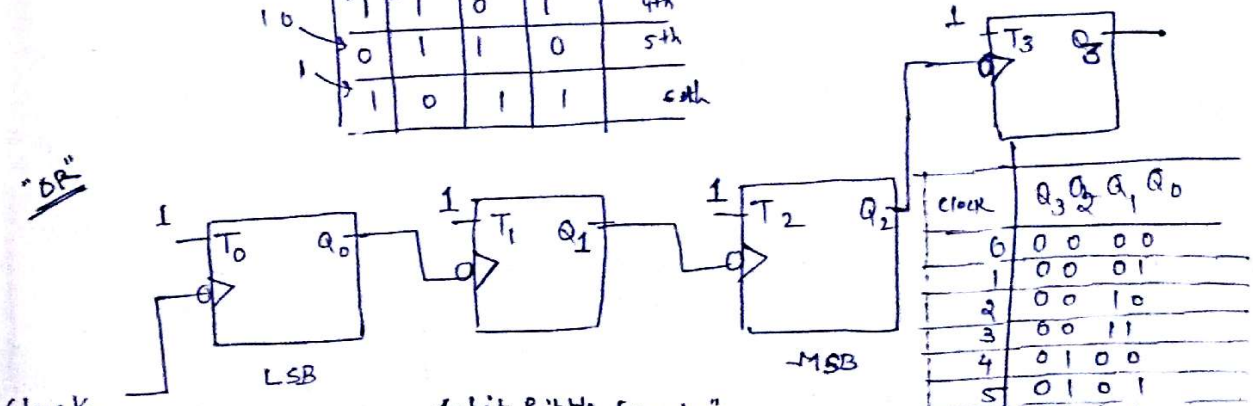
"ckt diagram of Seven segment"

3—(a)

1 0 1 1 0 1	1	1	0	1	initially
1 0 1 1 0	1	1	1	0	1st
1 0 1 1	0	1	1	1	2nd
1 0 1	1	0	1	1	3rd
1 0	1	1	0	1	4th
1	0	1	1	0	5th
	1	0	1	1	6th

"DR"

b)

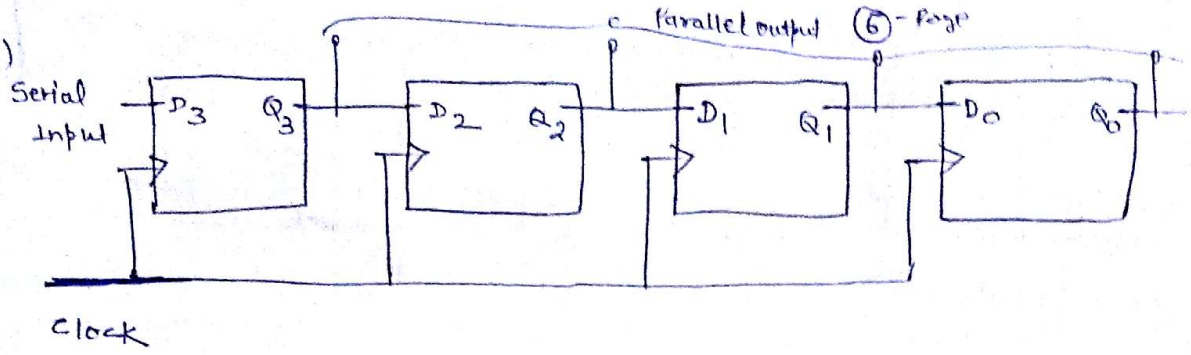


4 bit Ripple Counter"

Clock	$Q_3 Q_2 Q_1 Q_0$
Initially	0 0 0 0
1st	0 0 0 1
2nd	0 0 1 0
3rd	0 0 1 1
4th	0 1 0 0
5th	0 1 0 1
6th	0 1 1 0
7th	0 1 1 1
8th	1 0 0 0
9th	1 0 0 1

Clock	$Q_3 Q_2 Q_1 Q_0$
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1
10	1 0 1 0
11	1 0 1 1
12	1 1 0 0
13	1 1 0 1
14	1 1 1 0
15	1 1 1 1

(b)



* In n bit SIPO register, to provide n-bit data serially in, it requires n clock pulse
* To provide parallel output no clock pulse is required.

[4] $Y_1 = x_1x_2 + x_1y_2' + x_2'y_1$

$Y_2 = x_2 + x_1y_1'y_2 + x_1'y_1$

$Z = x_2 + y_1$

$y_1y_2x_1x_2$	x_1x_2	x_1y_2'	$x_2'y_1$	Y_1	x_2	$y_1'y_2$	$x_1y_1'y_2$	$x_1'y_1$	Y_2	Z
0000	0	0	0	0	0	0	0	0	0	0
0001	0	0	0	0	1	0	0	0	1	1
0010	0	1	0	1	0	0	0	0	0	0
0011	1	1	0	1	1	0	0	0	1	1
0100	0	0	0	0	0	1	0	0	0	0
0101	0	0	0	0	1	1	0	0	1	1
0110	0	0	0	0	0	1	1	0	1	0
0111	1	0	0	1	1	1	1	0	1	1
1000	0	0	1	1	0	0	0	1	1	1
1001	0	0	0	0	1	0	0	1	1	1
1010	0	1	1	1	0	0	0	0	0	1
1011	1	1	0	1	1	0	0	0	1	1
1100	0	0	1	1	0	0	0	1	1	1
1101	0	0	0	0	1	0	0	1	1	1
1110	0	0	1	1	0	0	0	0	0	1
1111	1	0	0	1	1	0	0	0	1	1

(b)

y_1y_2 \ x_1x_2	00	01	11	10
00	(00)	01	11	10
01	00	(01)	11	(01)
11	(11)	01	(11)	10
10	11	01	11	(10)

Transition table

y_1y_2 \ x_1x_2	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	1	1	1
10	1	1	1	1

Map for output

y_1y_2 \ x_1x_2	00	01	11	10
00 = a	(a), 0	b, 1	c, 1	d, 0
01 = b	a, 0	(b), 1	c, 1	(b), 0
11 = c	(c), 1	b, 1	(c), 1	d, 1
10 = d	c, 1	b, 1	c, 1	(d), 1

(c) Flow table

4-[B]

a	(a), 0	b, –	–, –	e, –
b	a, –	(b), a	c, –	–, –
c	–, –	d, –	(c), 0	h, –
d	a, –	(d), 1	–, –	–, –
e	a, –	– –	f, –	(e), 0
f	– –	g, –	(f), 0	h, –
g	a, –	(g), 0	–, –	–, –
h	a, –	– –	–, –	(h), 0

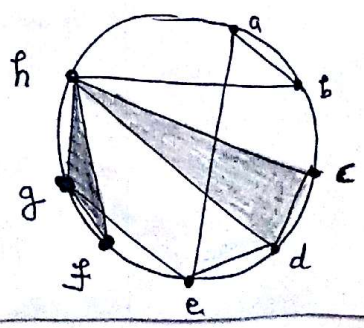
b	✓					
c	b, d × e, h ×	b, d ×				
d	b, d ×	×	✓			
e	✓	c, f ×	c, f ×	✓		
f	b, g × e, h ×	b, g × c, f ×	d, g × c, f ×	d, g × c, f ×	e, h ×	
g	b, g ×	b, g ×	d, g ×	×	✓	✓
h	e, h ×	✓	✓	✓	e, h ×	✓	✓
	a	b	c	d	e	f	g

(i) The compatible pairs are:

(a,b), (a,e), (b,h), (c,d), (c,h), (d,e), (d,h), (e,g), (f,g), (f,h), (g,h).

(ii) Maximal compatible pairs are:

(f, g, h), (c, d, h), (a, b), (a, e) or (d, e)



(iii) (a,b) (c,d) (e,f,g,h)

(8) Page

OR

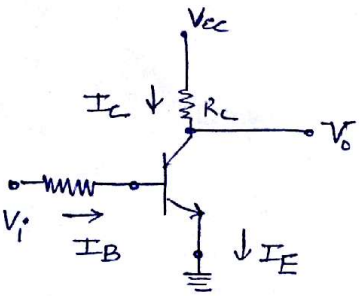
$F(w,x,y,z) = \Sigma(0,2,6,8,10,12)$

wx \ yz	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

$F = \bar{x}\bar{z} + \bar{w}y\bar{z} + w\bar{y}\bar{z}$

There is no static hazard.

[5] $R_C = 1k\Omega$ $R_B = 22k\Omega$ $h_{FE} = 50$ $V_{CC} = 5V$ $V_H = 5V$ $V_L = 0.2V$



Case(i)

$V_i = L = 0.2V$

then $V_{BE} < 0.6V$ therefore transistor is cutoff. The collector emitter circuit behaves like an open circuit, so output voltage $V_o = 5V = H$

Case(ii)

$V_i = H = 5V$, we infer that $V_{BE} > 0.6$

assuming that $V_{BE} = 0.7V$, we calculate

$I_B = \frac{V_i - V_{BE}}{R_B} = \frac{5-0.7}{22k\Omega} = 0.195mA$

$V_{CE} = 0.2V$ (assume), the maximum Collector Current $I_{CS} = \frac{V_{CC} - 0.2}{R_C} = \frac{5-0.2}{1k\Omega} = 4.8mA$

thus $I_B \geq \frac{I_{CS}}{h_{FE}}$

$0.195 \geq \frac{4.8}{50}$

$.195 \geq 0.096mA$

* thus transistor is saturated and output voltage $V_o = V_{CE} = 0.2V$ thus the circuit behaves as an inverter.

5-(b) Fan in and fan-out, Power dissipation, Propagation delay, Noise margin, figure of merit.

Power dissipation – The power dissipated per logic gate.

Propagation delay – Time required to get the output when input is given.

Fanout - It is the maximum number of logic gates that can be driven by logic gate output without affecting its operation

Figure of merit = Power dissipation * Propagation delay

$= P_{diss.} * t_{pd}$

Noise margin – It is the maximum noise voltage that can be added to a logic gate input which will not affect the output

Types of semiconductor memories.

RAM

ROM

PROM

EPROM

EEPROM

ii) $F = \Sigma(0, 5, 6, 7)$

A \ BC	00	01	11	10
0	0	1	3	2
1	4	5	7	6

$F = \bar{A}\bar{B}\bar{C} + AC + AB$