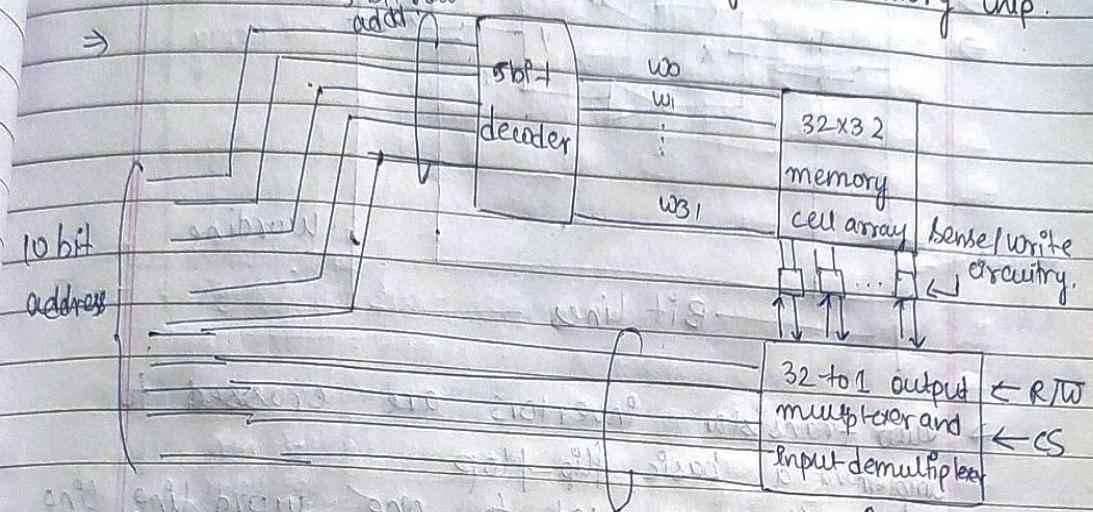


Unit 3:-

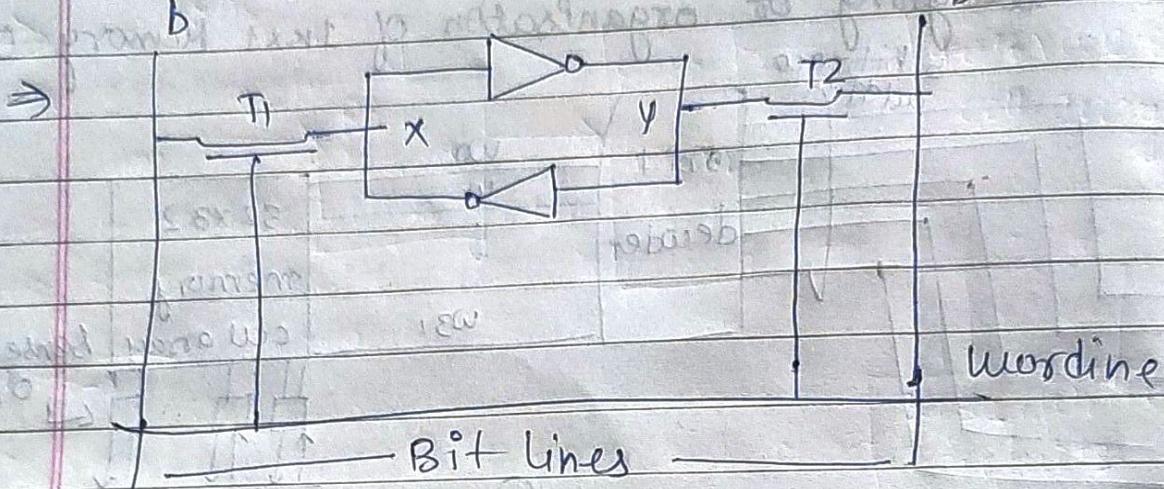
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Q1. Explain designing or organisation of  $1k \times 1$  Memory Chip.



- 1  $k \times 1$  memory chip consists of a  $32 \times 32$  memory cell array, 5 bit decoder and 32 to 1 output multiplexer and input demultiplexer.
- 10 bit address is needed but there is only one data line.
- So required 10-bit address is divided into 2 groups of 5 bits each to form a row and column address for the cell array.
- Row address selects a row of 32 cells, all of which are selected in parallel.
- According to the column Address only one of these cells is connected to the external data line by the output multiplexer and input demultiplexer.

Q2 Explain static Ram cell and also Read and write operations for the same.

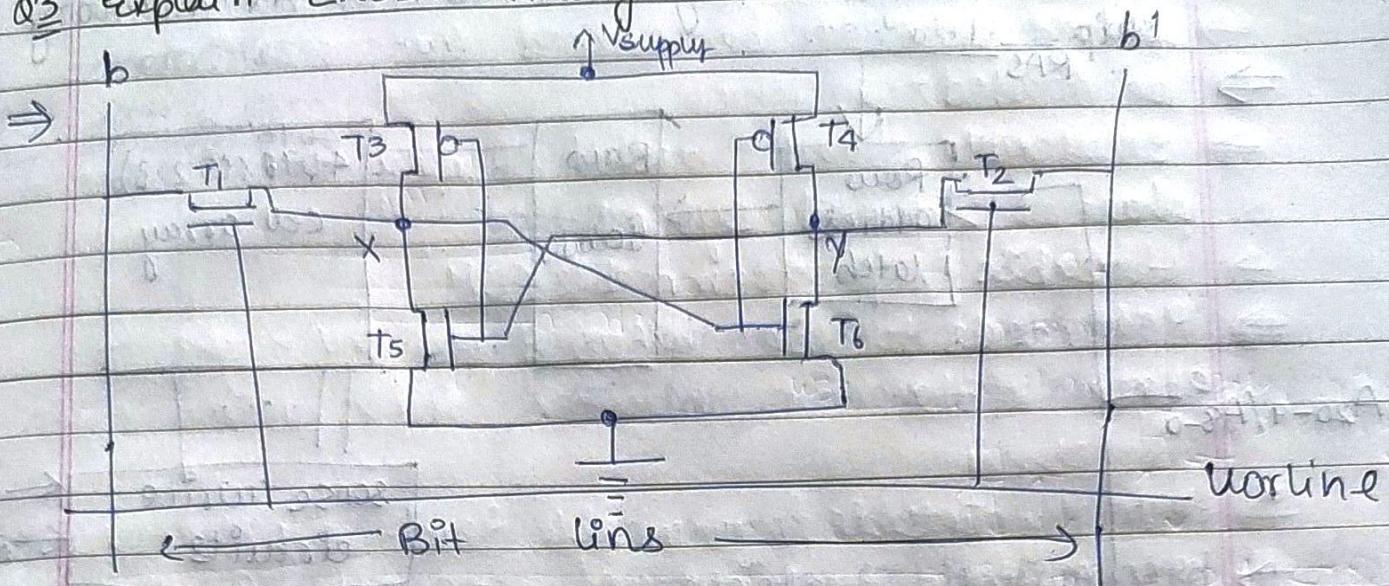


- Two transistor invertors are crossed to implement a basic flip-flop
- The cell is connected to one word line line and two bit lines by transistors  $T_1$  and  $T_2$ .
- When word line is at the ground level, the transistors are turned off and the latch retains its state
- Read operation:-

In order to read state of SRAM cell, the word line is activated to close switches  $T_1$  and  $T_2$ . Sense / Write circuits at the bottom monitor the state of  $b$  and  $b'$ .

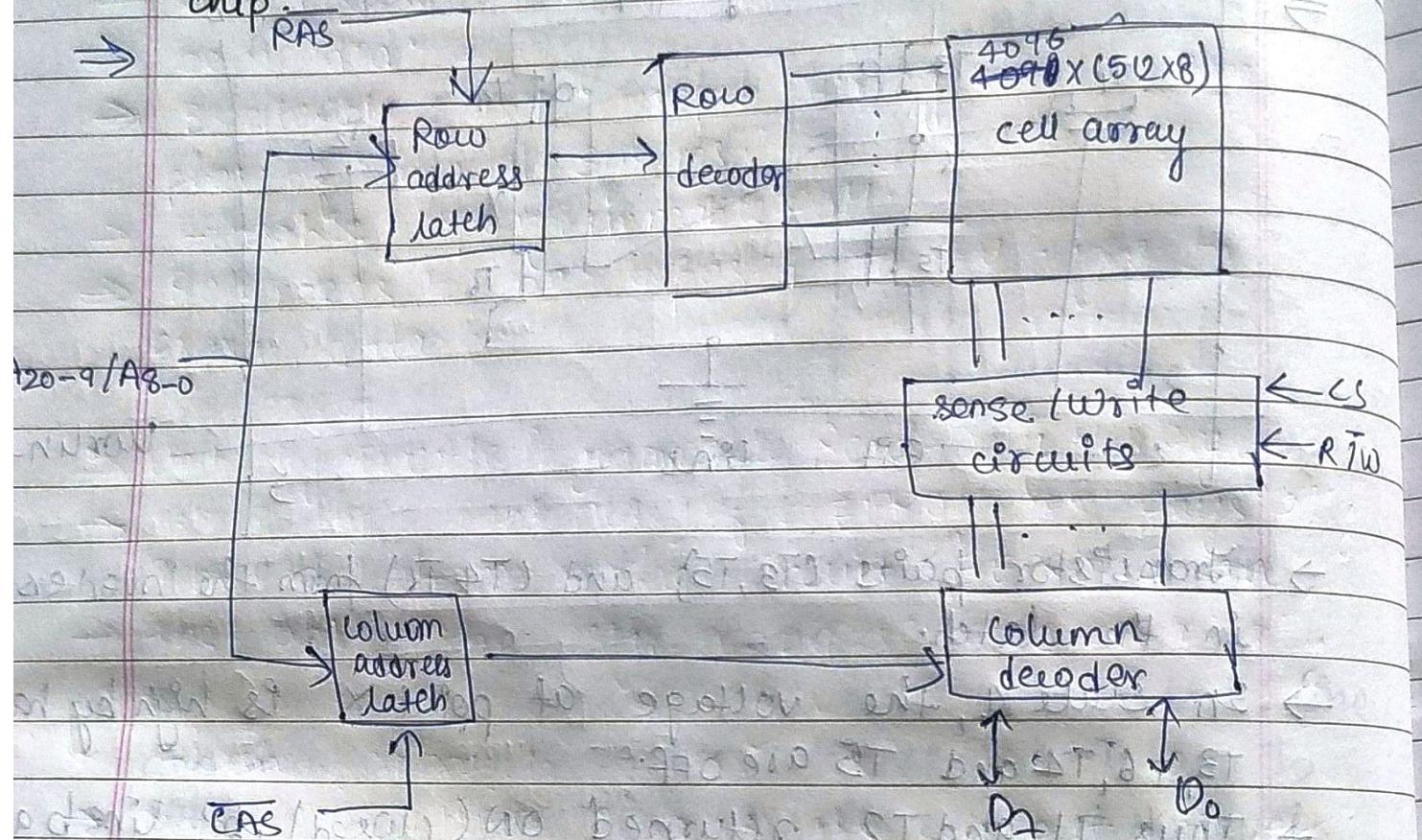
- Write Operation:
  - The state of the cell is set by placing the appropriate value on bit line  $b$  and its complement on  $b'$  and then activating the word line
  - This forces the cell into the corresponding state. The required signal on the bit lines are generated by Sense / write circuit

Q3 Explain CMOS Memory cell.



- Transistor pairs (T3, T5) and (T4, T6) form the inverters in the latch.
- In state 1, the voltage at point X is high by having T3, T6, T4 and T5 are off.
- Thus T1 and T2 returned ON (closed), bit line b and b' will have high and low signals respectively.
- The CMOS requires 5V (in older version) or 3.3V (in new version) of power supply voltage.
- The continuous power is needed for the cell to retain its state.
- Merit: It has low power consumption because the current flows in the cell only when the cell is being accessed.
- Its access time is few nanoseconds.
- Demerit: They have volatile memories, because their contents are lost when the power is interrupted.

Q4 Explain  $2M \times 8$  asynchronous DRAM memory chip.



→ Each row can store 512 bytes. 12 bits to select a row, and 9 bits to select a group in a row. Total 21 bits.

→ First apply row address, RAS signal latches the row address. Then apply the column address, CAS signal latches the column address.

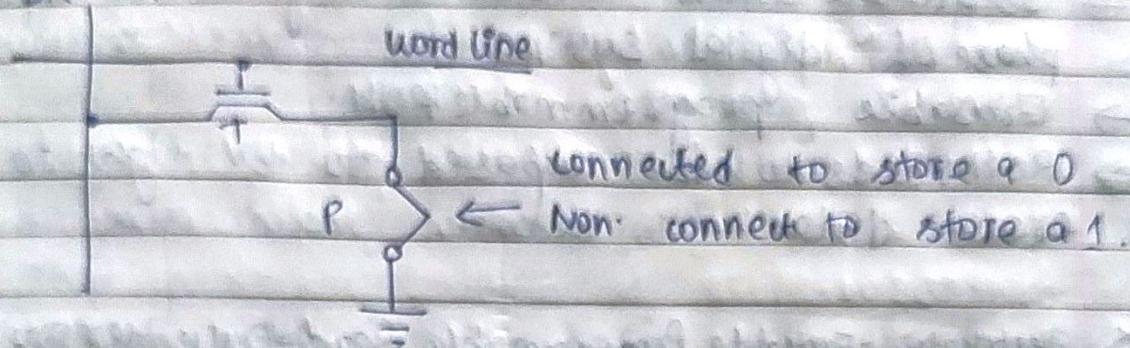
→ Timing of the memory unit is controlled by a specialized units which generates RAS and CAS signals.

→ It consists of a  $4096 \times (512 \times 8)$  cell array, sense circuits, column decoder, column address latch, row decoder, row address latch.

This is a  $2M \times 8$  asynchronous DRAM.

Q5 Explain ROM CELL and compare different ROM memories.

Ans ROM CELL  
Bit line



- At logic value '0' → Transistor (T) is connected to the ground point (P).
- Transistor T is closed and voltage  $V_{DD}$  of bit line nearly drops to zero.
- At logic value '1' → Transistor switch T is open. The bit line remains at high voltage.
- To read the state of the cell, the word line T is activated.
- A sense circuit at the end of the bit line generates the proper output value.
- Data are written into a ROM when it is manufactured.

\* Programmable Read - Only Memory (PROM)

- Allows the data to be loaded by a user
- Process of inserting the data is irreversible.
- Storing information specific to a user in a ROM is expensive.
- Providing programming capabilities to a user may be better.

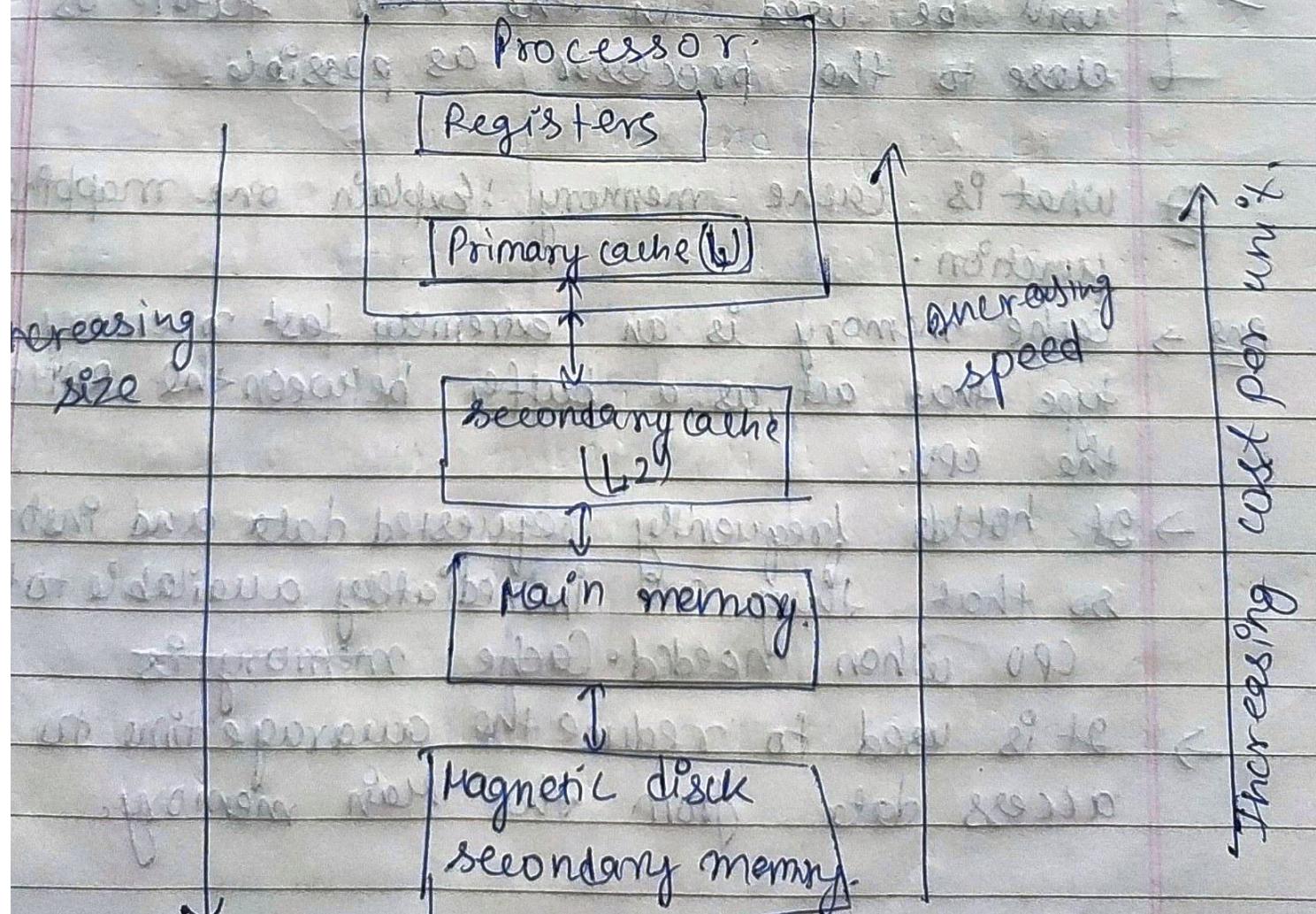
- \* Erasable Programmable Read-Only Memory (EPROM).
  - Stored data to be erased and new data to be loaded.
  - Is flexible and useful during the development phase of digital systems.
  - Erasable, programmable ROM.
  - ROM needs to be exposed to UV light to erase data.

- \* Electrically Erasable Programmable Read-Only Memory (EEPROM)
  - While the contents of EPROM are physically removed from the circuit in EEPROMS, the contents are stored and erased electrically.

- \* Flash Memory
  - Read the contents of a single cell, but write the contents of an entire block of cells.
  - Has similar approach to EEPROM.
  - Has greater density.
  - Power consumption is very low, making it attractive for use in equipment that is battery-driven.
  - Single flash chips are not sufficiently large, so large memory modules, flash cards and flash drives are used.

Q6 Explain memory hierarchy wrt speed, size and cost.

- A big challenge in the design of a computer system is to provide a sufficiently large memory, with a reasonable speed at an affordable cost.
- \* Static RAM: very fast, but expensive, because a basic SRAM cell has a complex circuit making it impossible to pack a large number of cells onto a single chip.
  - \* Dynamic RAM: simpler basic cell circuit, hence are much less expensive, but significantly slower than SRAMs.
  - \* Magnetic disks: storage provided by DRAMs is higher than SRAMs, but is still less than what is necessary. Magnetic disks provide a large amount of storage, but is much slower than DRAMs.



- Fastest access is to data held in processor registers. Registers are at the top of the memory hierarchy.
- Relatively small amount of memory that can be implemented on the processor chip. This is processor cache.
- Level 1 cache is on the processor chip.  
Level 2 cache is between main memory and processor.
- Next level is main memory, implemented as SDRAMs. Much larger, but much slower than cache memory.
- Next level is magnetic disks. Huge amount of inexpensive storage.
- { speed of memory access is critical, the idea is to bring instructions and data that will be used in the near future as close to the processor as possible.

- Q What is Cache memory? Explain one mapping function.
- Cache memory is an extremely fast memory type that act as a buffer between the RAM and the CPU.
  - It holds frequently requested data and instruction so that they are immediately available to the CPU when needed. Cache memory is used to reduce the average time to access data from the main memory.

Mapping functions determine how memory blocks are placed in the cache.

A simple processor example

- Cache : 128 blocks of 16 words each
- Cache size : 2048 (2k) words
- Main memory is addressable by a 16-bit address
- Main memory has 64K words
- Main memory has 4k blocks of 16 words each

### 1. Direct mapping

Cache

Tag	Block 0	Block 1	Block 0	Block 1	Block 127	Block 128	Block 129
Tag	Block 1						
Tag	Block 127						

5 | 7 | 4 |  
Main memory address

Block 255
Block 256
Block 257
Block 4095

- Block  $j$  of the main memory maps to  $j \bmod 128$  of the cache. 0 to 0, 129 maps to 1.
- More than one memory block is mapped onto the same position in the cache.
- May lead to contention for cache blocks even if the cache is not full.
- Contention is resolved by allowing new block to replace the old block (FIFO replacement Alg.)
- Memory address is divided into three fields.
  - Low order 4 bits determine one of the 16 words in the block.
  - When a new block is brought into the cache, the next 7 bits determine which cache block this new block is placed in.
  - High order 5 bits determine which of the possible 32 blocks is currently present in the cache. These are tag bits.
- Simple to implement but not very flexible.

- Associative mapping cache

Tag	Block 0
Tag	Block 1
X	X
Tag	Block 127

Tag	Word
12	4

Main memory address

Main memt.

Block 0
Block 1

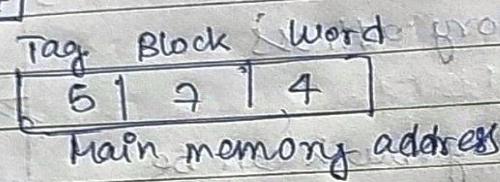
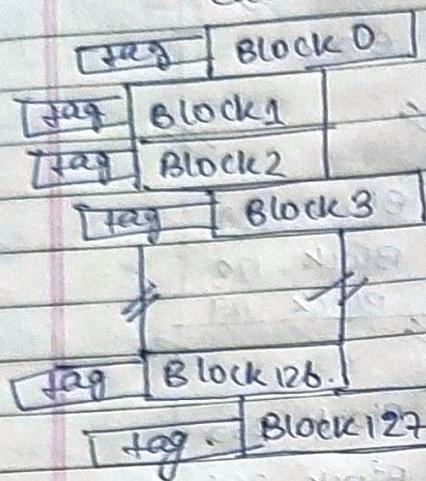
Block 127
Block 128
Block 129

Block 255
Block 256
Block 257

Block 4095
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- Main memory block can be placed in any cache position.
- Memory address is divided into 2 fields
- Low order 4 bits identify the word within a block
- High order 12 bits or tags bits identify a memory block when it is resident in the cache.
- Flexible, and uses cache space efficiently
- Replacement algorithms can be used to replace an existing block in the cache when the cache is full.
- Cost is higher than direct-mapped cache because of need to search all 128 patterns to determine whether a given block is in the cache.

## \* Set - Associative mapping cache.



- Blocks of cache are grouped into sets
- Mapping function allows a block of the main memory to reside in any block of a specific set.
- Divide the cache into 64 sets, with no two blocks per set.
- Memory block 0, 64, 128 etc. map to block 0, and they can occupy either of the two positions.
- Memory address is divided into three fields-
  - 6 bit field determining the set number.
  - 6 high order 6 bit fields are compared to the tag fields of the two blocks in a set.
- Set - associative mapping combination of direct and associative mapping.
- Number of blocks per set is a design parameter.
- One extreme is to have all the blocks in one set requiring no set bits (fully associative mapping)
- Other extreme is to have one block per set, is the same as direct mapping.