UNIT - III

CLOCKS AND FLIP - FLOPS

1 Calculate the time period for a sysbem that uses
(i) 200 KHz clock
(ii) 1 MHz clock

→ (i) $T = \frac{1}{f}$

$= \frac{1}{200 \times 10^3}$

$= 0.5 \times 10^{-5}$

$= 5 \times 10^{-6}$

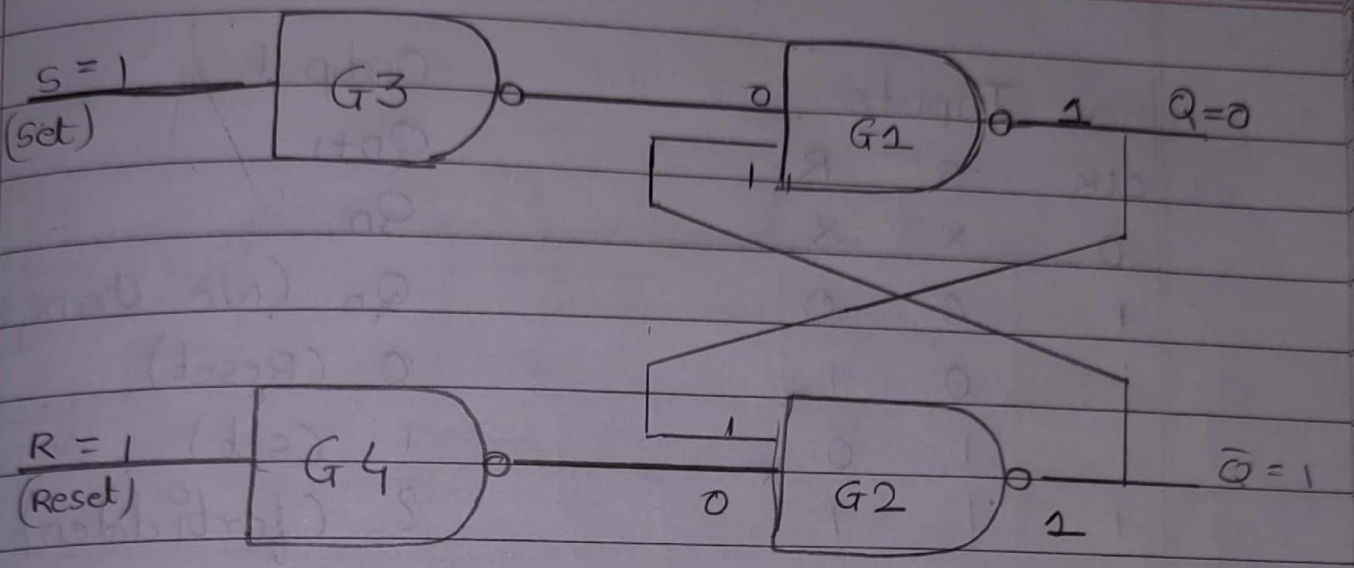
$= 5\ \mu$ sec

(ii) $T = \frac{1}{1 \times 10^{+6}}$

$= 10^{-6}$ sec

$= 1$ Msec

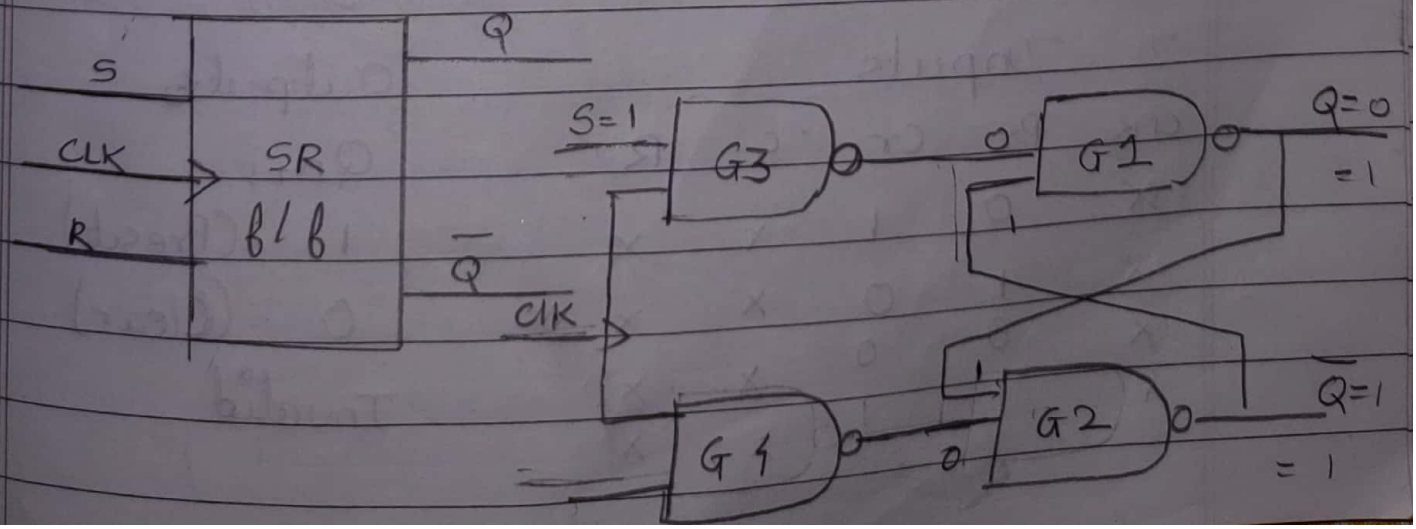
BASIC SR LATCH USING NAND



Inputs		Outputs
S	R	Q_{n+1} (
0	0	Q_n (No change)
0	1	0 (Reset)
1	0	1 (Set)
1	1	? (Forbidden)

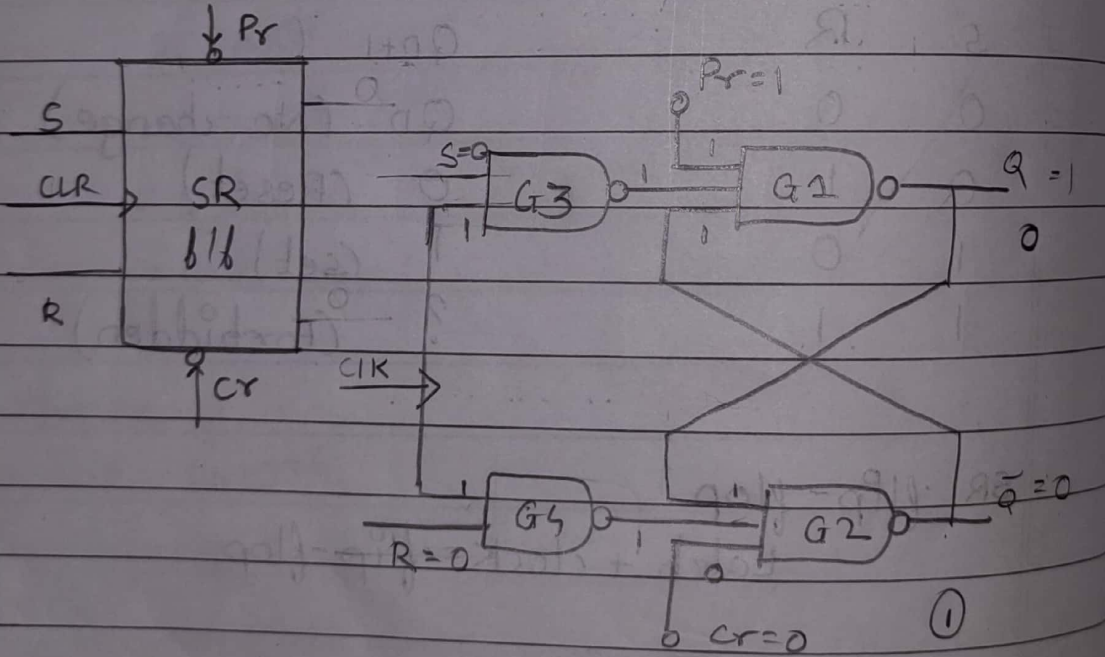
SR flip-flop

Latch + clock = flip-flop.



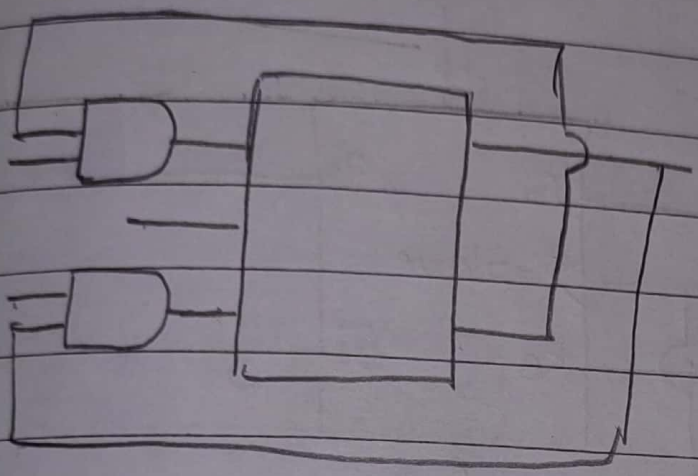
Inputs			Output
CLK	S	R	Q_{n+1}
0	x	x	Q_n
1	0	0	Q_n (No change)
1	0	1	0 (Reset)
1	1	0	1 (set)
1	1	1	? (forbidden)

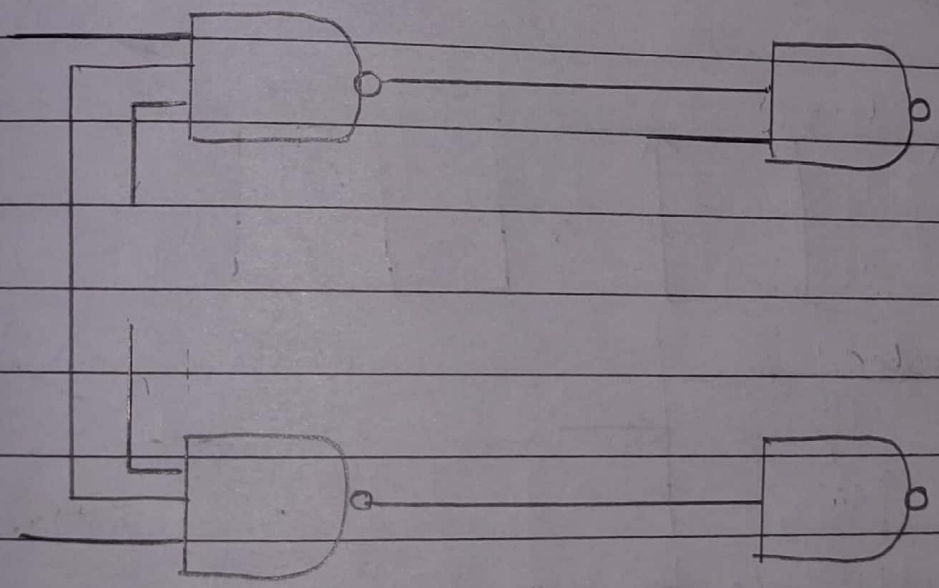
ASYNCHRONOUS INPUTS PRESET & CLEAR



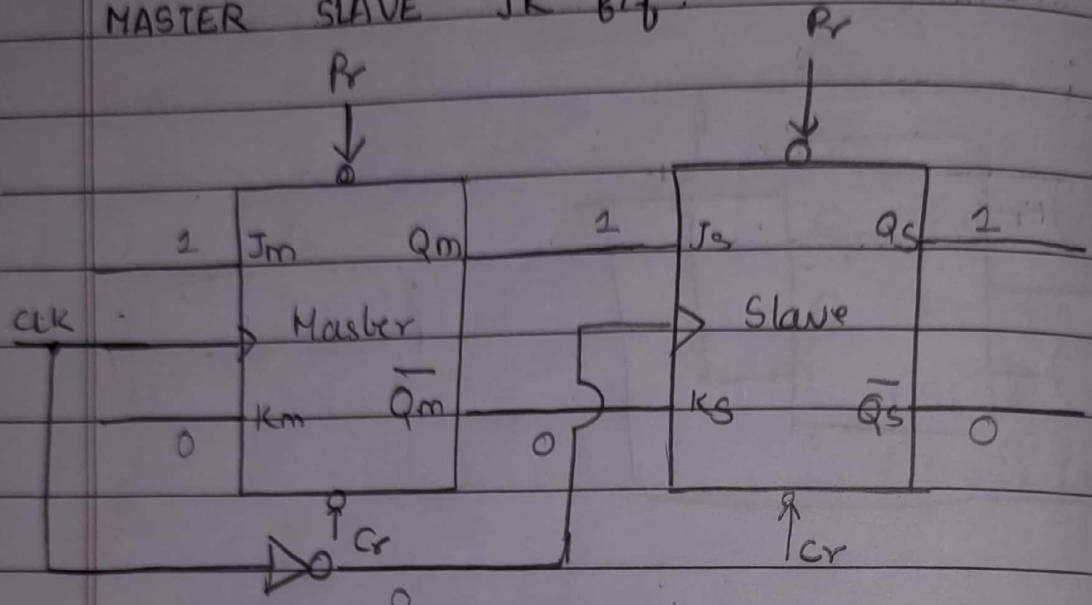
Inputs					Outputs
CLK	Pr	Cr	S	R	Q_{n+1}
X	0	1	x	x	1 (Presch)
X	1	0	x	x	0 (Clear)
X	0	0	x	x	Invalid
X	1	1	x	x	

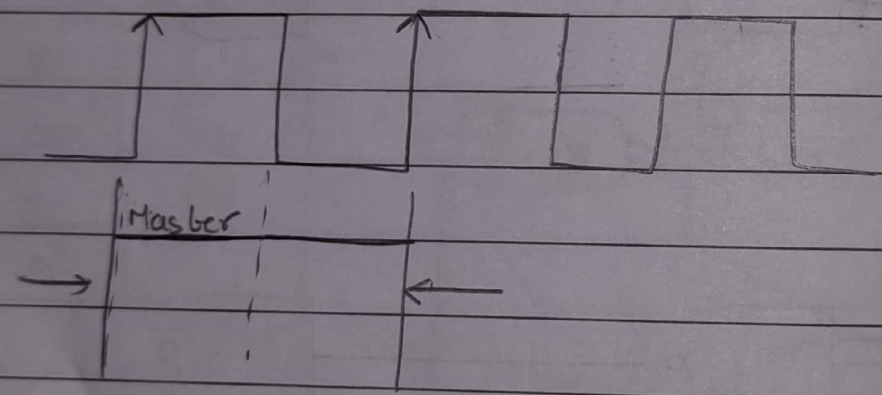
JK ..FLIP - FLOP





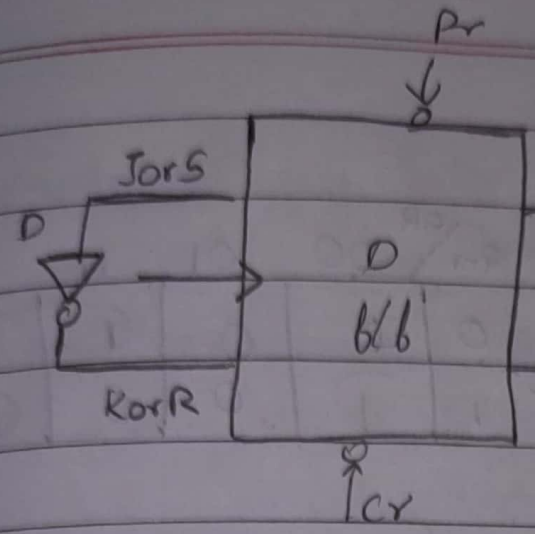
MASTER SLAVE JK f/f.





CLK	S	R	J	K	Q_{n+1}
↓	0	0	0	0	Q_n
↓	0	1	0	1	0
↓	1	0	1	0	1
↓	1	1	1	1	? / $\bar{Q}_n$

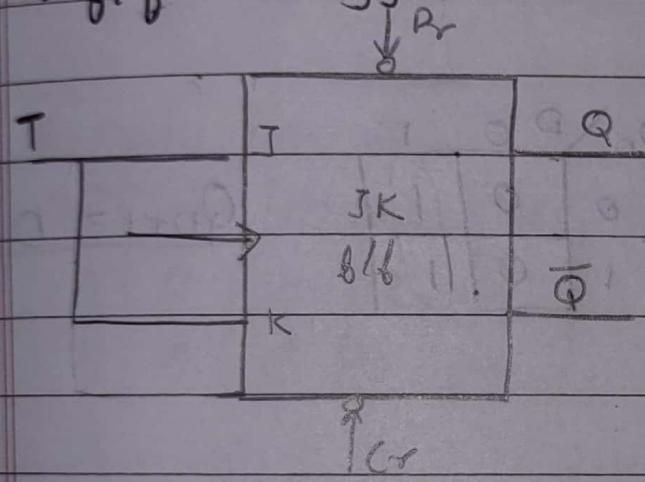
D (f/f) [Delay]



Input		Output
CLK	D	Q_{n+1}
0	x	Q_n
1	0	0
1	1	1

$\therefore$ **$Q_{n+1} = D$**

T f/f [Toggle]



Inputs		Output
CLK	T	Q_{n+1}
0	x	Q_n
1	0	Q_n
1	1	$\overline{Q_n}$

Note

SR flip/flop can not be used to [design] obtain T f/f because of forbbiden state [S = R = 1]

CHARACTERISTIC EQUATIONS

①

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	?

q_n \ SR	00	01	11	10
0	0	0	x	1
1	1	0	x	1

$Q_{n+1} = S + Q_n\bar{R}$

② JK f/f

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

Q_n \ SR	00	01	11	10
0	0	0	1	1
1	1	0	0	1

$$Q_{n+1} = \overline{Q_n} J + Q_n \overline{K}$$

③ D f/f

D	Q_{n+1}
0	0
1	1

Q_n \ D	0	1
0	0	1
1	0	1

$$Q_{n+1} = D$$

④ T f/f

T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

Q_n \ T	0	1
0	0	1
1	1	0

$$Q_{n+1} = \overline{Q_n} T + Q_n \overline{T}$$

$$Q_{n+1} = Q_n \oplus T$$

EXCITATION TABLE

$Q_n \rightarrow Q_{n+1}$	S	R	J	K	D	T
0 → 0	0	X	0	X	0	0
0 → 1	1	0	1	X	1	1
1 → 0	0	1	X	1	0	1
1 → 1	X	0	X	0	1	0

- Convert SR f/f into JK f/f

		Available		Required	
Q_n	Q_{n+1}	S	R	J	K
0	0	0	x	0	x
0	1	1	0	1	x
1	0	0	1	x	1
1	1	x	0	x	0

K-Map for S

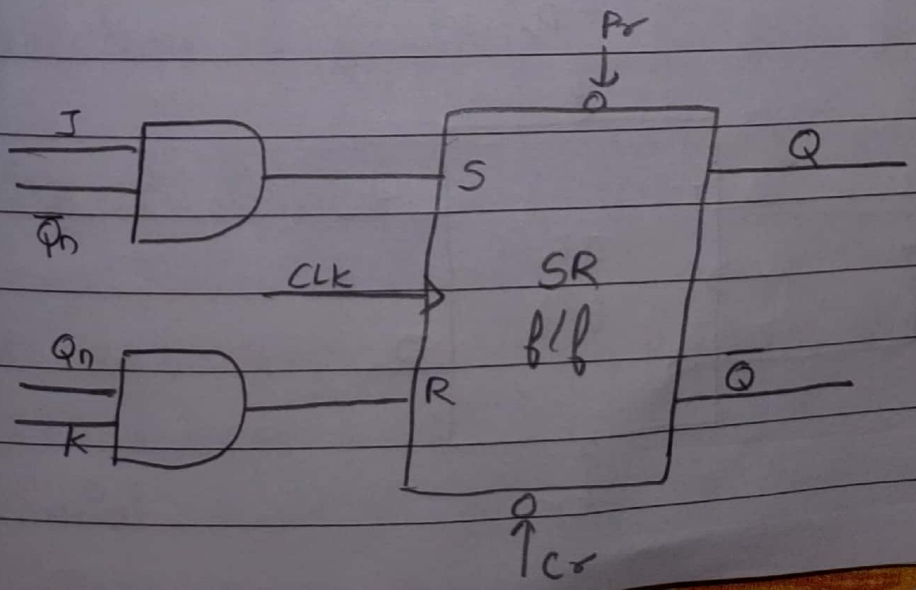
Q_n \ JK	00	01	11	10
0	0	0	1	1
1	x	0	0	x

$S = \bar{Q_n} J$

K-Map for R

Q_n \ JK	00	01	11	10
0	x	x	0	0
1	0	1	1	0

$R = Q_n K$



- Convert JK f/f into D f/f

Q_n	Q_{n+1}	J	K	D
0	0	0	x	0
0	1	1	x	1
1	0	x	1	0
1	1	x	0	1

K-Map for J

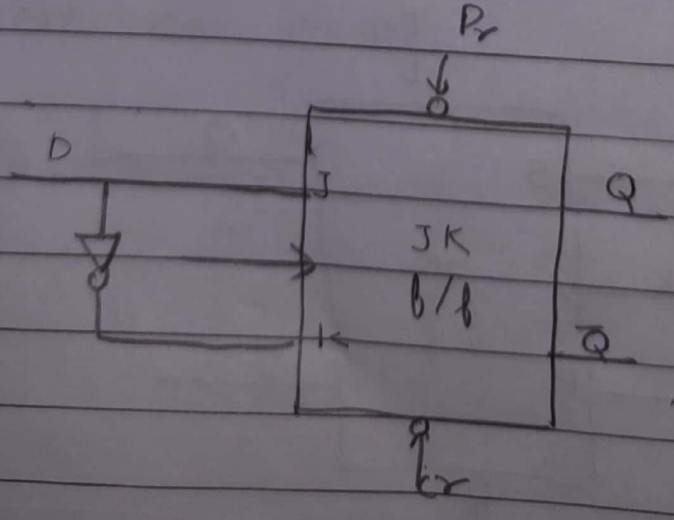
Q_n \ D	0	1
0	0	1
1	x	x

$J = D$

K-Map for K

Q_n \ D	0	1
0	$\bar{x}$	x
1	1	0

$J = \bar{D}$



UNIT - IV

ANALYSIS OF SEQUENTIAL CIRCUITS

DIFFERENCE BETWEEN COMBINATIONL CIRCUITS AND SEQUENTIAL CIRCUIT

	COMBINATIONAL CIRCUIT	SEQUENCIAL CIRCUIT
1.	Output depends on combination input variable	The Output depends not only on the input variables but also on the present state of the circuit
2	Memory unit is not required. Ex = Parallel Adder	2. Memory unit is required to store the previous state. Ex Serial Adder.
3	Execution is faster	3. Execution is slower.
4	Design is simple	4. Design is complicated

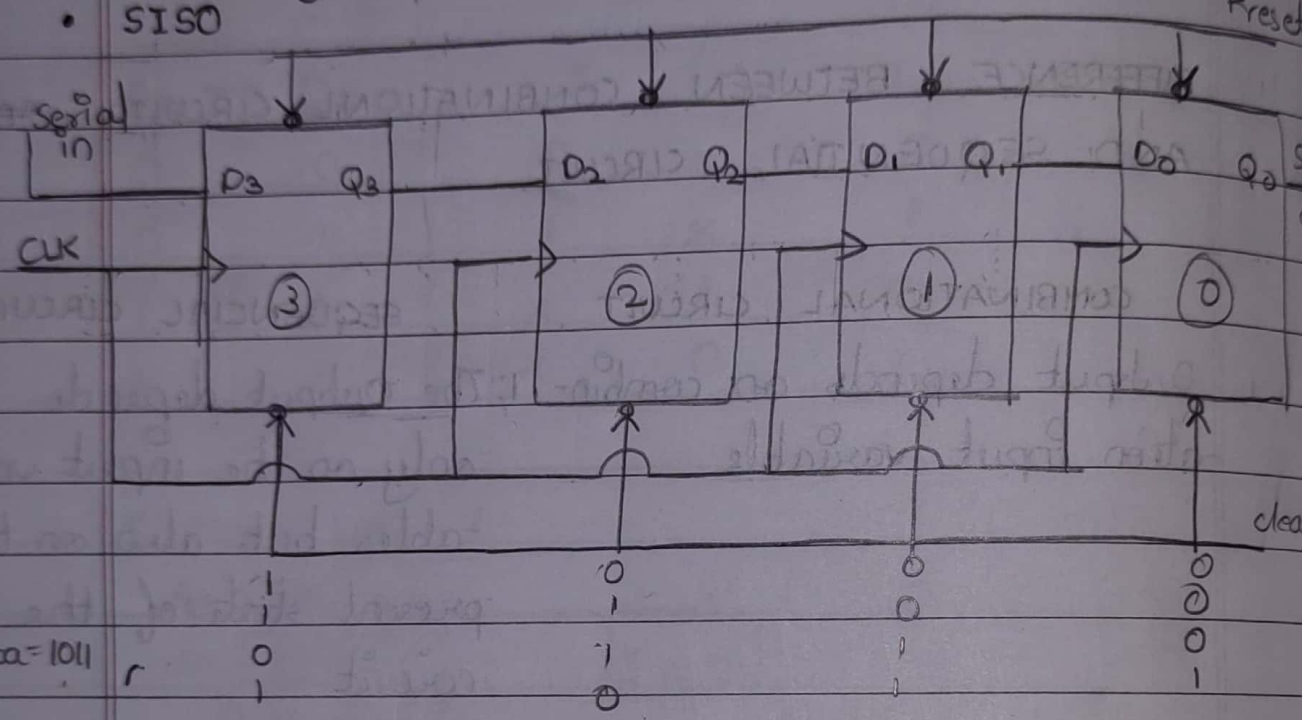
SHIFT REGISTERS

- SISO
- SIPO
- PISO
- PIPO

S - Serial P - Parallel . I - In O - Out

4-bit register (right shift register) 2^n+1 clk pulse

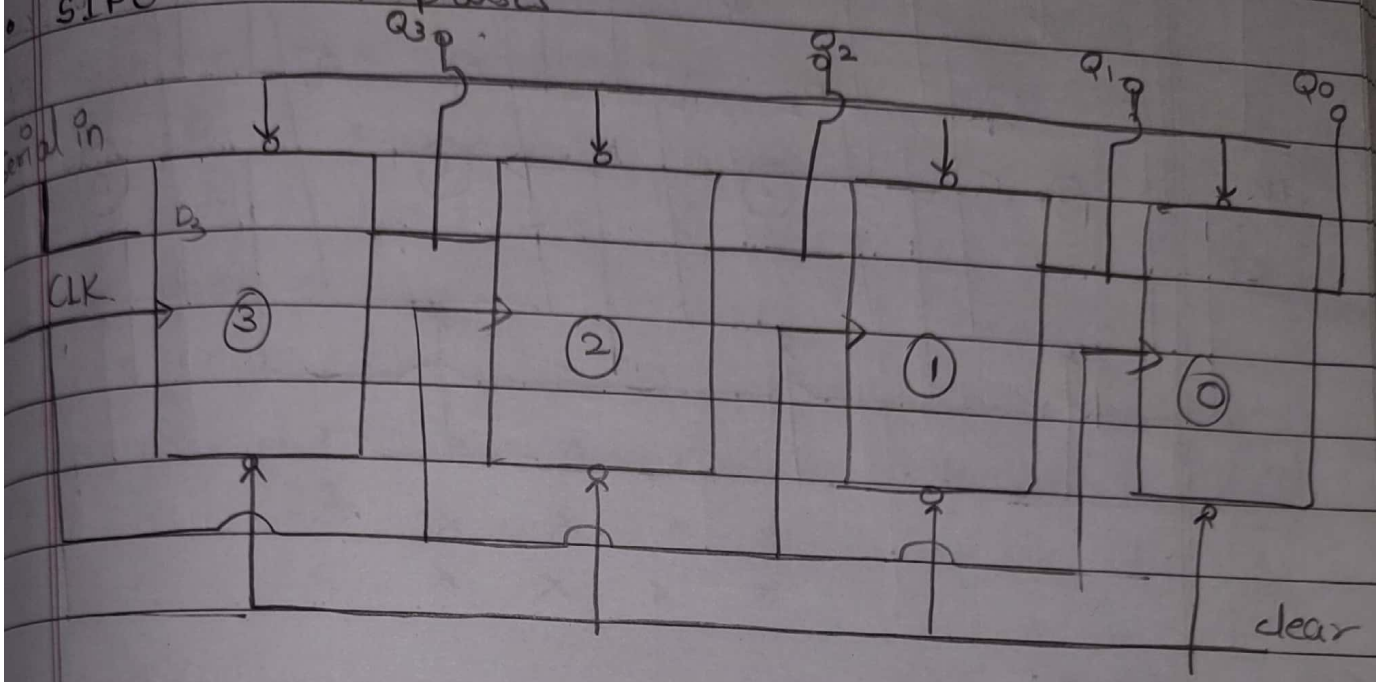
- SISO



Ex
Data = 1011

Gr	Pr	CLK	Serial input (D_3)	Serial Output
			D_3	Q_3 Q_2 Q_1 Q_0
0	1	x	x	0 0 0 0 clear
1	1	1	1 [LSB]	1 0 0 0
1	1	2	0	1 1 0 0
1	1	3	1	0 1 1 0
1	1	4	1 [MSB]	1 0 1 1 LSB
1	1	5	x	x 1 0 1
1	1	6	x	x x 1 0
1	1	7	x	x x x 1 MSB

• SIPO n clk pulses

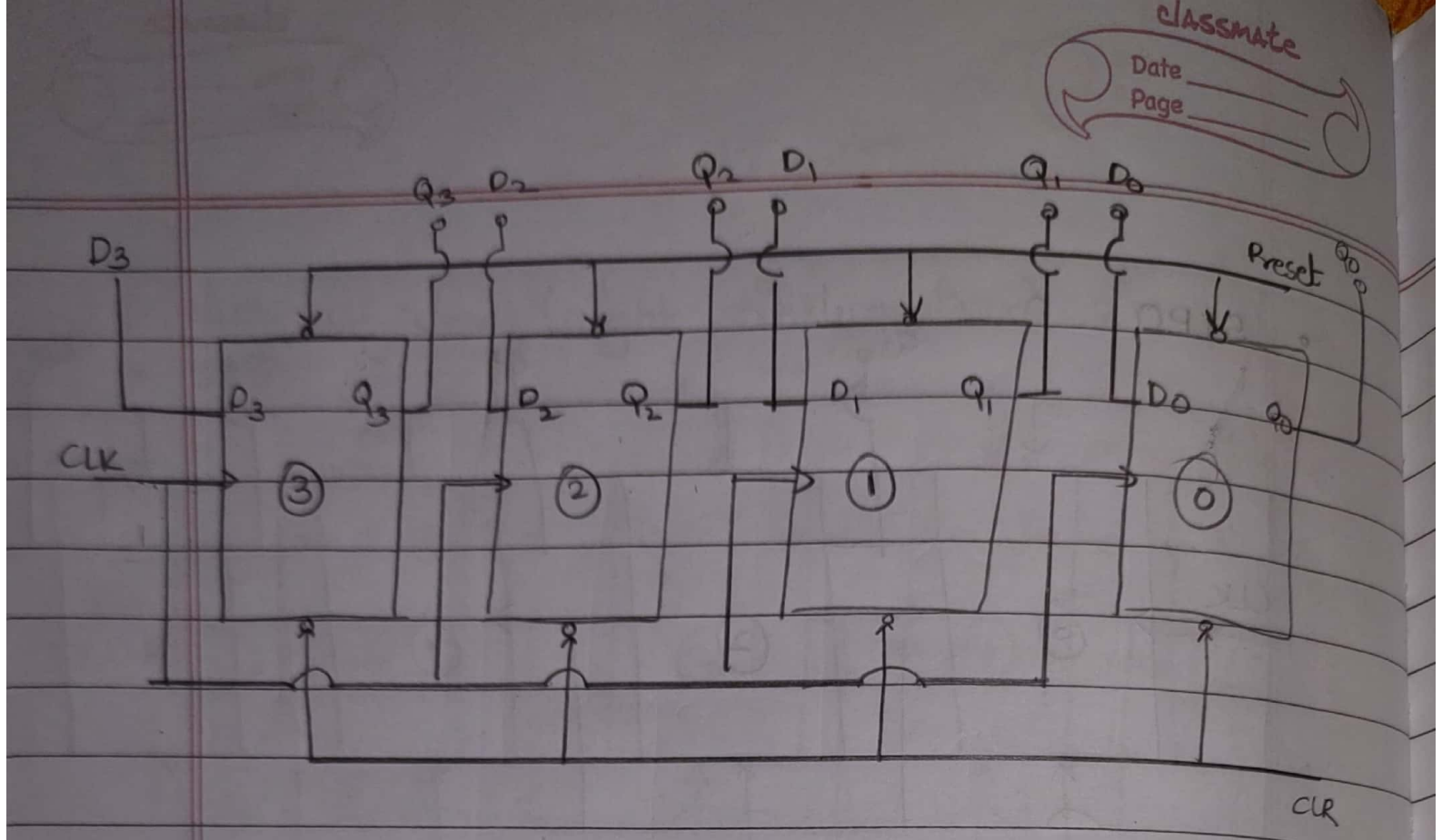


DATA = 1011

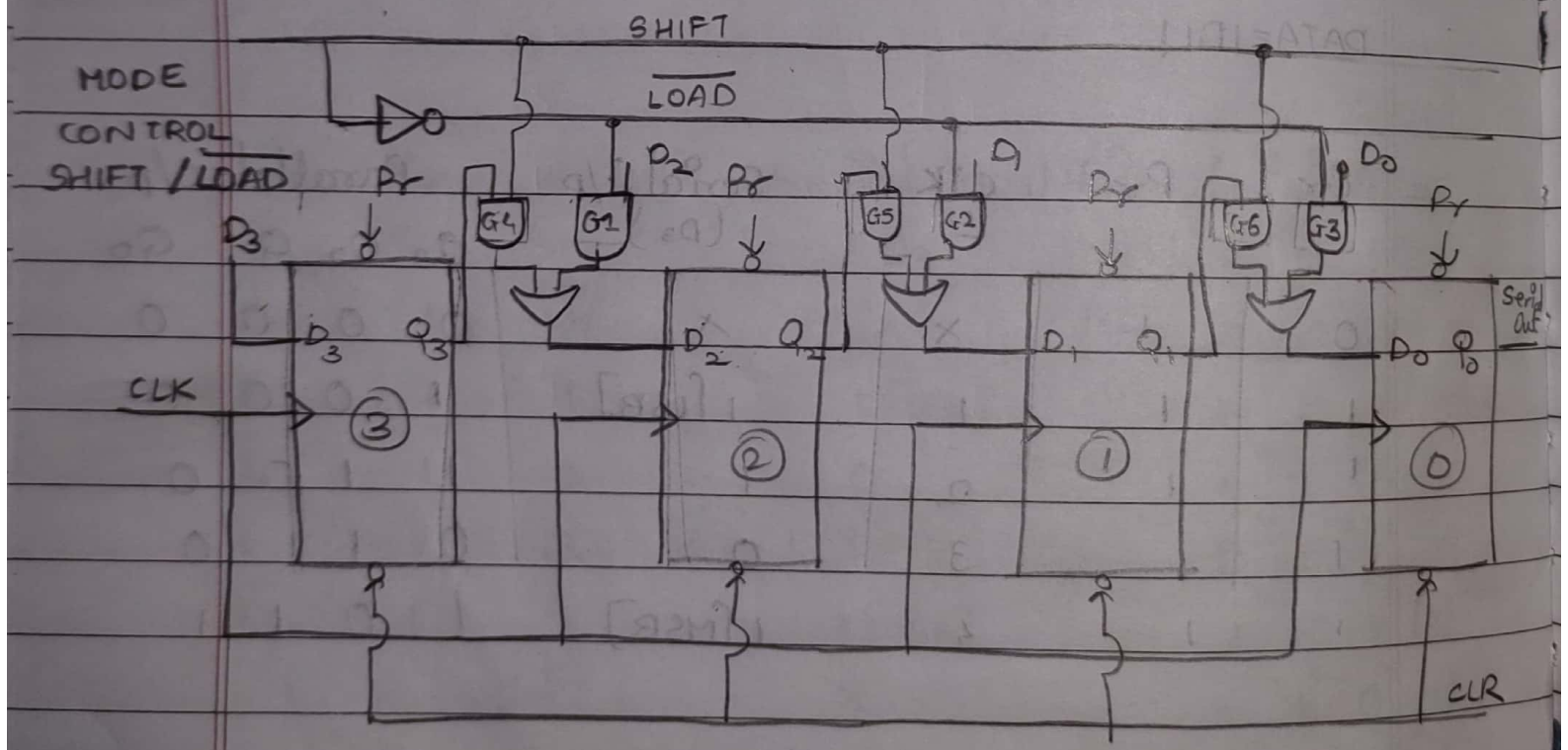
Cr	Pr	CLK	Serial i/p (D_3)	Parallel o/p Q_3 Q_2 Q_1 Q_0
0	1	x	x	0 0 0 0
1	1	1	1 [LSB]	1 0 0 0
1	1	2	1	1 1 0 0
1	1	3	0	0 1 1 0
1	1	4	1 [MSB]	1 0 1 1

• PIPO

Cr	Pr	CLK	Parallel i/p D_3 D_2 D_1 D_0	Parallel o/p Q_3 Q_2 Q_1 Q_0
0	1	x	x x x x	0 0 0 0 (clear)
1	1	1	1 0 1 1	1 0 1 1



- PISO



Inputs							Outputs				
P_r	C_r	CLK	D_3	D_2	D_1	D_0	Q_3	Q_2	Q_1	Q_0	
1	0	x	x	x	x	x	0	0	0	0	(clear)
1	1	1	1	1	0	1	1	1	0	1	LSB

* MODE 0

CLR → 2

MODE							
	1	x	x	x	x	x 1 1	0
	3	x	x	x	x	x x 1	1
	4	x	x	x	x	x x x	1

MSB

APPLICATION OF SHIFT REGISTER

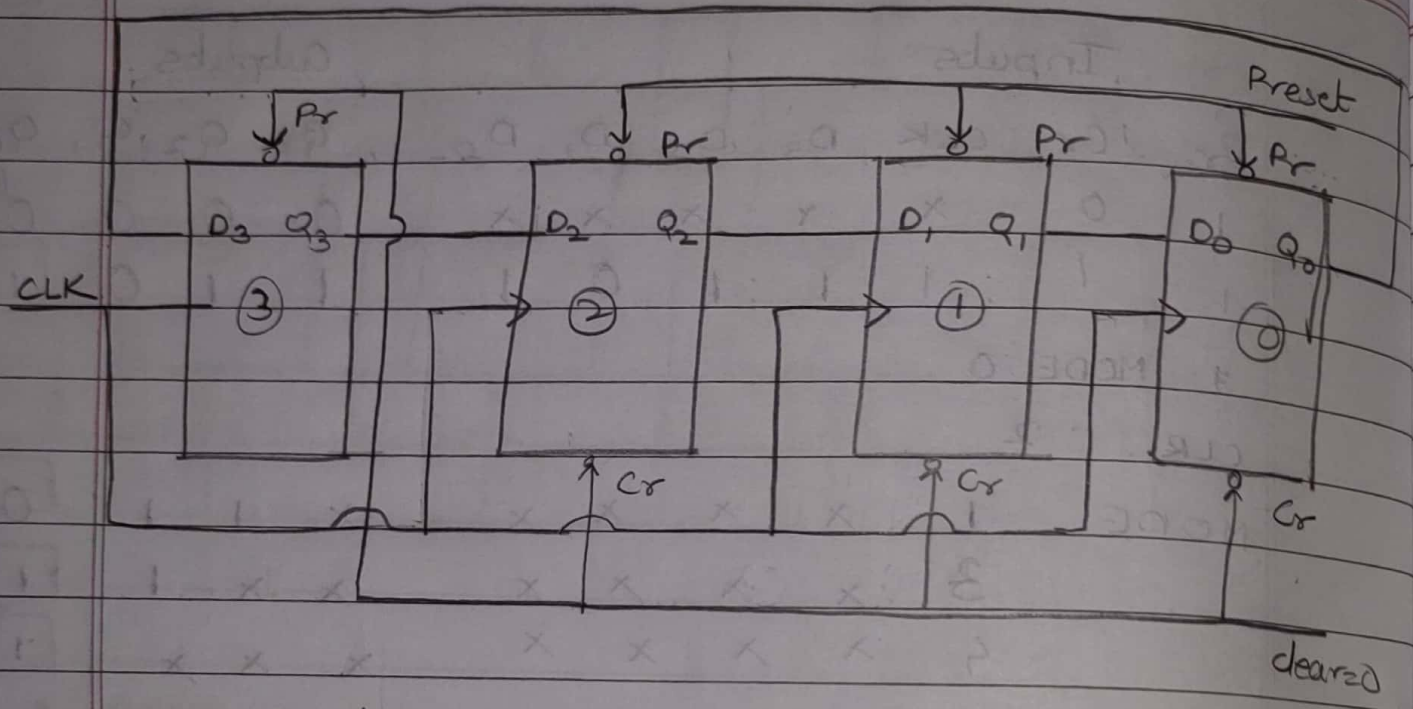
1. SISO : Delay $\Delta t = N \times \frac{1}{f_c}$

where N = No of stages

f_c = clock frequency

2. SIPO : serial to parallel converter
3. PISO : Parallel to serial converter
4. Ring counter
5. Johnson counter

4-bit Ring Counter



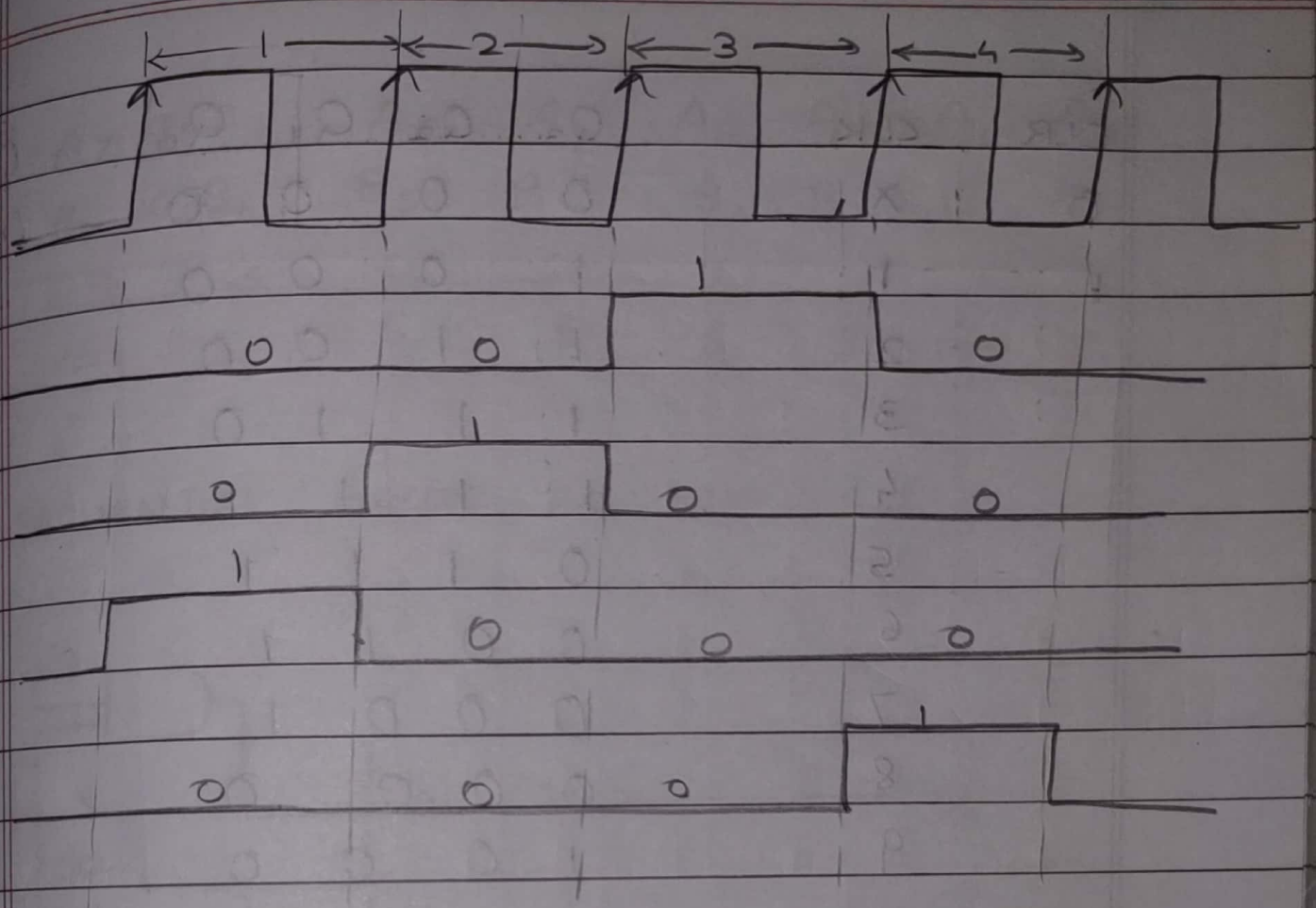
Inputs

CLR	CLK
0	X
1	1
	2
	3
	4

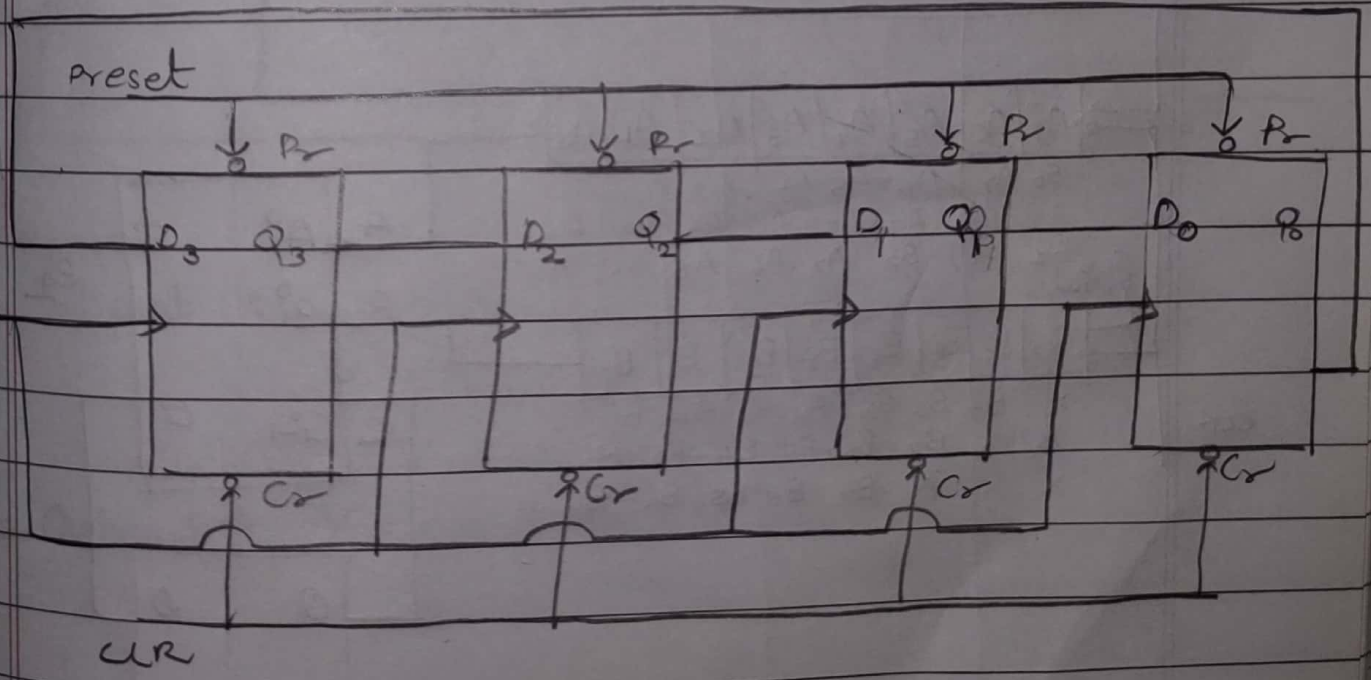
Outputs

Q_3	Q_2	Q_1	Q_0
1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1
1	0	0	0

Timing diagram / output waveform

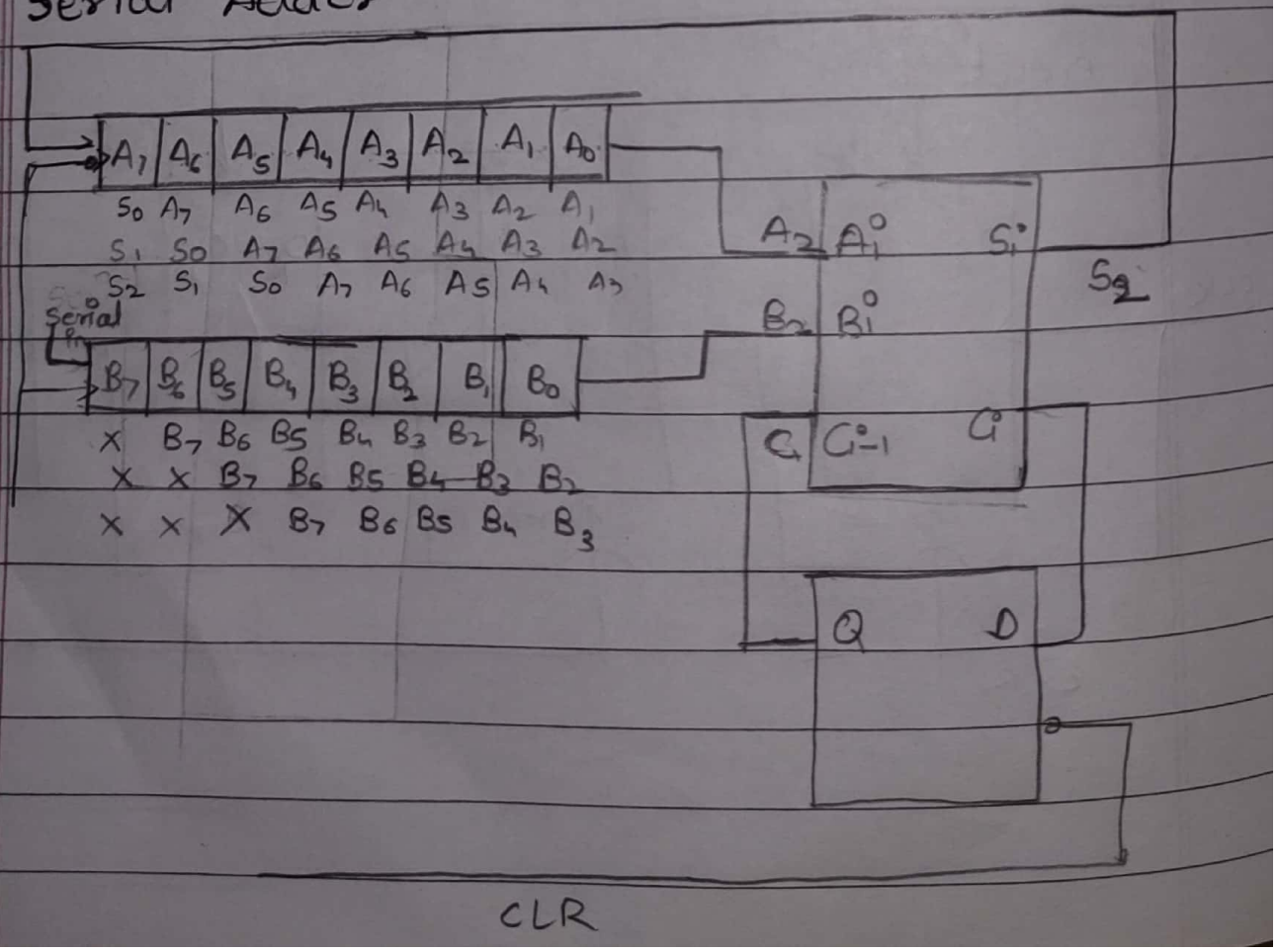


Johnson Counter



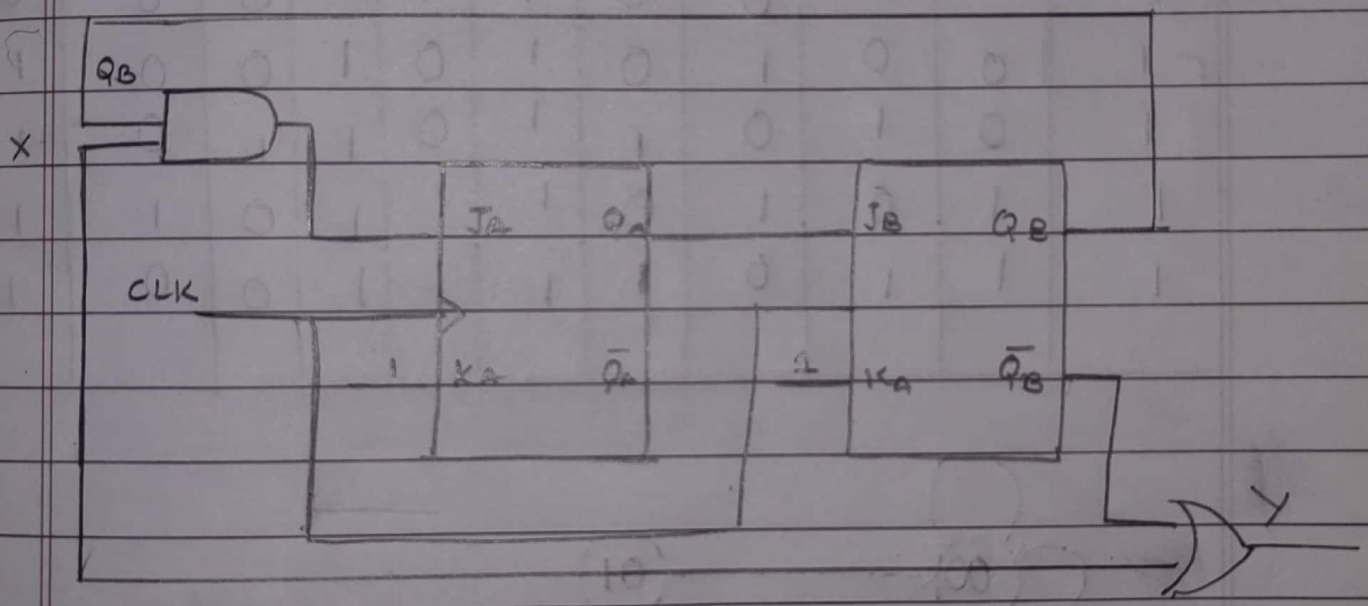
CLR	CLK	Q_3	Q_2	Q_1	Q_0	$\overline{Q_0}$
		0	0	0	0	(clear)
0	X	1	0	0	0	1
↓	1	1	1	0	0	
	2	1	1	1	0	
	3	1	1	1	1	
	4	0	1	1	1	
	5	0	0	1	1	
	6	0	0	0	1	
	7	0	0	0	0	
	8	0	0	0	0	
	9	1	0	0	0	

Serial Adder



A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

SEQUENTIAL CIRCUIT ANALYSIS



Input : $J_A = X$. $J_B = Q_A$

$K_A = 1$ $K_B = 1$

Output : $Y = (X + \overline{Q_B})$

Input	Present State			Flip-flop input				Next State		Output
X	Q_A	Q_B	$\overline{Q}_B$	J_A	K_A	J_B	K_B	Q_A^+	Q_B^+	y
0	0	0	1	0	1	0	1	0	0	1
0	0	1	0	0	1	0	1	0	0	0
0	1	0	1	0	1	1	1	0	1	1
0	1	1	0	0	1	1	1	0	0	0
1	0	0	1	0	1	0	1	0	0	1
1	0	1	0	1	1	0	1	1	0	1
1	1	0	1	0	1	1	1	0	1	1
1	1	1	0	1	1	1	1	0	0	1