

UNIT- 4

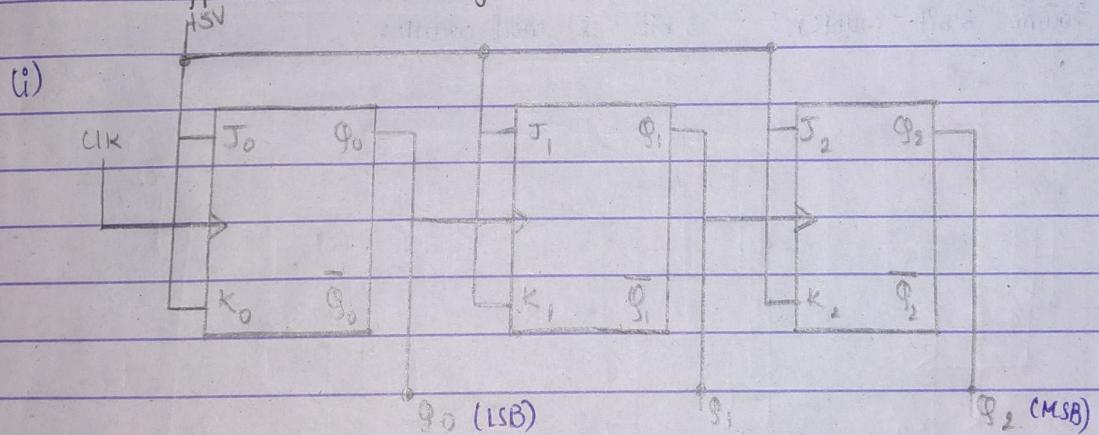
-° COUNTERS :-

Asynchronous Counter / Ripple counters:-

When the output of a flip flop is used as the clock input for next flip flop we call the counter ripple counter / asynchronous counter.

- A binary ripple counter can be constructed using clocked JK flip flop. JK flip flop connected in cascade, The system clock, a square wave drives flip flop Q_0 , the output of Q_0 drives flip flop Q_1 , and output of Q_1 drives flip flop Q_2 .
- JK inputs are connected to $+V_{cc}$
This means each flip flop will change its state (toggle) with a negative transition at its clock input.

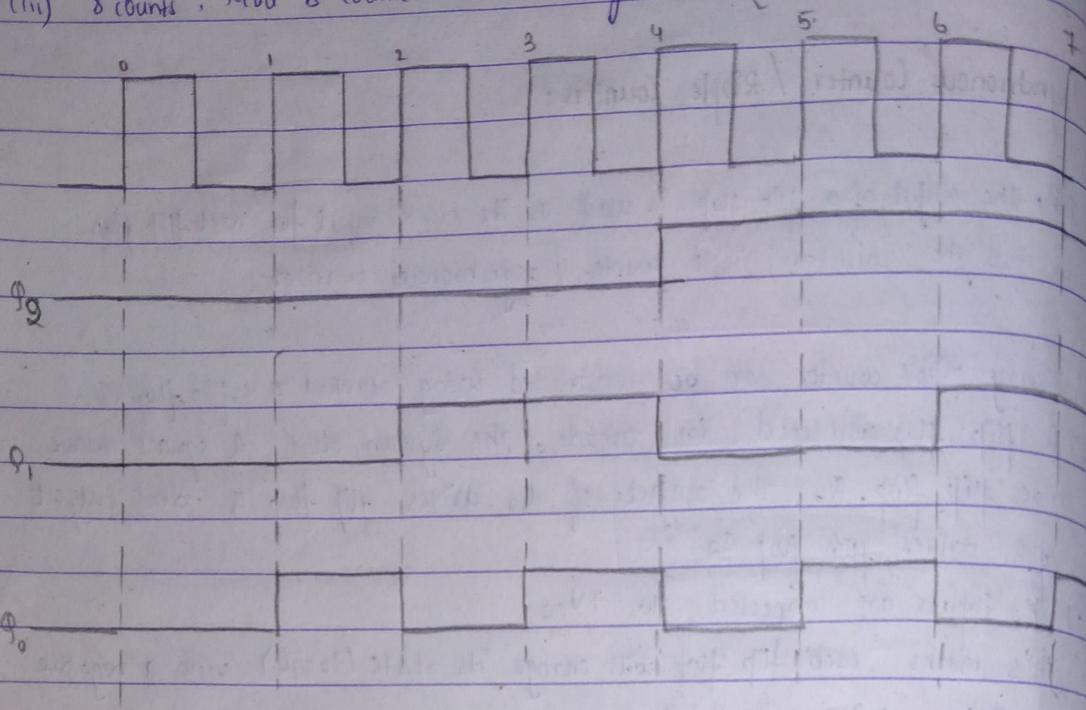
3 bit ripple counter :- (Asynchronous UP counter)



(ii)

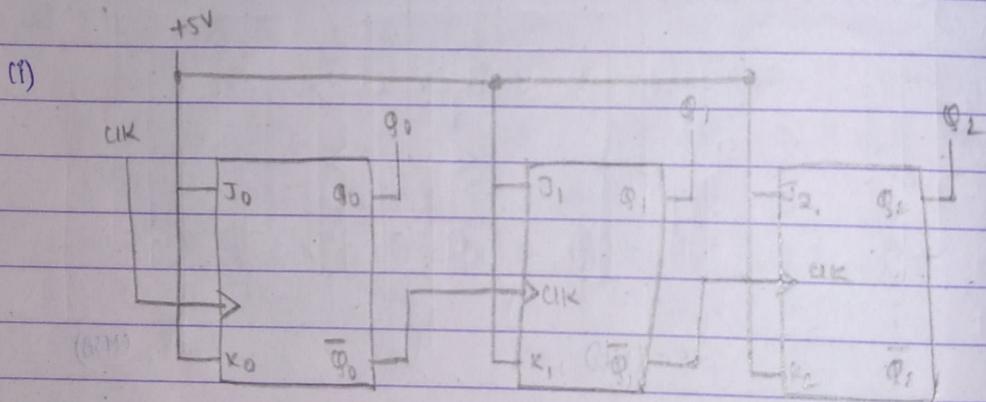
	CLK	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	1	
2	0	1	0	
3	0	1	1	
4	1	0	0	
5	1	0	1	
6	1	1	0	
7	1	1	1	

(iii) 8 counts : Mod 8 counter (clock diagram)



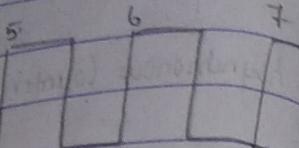
Asynchronous down counter / Ripple down counter.

Down 3 bit counter :- 3 bit 8 mod counter.



(ii)	UK	Q_2	Q_1	Q_0
0	1	1	1	
1	1	1	0	
2	1	0	1	
3	1	0	0	
4	0	1	1	
5	0	1	0	
6	0	0	1	
7	0	0	0	

(iii)



SYNCHRONOUS COUNTER:-

Mod 8 up synchronous counter using JK FF's.

→ (i) Current state			Next state			\bar{J}_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
0	0	1	0	1	X	0	0	X	1	X	
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

$Q_n \rightarrow Q_{n+1}$	\bar{J}	K
0 \rightarrow 0	0	X
0 \rightarrow 1	X	X
1 \rightarrow 0	X	1
1 \rightarrow 1	X	0

(ii) For J_2 :-

		Q ₁ Q ₂	00	01	11	10
		0	0	X	X	0
		1	0	X	X	1

$$J_2 = Q_0 \bar{Q}_1$$

For K_2 :-

		Q ₁ Q ₂	00	01	11	10
		0	X	0	0	X
		1	X	0	1	X

$$K_2 = Q_0 \bar{Q}_1$$

For J_1 :-

		Q ₁ Q ₂	00	01	11	10
		0	0	0	X	X
		1	1	1	X	X

$$J_1 = Q_0$$

For K_1 :-

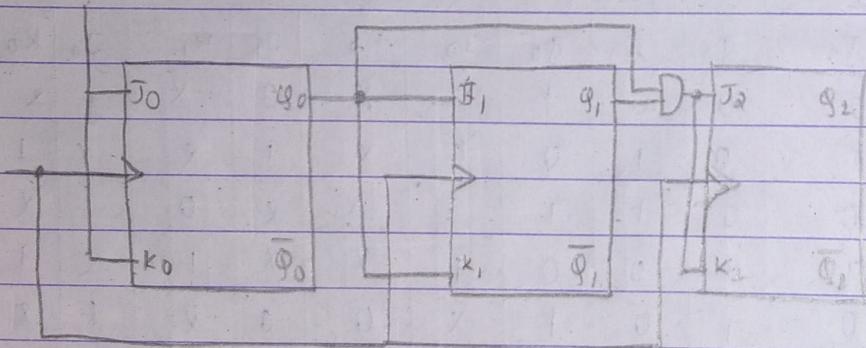
		Q ₁ Q ₂	00	01	11	10
		0	X	X	0	0
		1	X	X	1	1

$$K_1 = \bar{Q}_0$$

$$J_0 = 1 \quad K_0 = 1$$

(iii) Circuit Diagram :-

+5V (V_{CC})



	CK	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	1	
2	0	1	0	
3	0	1	1	
4	1	0	0	
5	1	0	1	

1. NAND gate is connected to output of Q_2 and Q_0 and set to zero.

SYNCHRONOUS COUNTERS :-

All flip-flops are clocked simultaneously.

Design a synchronous mod-8 up counter using JK FF

Current state			Next state			J ₂ K ₂	J ₁ K ₁	J ₀ K ₀
(MSB) Q ₂	Q ₁	Q ₀ ^(LSB)	Q ₂	Q ₁	Q ₀			
0	0	0	0	0	1	0 X	0 X	1 X
0	0	1	0	1	0	0 X	1 X	X 1
0	1	0	0	1	1	0 X	X 0	1 X
0	1	1	1	0	0	1 X	X 1	X 1
1	0	0	1	0	1	X 0	0 X	1 X
1	0	1	1	1	0	X 0	1 X	X 1
1	1	0	1	1	1	X 0	X 0	1 X
1	1	1	0	0	0	X 1	X 1	X 1

K-map for J₂

$Q_2 \backslash Q_0$		00	01	11	10
0	0	0	1	0	
1	X	X	X	X	

$$J_2 = Q_1 Q_0$$

K-map for K₀

$Q_2 \backslash Q_0$		00	01	11	10
0	0	X	X	X	X
1	X	0	0	1	0

$$K_0 = Q_1 Q_0$$

K-map for J₁

$Q_2 \backslash Q_0$		00	01	11	10
0	X	X	L	0	
1	X	X	1	0	

$$J_1 = Q_0$$

K-map for K₁

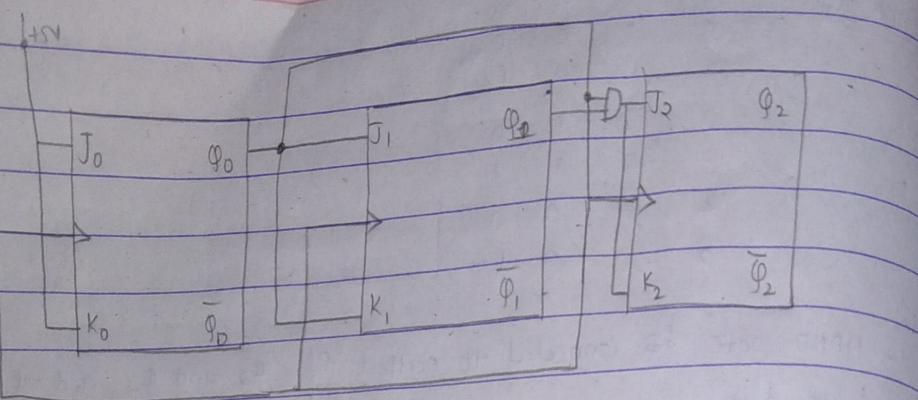
$Q_2 \backslash Q_0$		00	01	11	10
0	X	X	L	0	
1	X	X	1	0	

$$K_1 = Q_0$$

K-map for J₀ and K₀

$$J_0 = 1$$

$$K_0 = 1$$



2) 4-bit synchronous up counter using JK FF

→ Current state Next state

$Q_3\ Q_2\ Q_1\ Q_0$	$Q_3\ Q_2\ Q_1\ Q_0$	$J_3\ K_3$	$J_2\ K_2$	$J_1\ K_1$	$J_0\ K_0$
0 0 0 0	0 0 0 1	0 X	0 X	0 X	1 X
0 0 0 1	0 0 1 0	0 X	0 X	1 X	X 1
0 0 1 0	0 0 1 1	0 X	0 X	X 0	1 X
0 0 1 1	0 1 0 0	0 X	1 X	X 1	X 1
0 1 0 0	0 1 0 1	0 X	X 0	0 X	1 X
0 1 0 1	0 1 1 0	0 X	X 0	1 X	X 1
0 1 1 0	0 1 1 1	0 X	X 0	X 0	1 X
0 1 1 1	1 0 0 0	1 X	X 1	X 1	X 1
1 0 0 0	1 0 0 1	X 0	0 X	0 X	1 X
1 0 0 1	1 0 1 0	X 0	0 X	1 X	X 1
1 0 1 0	1 0 1 1	X 0	0 X	X 0	1 X
1 0 1 1	1 1 0 0	X 0	1 X	X 1	X 1
1 1 0 0	1 1 0 1	X 0	X 0	0 X	1 X
1 1 0 1	1 1 1 0	X 0	X 0	1 X	X 1
1 1 1 0	1 1 1 1	X 0	X 0	X 0	1 X
1 1 1 1	0 0 0 0	X 1	X 1	X 1	X 1

K-map for J_3

$Q_3\ Q_2\ Q_1\ Q_0$	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

K-map for K_3

$Q_3\ Q_2\ Q_1\ Q_0$	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	0	1	0
10	0	0	0	0

$$J_3 = Q_2 Q_1 Q_0$$

$$K_3 = Q_2 Q_1$$

K-map for J_2

		$Q_3 Q_2 \backslash Q_1 Q_0$				$Q_3 Q_2 \backslash Q_1 Q_0$				$Q_3 Q_2 \backslash Q_1 Q_0$			
		00	01	11	10	00	01	11	10	00	01	11	10
00	0	0	1	0	00	X	X	X	00	0	1	X	X
01	X	X	X	X	01	0	0	1	01	0	1	X	X
11	X	X	X	X	11	0	0	1	0	11	0	1	X
10	0	0	1	0	10	X	X	X	10	0	1	X	X

$$J_2 = Q_1 Q_0$$

K-map for K_2

		$Q_3 Q_2 \backslash Q_1 Q_0$				$Q_3 Q_2 \backslash Q_1 Q_0$				$Q_3 Q_2 \backslash Q_1 Q_0$			
		00	01	11	10	00	01	11	10	00	01	11	10
00	0	0	1	0	00	X	X	X	00	0	1	X	X
01	X	X	X	X	01	0	0	1	0	01	0	1	X
11	X	X	X	X	11	0	0	1	0	11	0	1	X
10	0	0	1	0	10	X	X	X	10	0	1	X	X

$$K_2 = Q_1 Q_0$$

K-map for J_1

		$Q_3 Q_2 \backslash Q_1 Q_0$				$Q_3 Q_2 \backslash Q_1 Q_0$				$Q_3 Q_2 \backslash Q_1 Q_0$			
		00	01	11	10	00	01	11	10	00	01	11	10
00	0	0	1	0	00	X	X	X	00	0	1	X	X
01	X	X	1	0	01	0	0	1	0	01	0	1	X
11	X	X	1	0	11	0	0	1	0	11	0	1	X
10	0	0	1	0	10	X	X	X	10	0	1	X	X

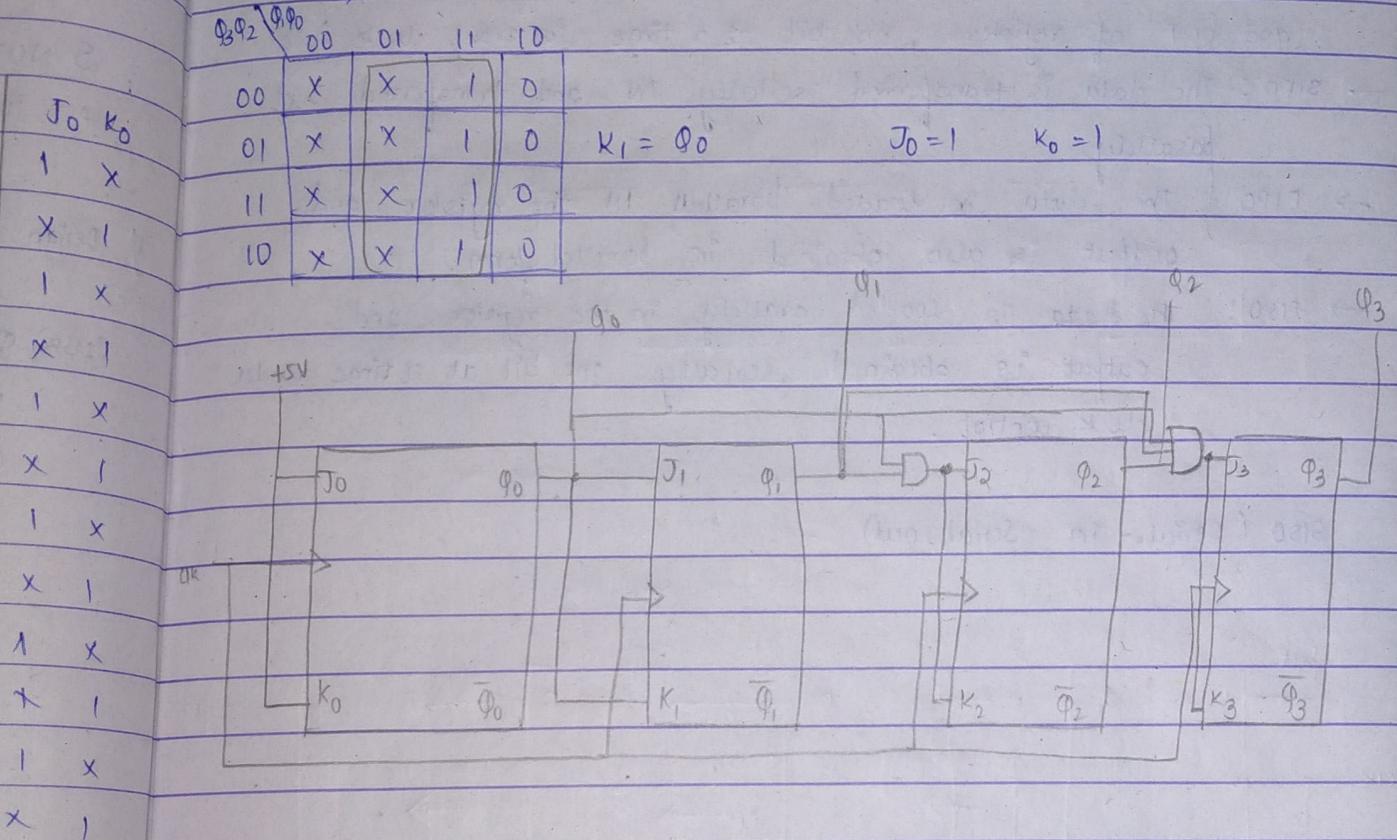
$$J_1 = Q_0$$

3b

		$Q_3 Q_2 \backslash Q_1 Q_0$				$Q_3 Q_2 \backslash Q_1 Q_0$				$Q_3 Q_2 \backslash Q_1 Q_0$			
		00	01	11	10	00	01	11	10	00	01	11	10
00	X	X	1	0	00	X	X	X	00	X	X	X	X
01	X	X	1	0	01	0	0	1	0	01	0	1	X
11	X	X	1	0	11	0	0	1	0	11	0	1	X
10	0	0	1	0	10	X	X	X	10	0	1	X	X

$$K_1 = Q_0$$

$$J_0 = 1 \quad K_0 = 1$$



In synchronous down, same as asynchronous down, start from last count in current state, next procedure remains same.

If mod-6 or mod-10 or mod-5 any such counters are given then write count till $(n-1)$

In K-map rest (remaining) places are considered as X

If lock-in condition is which then in current state consider test number also and in next state write 0 for them and solve K-map.

$$= Q_2 Q_1 Q_0$$

REGISTERS

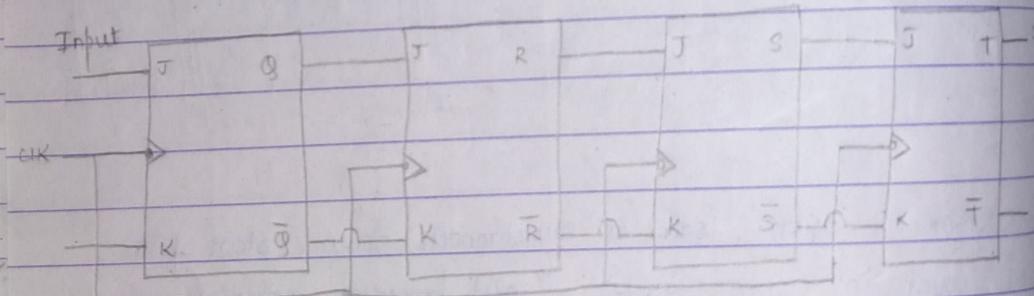
Shift registers are the sequential logic circuits that are used for storing or transferring data in the form of binary numbers.

The data is transferred to the output for every clock cycle (one bit). Hence called shift registers.

Four different types of shift registers :-

- SISO (serial - in serial - out) :- The data is transferred serially and OUT of registers, one bit at a time for every clock cycle.
- SIPO :- The data is transferred serially IN and transferred out parallel.
- PIPO :- The data is loaded parallelly IN the register and output is also obtained in parallel form.
- PISO :- The data is loaded parallelly in the register and output is obtained serially one bit at a time under clock control.

SISO (serial - in Serial out) :-



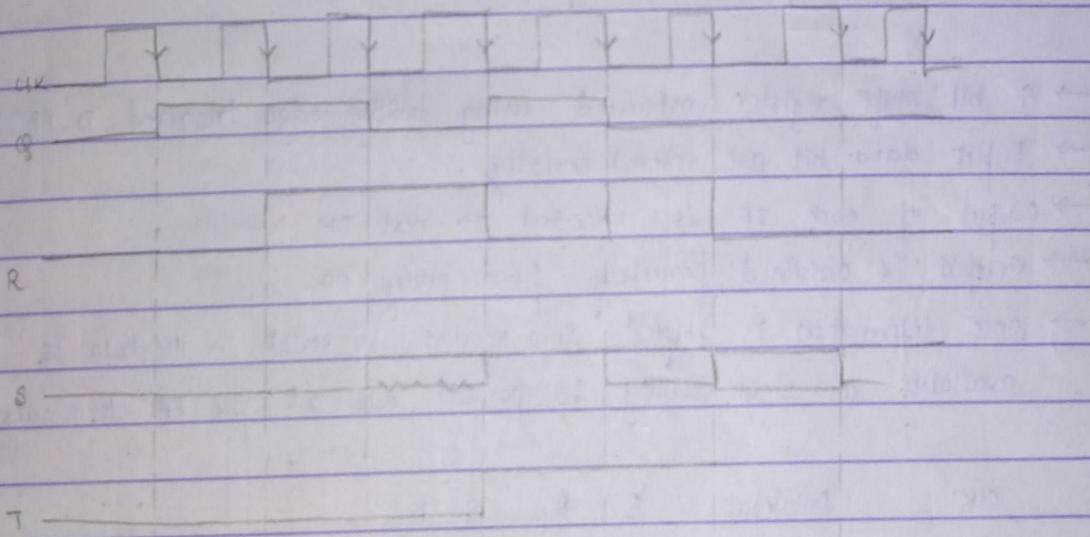
- 4 bit shift registers is constructed using JK flip flop. (negative edge triggered)
- The output of first flip flop is given to next flip flop.
- upon occurrence of negative edge on the clock, the content of each flip flop is shifted by one position to right
- The content of leftmost FF depends on signal value on serial data and content of rightmost FF is lost.

- It needs 4 clock pulse for 4 bit transfer.
- Output is transferred on to the last FF ie serial output.

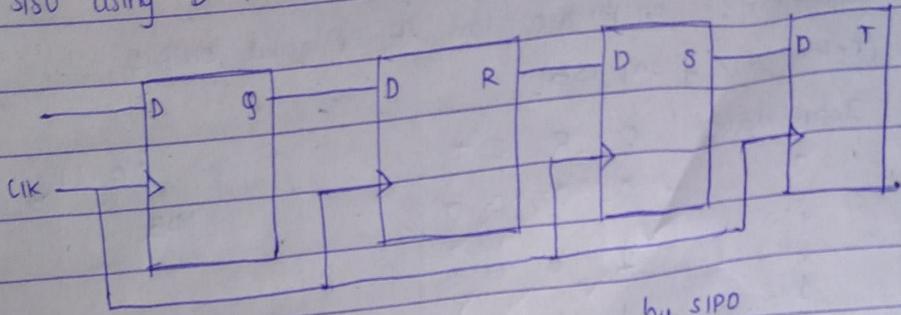
Input 1011 (enter data from LSB)

CK	Input-data	Q	R	S	T	
Initial	0	0	0	0	0	
↓	1	1	0	0	0	
↓	1	1	1	0	0	
↓	0	0	1	1	0	
↓	1	1	0	1	1	(LSB)
↓	0	0	1	0	1	
↓	0	0	0	1	0	
↓	0	0	0	0	1	(MSB)

CLK Diagram :-



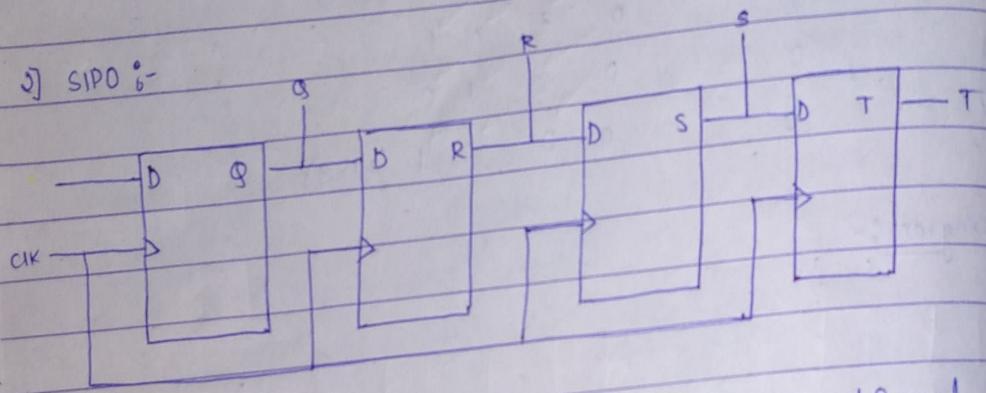
SISO using D FF



Disadvantage of SISO can be overcome by SIPO

where we don't need additional $n-1$ clock to get output.

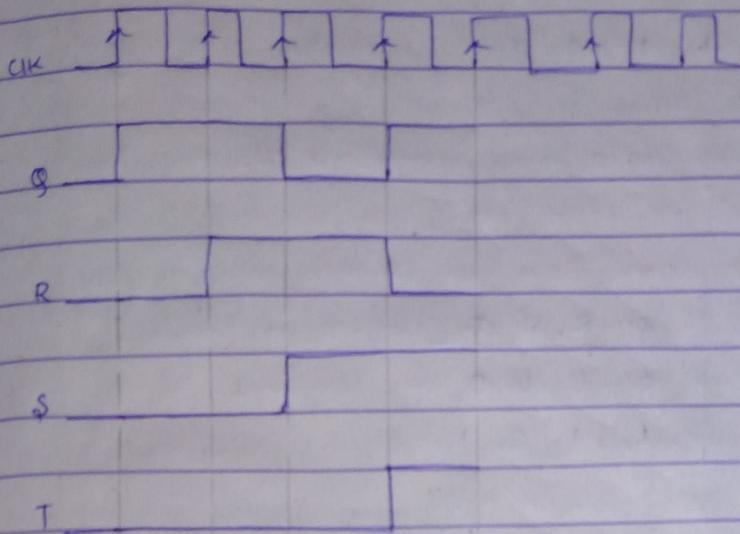
5] SIPO :-



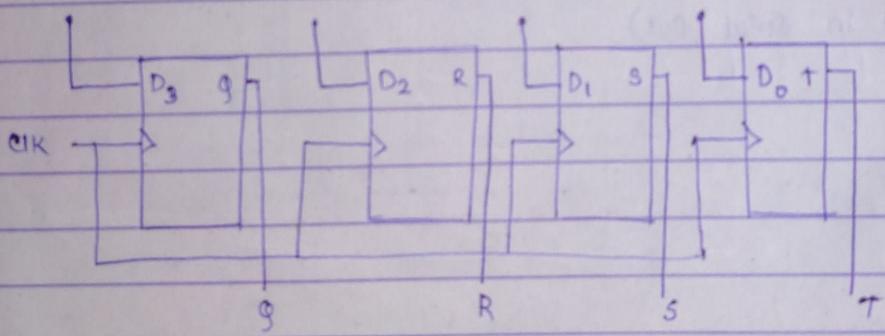
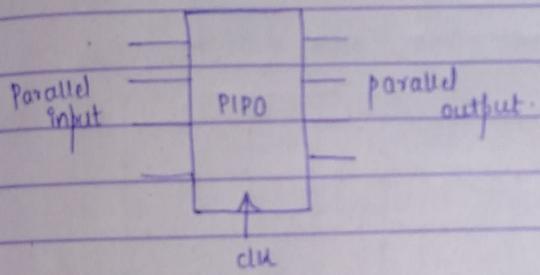
- 4 bit shift register constructed using positive edge triggered D FF
- Input data bits are entered serially
- Output of each FF is connected to next FF
- Output is obtained parallelly from every FF
- Once information is shifted into registers ie serial in the data is available as single entity ie parallel out at the FF terminal

CLK	Data Input	Q	R	S	T	
Initially	0	0	0	0	0	
↑	1	1	0	0	0	1011 → MSB
↑	1	1	1	0	0	
↑	0	0	1	1	0	
↑	1	1	0	1	1	

CLK Diagram :-



3) PIPD :- /Storage register /Buffer register.



→ 4-bit shift register is constructed using positive edge triggered D flip flop.

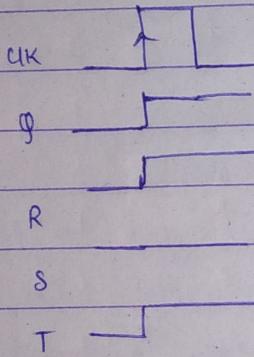
→ Input is given parallelly to each FF

→ Output is also obtained in parallel form from each flip flop in same clock pulse

CLK	data input	Q	R	S	T
X Initially	0	0 0 0 0			
↑	1	1 1 0 1			
↑	1				
↑	0				
↑	1] X				

CLK	D ₃	D ₂	D ₁	D ₀	Q	R	S	T
Initially	0	0	0	0	0	0	0	0
↑	1	1	0	1	1	1	0	1

Clock diagram :-



f) PISO (Parallel in Serial Out)

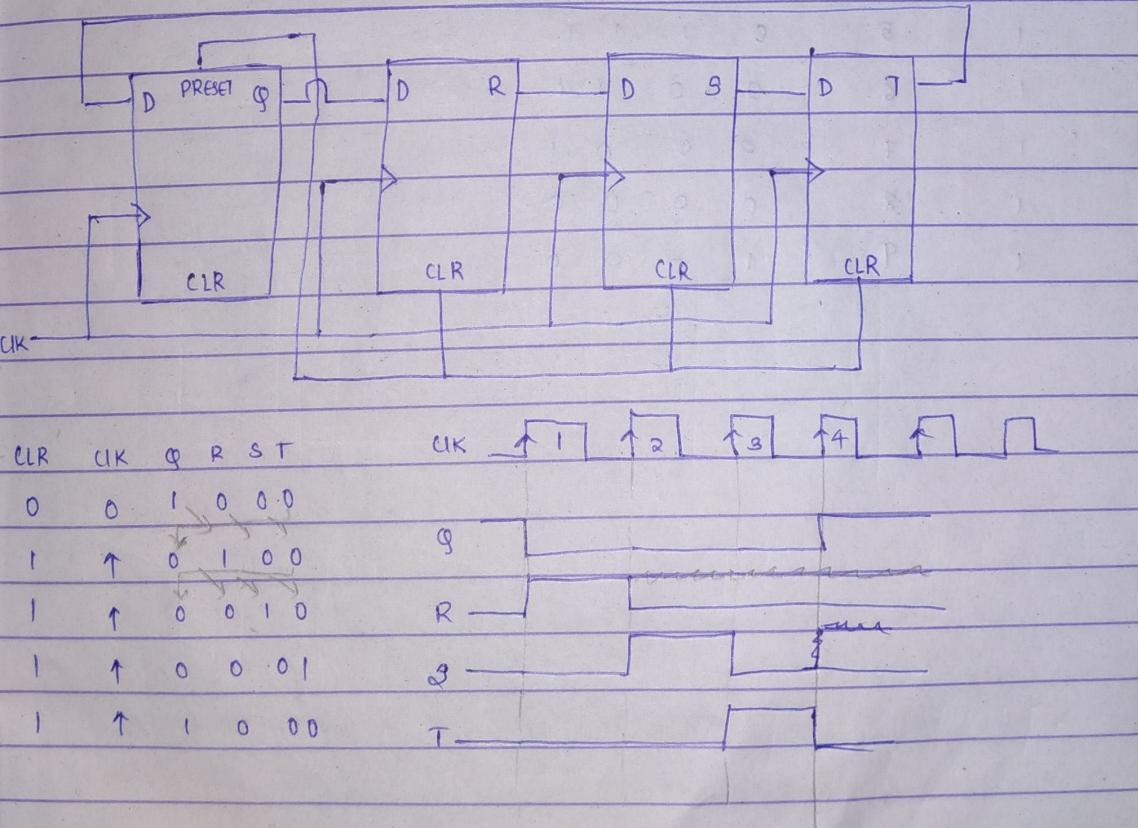
APPLICATION OF SHIFT REGISTERS :-

The ring counter and Johnson counter.

They are basically shift registers whose serial outputs are connected back to the serial input in order to get a particular sequence.

The ring Counter :-

- A ring counter is basically a circulating shift register in which the output is connected back to input at first stage
- 4-bit ring counter constructed using D flip flop.
- The output of each stage is shifted to next stage for every positive trigger at the clock pulse
- If the CLEAR is high, all the FF's are reset to 0, except the first one which is set to 1
- After 4 clock pulse, again the sequence repeats hence ring counter.

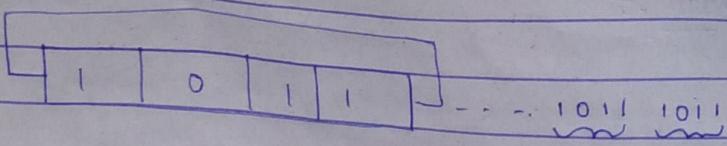


Johnson Counter :-

- 4 bit Johnson counter is constructed using a negative edge triggered FF.
- Instead of non-inverting output being connected to first FF, inverting output is connected to serial-in.
- Initially all FF are cleared. Then all FF have input as zero except first because it gets complement of 0 as input.
- During the next clock pulse again the complement is applied to serial-in. ∴ if initially it was 1000 next cycle will be 1100.

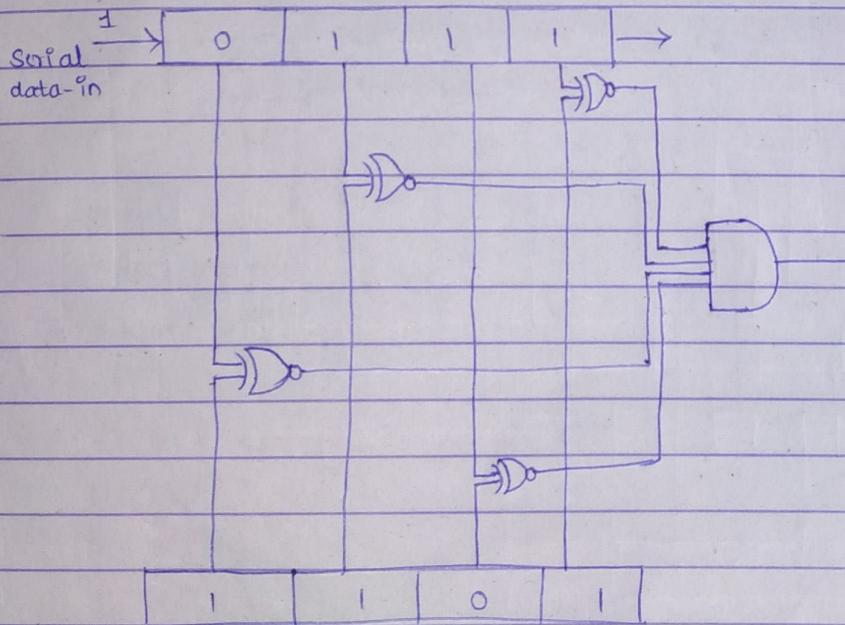
CLR	CIK	ϕ	R	S	T
0	0	0	0	0	0
1	1	1	0	0	0
1	2	1	1	0	0
1	3	1	1	1	0
1	4	1	1	1	1
1	5	0	1	1	1
1	6	0	0	1	1
1	7	0	0	0	1
1	8	0	0	0	0
1	9	1	0	0	0

SEQUENCE GENERATOR :-



- Sequence generator is useful for generating a sequence pattern repetitively.
- The basic block diagram of shift register where sequence generator is presented as pipe full of data and each FF as compartments in it.
- The leftmost FF is serial - data - in
- The rightmost FF is connected to serial - data - out.
- The clock is applied and data transfers only during a clock trigger.
- The shift register is applied like a ring counter, when a trigger occurs the serial - data - in / binary word stored comes out serially but it is not lost, instead fed back to the first FF

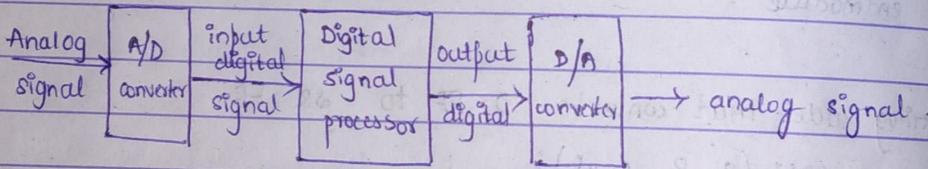
Sequence detector :-



Circuit - data to detect 1101 from given input data stream

Analog to digital converter:

- Most of the information carrying signals such as voltage, charge, current, temperature time are all in analog form.
 - But for data processing, storage, transmission, it is better that signal is in digital form.
 - When expressed in digital form they provide better accuracy and reduce noise.
 - The development in the microprocessor technology has made it compulsory for the data to be in digital form.
 - Since microprocessing uses binary zeroes and ones, it is important to convert analog signal to digital using A/D converter.
- Once the signal is measured it is
- (i) compared with set value and determine the control signal in the process control system
 - (ii) Generate the desired output by processing the signal.

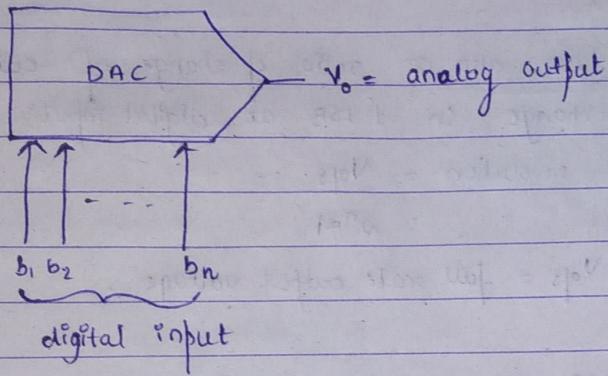


Basic elements of digital signal processing

- Most of the data is analog in nature. This has to be converted to digital form using A/D converter.
- Thus the A/D converter generates an array of samples and gives it to the digital signal processor. This array of sample is equivalent form of analog signal hence called digital.
- Digital signal processor performs signal processing operations like filtering, multiplication, amplification, transformation etc over the digital signal and generates another digital signal as its output.
- Digital signal processor
Eg.: High speed digital computer

Digital to analog converter :-

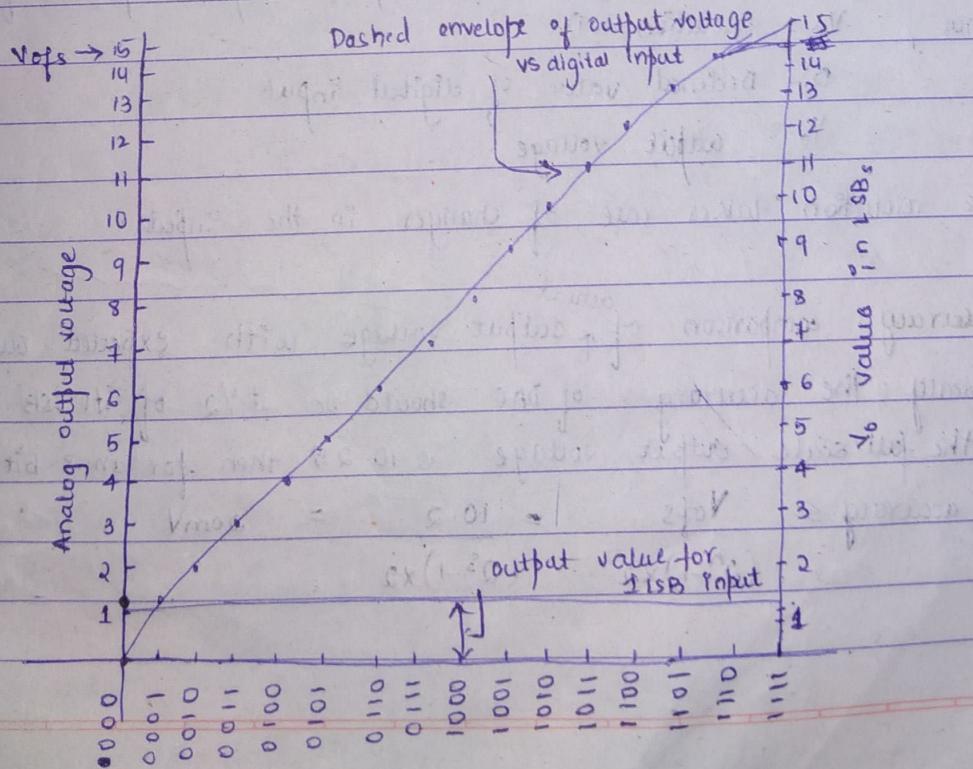
A DAC (digital to analog converter) accepts a n -bit input word $b_1, b_2 \dots b_n$ in binary and produce analog output proportional to it.



DAC circuit symbol

For 4-bit binary input :-

- 4-digital inputs, indicating 4-bit DAC. Each digital input requires a electrical signal representing a logic 1 or logic 0
- b_n is least significant bit (LSB)
- b_1 is MSB



Performance parameters of DAC :-

1) Resolution:- is the number of different analog output values that can be provided by DAC

Hence for n bit DAC

$$\text{resolution} = 2^n$$

Resolution can also be ratio of change of output voltages resulting from a change in 1 LSB at digital input.

$$\therefore \text{resolution} = \frac{V_{ofs}}{2^n - 1}$$

$$V_{ofs} = \text{full scale output voltage}$$

For an 8 bit DAC resolution can be given by

$$\text{resolution} = 2^8 = 256$$

If full scale output voltage is 10.2V then by second definition the resolution for an 8-bit DAC can be

$$\text{resolution} = \frac{10.2}{2^8 - 1} = 40 \text{ mV/LSB}$$

→ From resolution we can obtain the input - output equation for DAC

$$\text{Thus, } V_o = \text{resolution} \times D$$

D = Decimal value of digital input

V_o = output voltage

The resolution takes care of changes in the input.

2) Accuracy: comparison of ^{actual} output voltage with expected output.

Ideally the accuracy of DAC should be $\pm \frac{1}{2}$ of its LSB. If the full scale output voltage is 10.2V then for an 8-bit DAC

$$\text{accuracy} = \frac{V_{ofs}}{(2^n - 1) \times 2} = \frac{10.2}{(2^8 - 1) \times 2} = 20 \text{ mV}$$

Problems:

i) An 8-bit DAC has an output voltage range of 0 - 2.55V.

Define its resolution in two diff ways

$$\rightarrow i) n = 8 \text{-bit}$$

$$\text{Resolution} = 2^n = 2^8 = 256$$

$$ii) V_{ofs} = 2.55V$$

$$\text{resolution} = \frac{V_{ofs}}{2^{n-1}} = \frac{2.55}{2^8-1} = 10mV/\text{LSB}$$

Thus an input change of 1 LSB, causes an output change by 10mV.

2] The digital input for a 4-bit DAC is 0110. Calculate its final output voltage.

$$\rightarrow \text{Input} = 0110 = 6 = D$$

$$V_o = \text{resolution} \times D = 15 \times 6 = 90$$

$$\text{Resolution} = 2^n = 2^4 = 16$$

$$\therefore V_{ofs} = 15V$$

$$\text{resolution} = \frac{15}{2^4-1} = \frac{15}{15} = 1mV/\text{LSB}$$

$$V_o = 1 \times 6 = 6V$$

Binary equivalent weight:

In general, the binary equivalent weight assigned to the LSB is

$$\text{LSB weight} = \frac{1}{2^{n-1}}$$

where n is no of bits.

The remaining weights are found by multiplying 2, 4, 8 and so on

if Find binary equivalent of each bit in 4-bit system

$$\rightarrow \text{LSB weight} = \frac{1}{2^{n-1}} = \frac{1}{2^4-1} = \frac{1}{15} = 1mV$$

$$2^{\text{nd}} \text{ LSB} = \frac{1 \times 2}{15} = \frac{2}{15}$$

$$3^{\text{rd}} \text{ LSB} = \frac{1}{15} \times 4 = \frac{4}{15}$$

$$4^{\text{th}} \text{ LSB} = \frac{3}{15}$$

$$\frac{1}{15} + \frac{2}{15} + \frac{4}{15} + \frac{8}{15} = \frac{15}{15} = 1$$

\rightarrow	Bit	Weight	Bit	Weight	
	2^0	$1/7$		2^0	$1/15$
	2^1	$2/7$		2^1	$2/15$
	2^2	$4/7$		2^2	$4/15$
	Sum	$1/7$		2^3	$8/15$
	3-bit binary equivalent weight		sum	$15/15$	
			4-bit binary equivalent weight		

Resistive divider :- To convert digital input to equivalent analog

Millman's theorem :- States that voltage appearing at any node in a resistive network is equal summation of currents entering the node divided by the summation of conductances connected to node.

Example :- For a 5-bit resistive divider. Determine the following

- The weight assigned to LSB
- Weight assigned to 2nd LSB and 3rd LSB
- Change in output voltage due to change in LSB, 2nd LSB and 3rd LSB
- Output voltage for a digital input 10101

assume $0 = 0V$ $1 = 10V$

$$\rightarrow a) \text{ LSB weight} = \frac{1}{31} = \frac{1}{2^{5-1}} = \frac{1}{31}$$

$$b) \text{ 2nd LSB} = \frac{2}{31} \quad \text{3rd LSB} = \frac{4}{31}$$

$$c) \text{ change in output voltage due to change in LSB} = \frac{10}{31} V \quad \text{in 2nd LSB} = \frac{20}{31} V$$

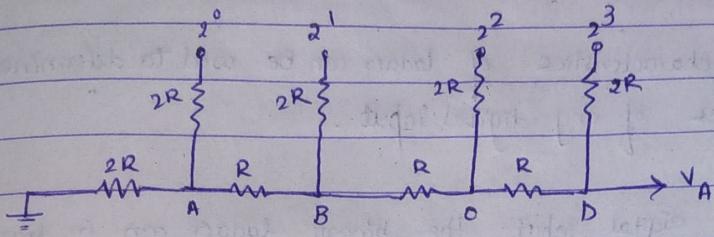
$$d) V_A = 10 \times 2^0 + 0 \times 2^1 + 10 \times 2^2 + 0 \times 2^3 + 10 \times 2^4$$

$$= \frac{010}{31} = 6.77V$$

R-2R ladder digital to analog converter (Voltage switched)

A binary ladder is a resistive network whose output voltages are weighted sum of all ^{digital} input.

A 4-bit binary ladder is constructed as shown:



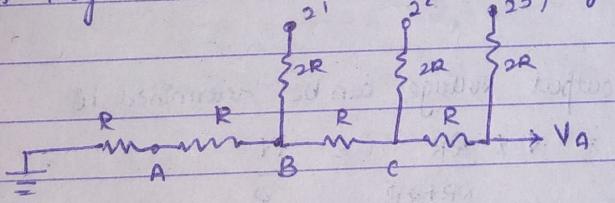
→ The ladder is constructed with resistors of two different values to overcome objective of resistive divider.

→ The left end of the ladder is terminated with resistor $2R$ and right end is open circuited.

→ Examining the resistive properties of the network.

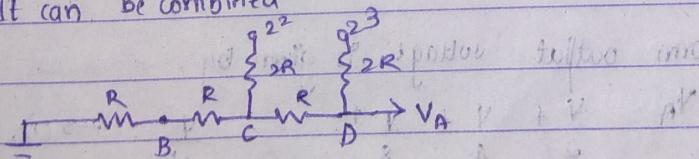
i) All digital inputs are grounded. The node A has a total resistance looking into the terminating resistor is $2R$. The total resistance looking out toward 2^0 input is also $2R$.

Thus they can be combined to simplify the circuit.

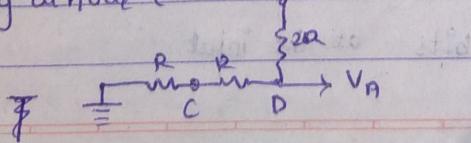


ii) At node B, the total resistance looking into the branch towards the node A is $2R$ and also the resistance at 2^1 input

∴ It can be combined



(iii) Similarly at node C

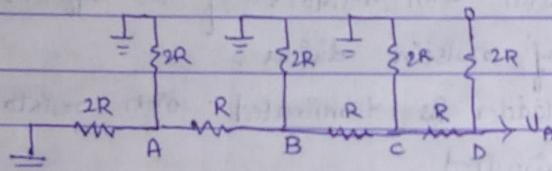


(Q) From this equivalent circuit, it is clear that the resistance looking back towards node C is $2R$ and same at 2^3 input.

→ To summarise, the total resistance looking back from any node back to the terminating resistor or towards digital input is $2^3 R$. This is regardless of whether the digital inputs are grounded or +V.

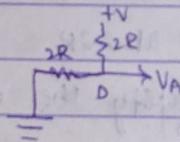
→ The resistance characteristics of ladder can be used to determine the output voltage of any digital input.

Eg:- With various digital input the binary ladder can be drawn as shown. Input = 1000



Since there are no voltage sources to the left of node D.

All the network toward the left of this node can be replaced by $\frac{+V}{2}$ to form equivalent circuit.



From this the output voltage can be determined i.e

$$V_A = \frac{V}{2} \times \frac{R}{2R + R} = \frac{V}{6}$$

Thus at 1 at MSB will also give output voltage at $+V/2$

→ In equation form output voltage is given by

$$V_A = \frac{V}{2^n}$$

$$= \frac{V}{2} + \frac{V}{4} + \frac{V}{8} + \dots + \frac{V}{2^n} \quad \rightarrow (1)$$

where n is no of bits at the input

(i) can be simplified

$$V_A = V_0 2^0 + V_1 2^1 + V_2 2^2 + \dots + V_{n-1} 2^{n-1}$$

Bit position	Binary weight	Output voltage
MSB	V_2	$V/2$
2nd MSB	$V/4$	$V/4$
3rd MSB	$V/8$	$V/8$
1		
1		
n^{th} MSB	$V/2^n$	$V/2^n$

Problems:

i) what are the output voltages caused by each bit in a 5-bit ladder
if the input levels are $0 = 0V$ and $1V = 10V$.

$$\rightarrow \text{First MSB } V_A = \frac{V}{2} = \frac{10}{2} = 5V$$

$$\text{2nd MSB } V_A = \frac{V}{4} = \frac{10}{4} = 2.5V$$

$$\text{3rd MSB } V_A = \frac{V}{8} = \frac{10}{8} = 1.25V$$

$$\text{4th MSB } V_A = \frac{V}{16} = \frac{10}{16} = 0.625V$$

$$\text{5th } V_A = \frac{V}{32} = \frac{10}{32} = 0.3125V$$

ii) Find the output voltage from a 5-bit ladder that has a digital input of 1010 . Assume that $0 = 0V$ and $1 = +10V$

$$\rightarrow V_A = V_0 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3 + V_4 2^4$$

$$= 10 \times 2^0 + 0 \times 2^1 + 0 \times 2^2 + 10 \times 2^3 + 10 \times 2^4$$

$$= \frac{10(1+2^1+2^3+2^4)}{32} = \frac{10 \times 26}{32} = +8.125V$$

what is full scale output voltage of 5-bit ladder in eg (a)

$$V = 5 + 0.5 + 1.25 + 0.625 + 0.3125 = 9.6875V$$

It is simply sum of individual bit voltages.

Analog to digital converter - Simultaneous conversion :-

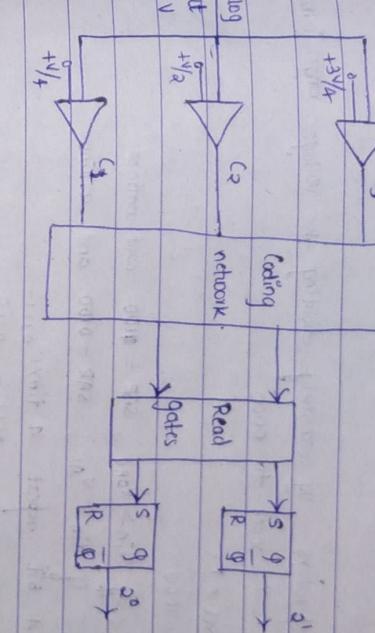
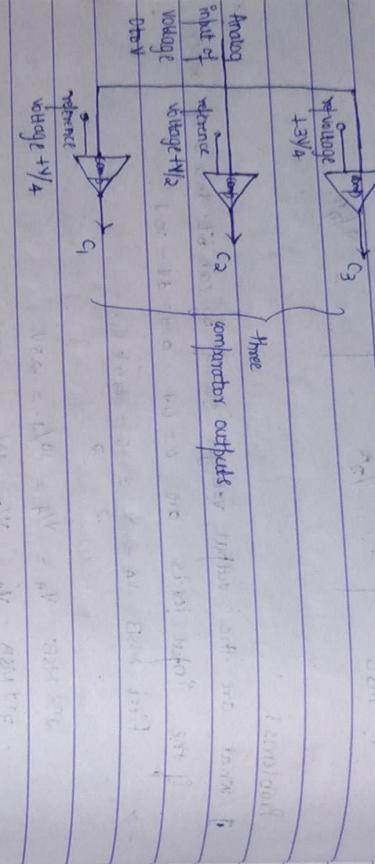
The process of converting an analog input voltage into its equivalent digital output is called A/D converter.

A/D conversion is more complicated than D/A.

A/D conversion is the most simplest way to do it.

Simultaneous conversion makes use of 3 comparator circuits for

A/D conversion.



\rightarrow The analog input is connected to each comparator as an input.

\rightarrow The other input to the comparator are reference voltages. The reference voltages are +V/4, +V/2, +3V/4

\rightarrow The analog input voltage ranges from 0 to V volts.

\rightarrow If the analog voltage exceeds the reference voltage then

comparator turns ON

\rightarrow If all the comparators are OFF then the analog input must be

between 0 to +V/4

\rightarrow These comparators output are specified in the below table for diff analog inputs.

\rightarrow There can be 4 ranges of output for the above converter.

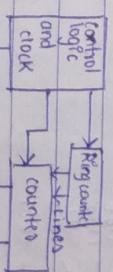
\rightarrow The comparator output are then sent to coding network to get 3-bit equivalent of analog input.

\rightarrow Then it is stored in flip flop registers.

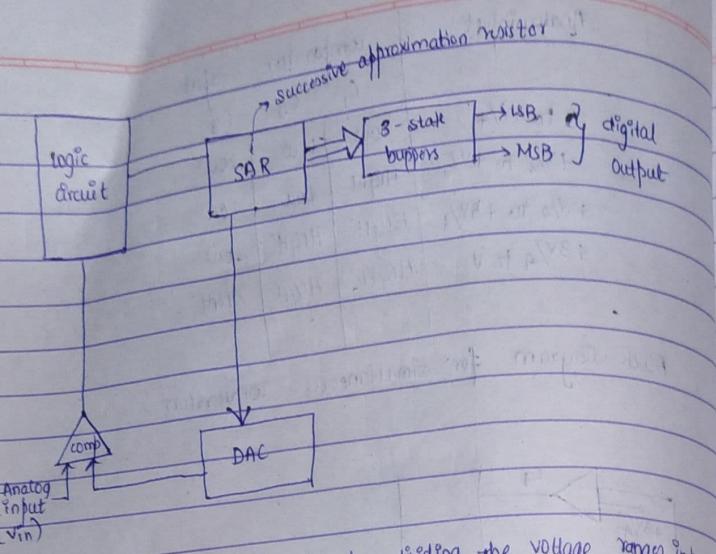
A/D - successive approximation :-

If multiplexing is required, then successive approximation is most useful.

Block diagram :-



digital output.



→ The converter operates by successively dividing the voltage range in half.

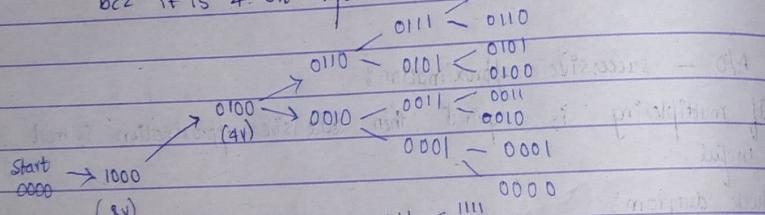
→ Initially counter is reset to 0000
then MSB is set = 1

Eg:- SAR = 1000

→ In next clock, If $V_{in} > V_{DAC}$, SAR = 0100 and continue

→ In next clock, If $V_{in} < V_{DAC}$, SAR = 0000 and continue

bcz it is 4-bit repeat 4 times 0111



Start
0000

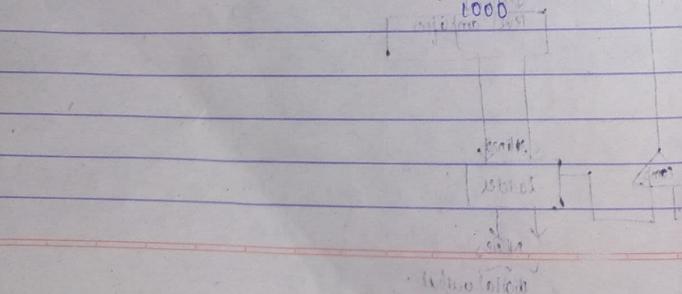
(8V)

1100 → 1110 ← 1101 ← 1100

1010 → 1011 ← 1011 ← 1010

1001 → 1000 ← 1001 ← 1000

1000 → 1000 ← 1000 ← 1000



→ The conversion operates by successively dividing the voltage range in half.

→ First the counter is reset to 0. The MSB is set to 1.

Then if the MSB should be kept or taken out is decided depending upon output of comparator

→ The 2nd MSB is set to 1. Then the comparison is made to decide whether second MSB should be reset.

→ Similar process is carried out down to the LSB. By this time the desired number is available on the counter

→ Since this process involves use of only one FF to convert starting with MSB, ring counter is used for FF selection.

→ Thus successive approximation is a process of approximating the analog voltage by trying 1 bit at a time beginning with MSB.

→ The above solution explains that time required for each conversion is the same.

→ Thus total conversion time is equal to the number of bits.

→ One conversion cycle mostly takes one clock cycle.

→ For eg:- a 10-bit converter operating with a 1-MHz clock has a conversion time of $10 \times 10^{-6} = 10^{-5}$

→ Other delays in the system like settling delay, multiplexer has to be considered.