

A circuit used for counting the pulses is known as counter. (8)

Basically there are two types of counters

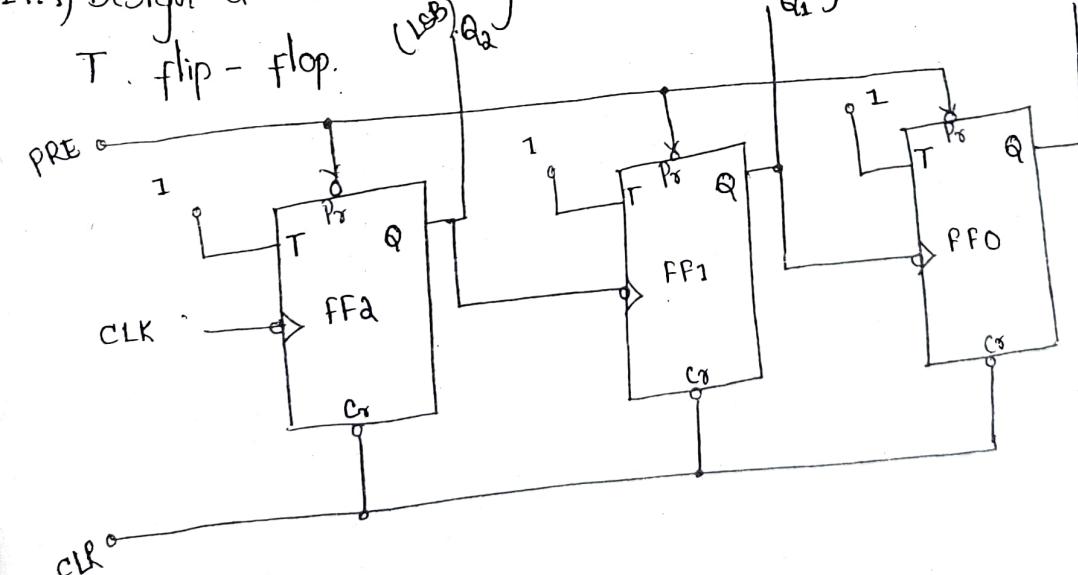
1. Asynchronous counter (Ripple counter)
2. Synchronous counter.

In asynchronous counter, all the flip-flops are not clocked simultaneously, whereas in synchronous counter all the flip-flops are clocked simultaneously.

A flip flop has two states, therefore a group of n flip-flop will have 2^n states

Ex: With 4 F/F we can obtain $2^4 = 16$ states

Ex: i) Design a 3-bit asynchronous binary up counter using T flip-flop.



Truth table:

Counter state

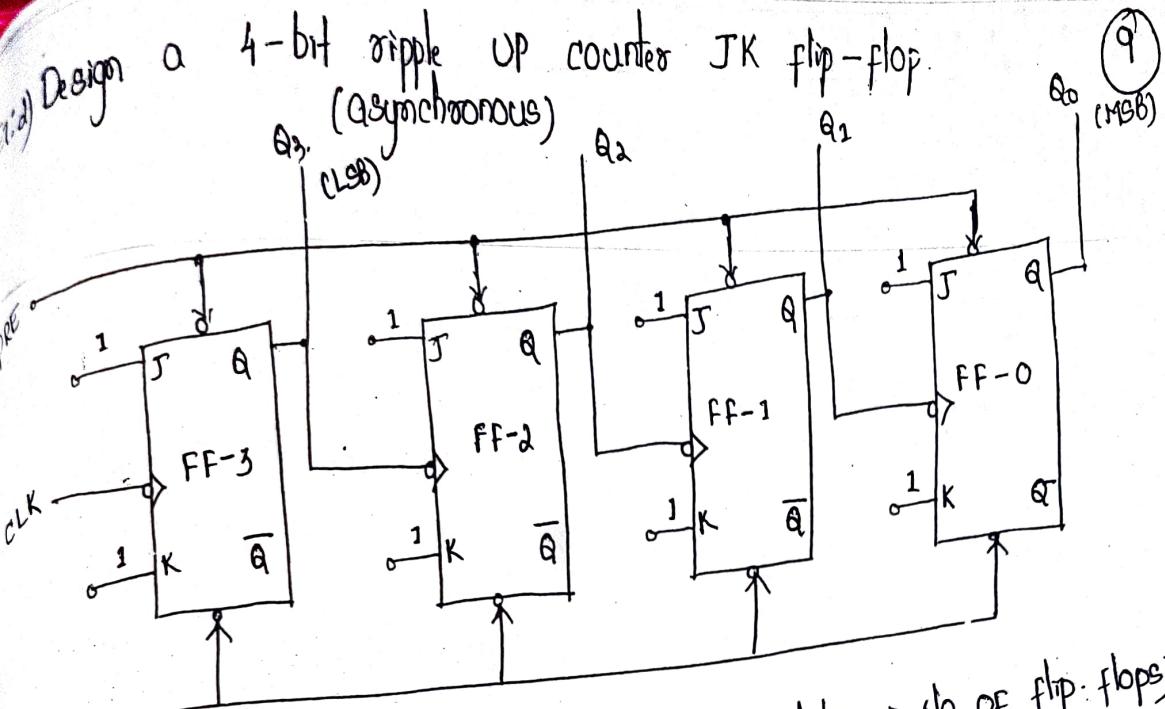
Counter state	Count		
	(LSB) Q_2	Q_1	(MSB) Q_0
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1
8	0	0	0

OR

Counter state

Counter state	Count		
	(MSB) Q_0	Q_1	(LSB) Q_2
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

(i) Design a 4-bit ripple up counter JK flip-flop.



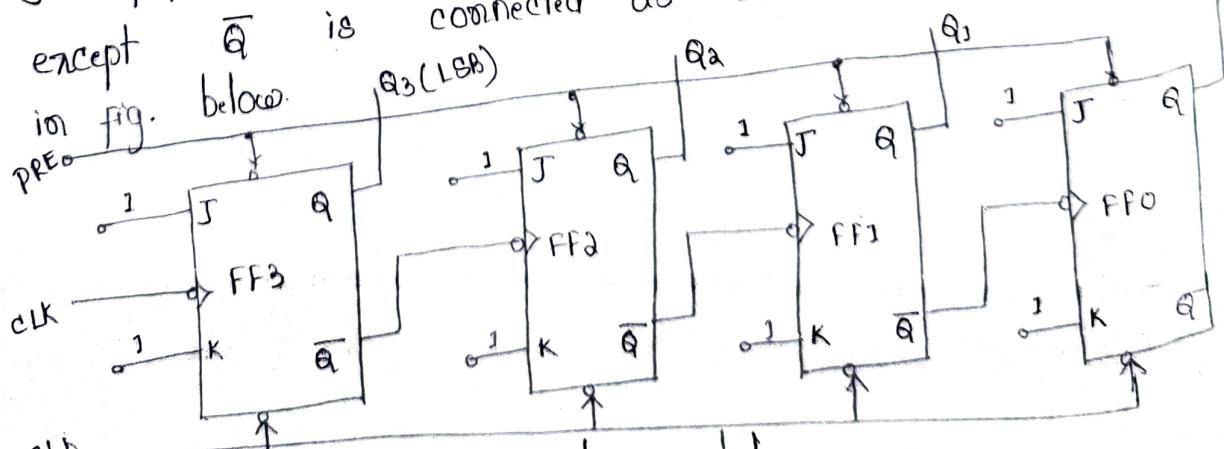
Truth table: $2^4 = 16$ states: $4 \rightarrow \text{No. of bits} \rightarrow \text{No. of flip-flops}$

clock pulse CLR

	Output			
	Q ₀	Q ₁	Q ₂	Q ₃
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	1	0	0	0
8	1	0	0	1
9	1	0	1	0
10	1	0	1	1
11	1	1	0	0
12	1	1	0	1
13	1	1	1	0
14	0	1	1	1
15	0	0	0	0
16	1	1	1	1

- CLK pulse (negative edge triggered) applied to the first flip flop only (FF₃) initially, using CLR input.
- All flip-flops are cleared initially, using CLR input.
- J and K inputs of all flip-flops are made '1' (Toggle condition). Also Q output of flipflops are given as CLK to next stage.
- When first clock pulse is, FF₃ toggles (0 to 1 transition), so no change in the state of FF₂, FF₁ and FFO.
- During second clock pulse, FF₃ again toggles (1 to 0 transition), so FF₂ changes its state from 0 to 1, but no change in FF₁ and FFO.
- FF₃ always toggles, FF₂ changes its state when FF₃ is changing its state from 0 to 1, FF₁ changes its state when FF₂ is changing its state from 0 to 1, FFO changes its state when FF₁ is changing its state from 0 to 1.
- During 15th clock pulse, we will obtain last state 1111.
- When 16th clock pulse is applied, it resets back to 0000.
- E2: 3) Design a 4-bit asynchronous DOWN counter using JK flip-flop.

Sol²: To design a 4-bit asynchronous DOWN counter using JK flip-flop, follow the same procedure of UP counter except \bar{Q} is connected as clock instead of Q as shown in fig. below.



→ Truth table is as shown below.

CLK pulse

CLR

Output
 $Q_0 \ Q_1 \ Q_2 \ Q_3$

(16)

0	0	0) 0) 0) 0)
1	1	1 1 1 0)
2	1	1 1 0 1)
3	1	1 1 0 0)
4	1	1 0 1 1)
5	1	1 0 1 0)
6	1	1 0 0 1)
7	1	1 0 0 0)
8	1	1 0 0 0)
9	1	0 1 1 1)
10	1	0 1 1 0)
11	1	0 1 0 1)
12	1	0 1 0 0)
13	1	0 0 1 1)
14	1	0 0 1 0)
15	1	0 0 0 1)
16	1	0 0 0 0)

→ Here the transition is considered from 0 to 1 because of \overline{Q} connected as clock

E1.3) Design MOD-5 counter (asynchronous counter) using JK flip-flops.

Soln: A MOD-N counter has only 'N' states i.e., 0 to $N-1$.

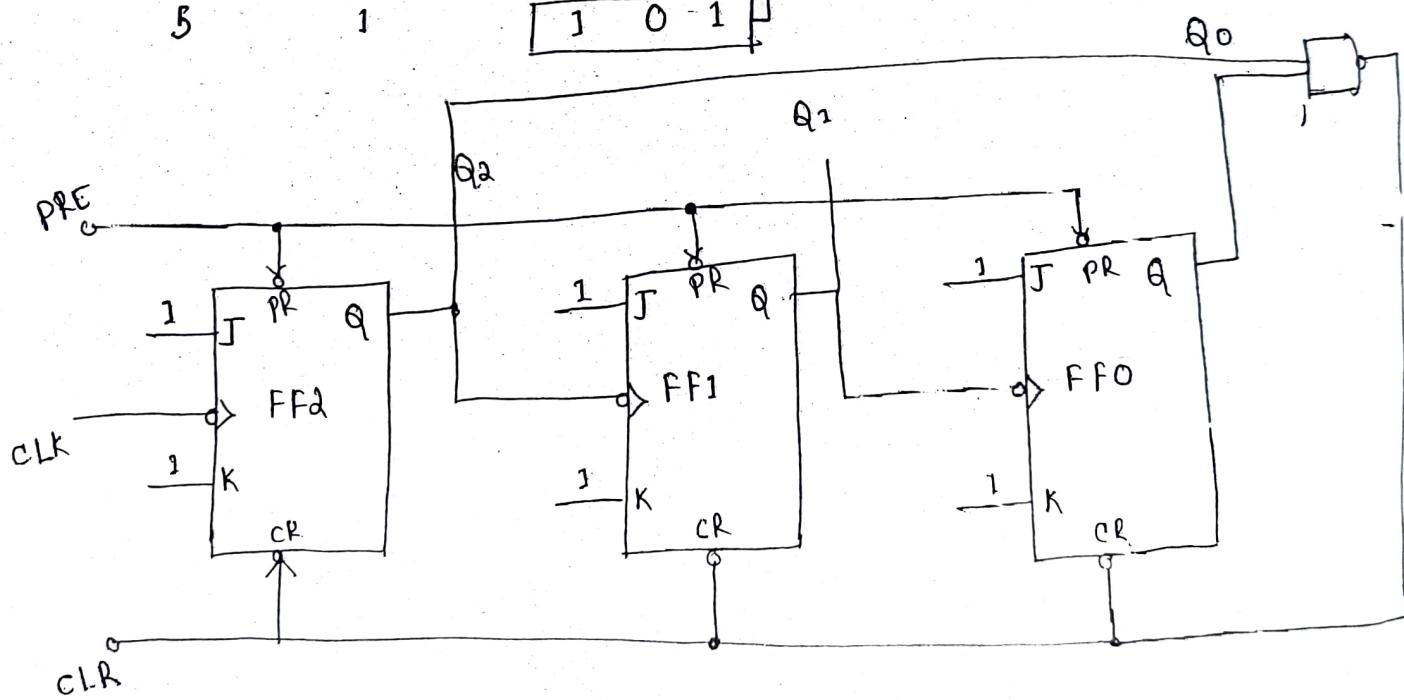
→ MOD-5 counter will count from 0 to 4.

→ No. of flip-flops required : $2^d = 4$ (0 to 3 only), not enough to generate 5 states (0 to 4)
so $2^3 = 8$; 3 flip-flops are required

→ $2^N \geq M$; here $M = 5$
 $\therefore N=3$; No. of flip-flops

→ Truth table of MOD-5 counter is as shown below

CLK	CLR	Outputs $Q_0 \ Q_1 \ Q_2$
0	0	0 0 0
1	1	0 0 1
2	1	0 1 0
3	1	0 1 1
4	1	1 0 0
5	1	1 0 1



→ When $Q_0 = 1$; $Q_2 = 1$; the sequence should be truncated and reset to 000 through NAND gate and clear input.

Design of Synchronous counters:

Design a 4-bit synchronous up counter using JK flip flop. (11)

In synchronous counters, all the flip-flops are clocked simultaneously.

The truth table for 4-bit synchronous counter is shown below.

CLK	Present State				Next State				Flip-flop inputs							
	Q_D	Q_C	Q_B	Q_A	Q_D^+	Q_C^+	Q_B^+	Q_A^+	J_D	K_D	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	0	0	0	1	0	x	0	x	0	x	1	x
1	0	0	0	1	0	0	1	0	0	x	0	x	1	x	x	1
2	0	0	1	0	0	0	1	1	0	x	0	x	x	0	1	x
3	0	0	1	1	0	1	0	0	x	1	x	x	1	x	1	x
4	0	1	0	0	0	1	0	1	0	x	x	0	0	x	1	x
5	0	1	0	1	0	1	1	0	0	x	x	0	1	x	x	1
6	0	1	1	0	0	1	1	1	0	x	x	0	x	0	1	x
7	0	1	1	1	1	0	0	0	1	x	x	1	x	1	x	1
8	1	0	0	0	1	0	0	1	x	0	0	x	0	x	1	x
9	1	0	0	1	1	0	1	0	x	0	0	x	1	x	x	1
10	1	0	1	0	1	0	1	x	0	0	x	x	0	1	x	1
11	1	0	1	1	1	1	0	0	x	0	1	x	x	1	x	1
12	1	1	0	0	1	1	0	1	x	0	x	0	0	x	1	x
13	1	1	0	1	1	1	1	0	x	0	x	0	1	x	x	1
14	1	1	1	0	1	1	1	1	x	0	x	0	x	0	1	x
15	1	1	1	1	0	0	0	0	x	1	x	1	x	1	x	1

Excitation table of JK flip-flop:

$Q_n \rightarrow Q_{n+1}$	J	K
0 , 0	0	x
0 , 1	1	x
1 , 0	x	1
1 , 1	x	0

→ Plot K-map for flip flop inputs

J _D		Q _A _B _C		Q _A _B _C		Q _A _B _C	
Q _A _B _C	J _D	00	01	11	10	00	01
00	0	0	0	0	0	0	0
01	0	0	0	(1)	0	X	X
11	X	X	(X)	X	X	X	X
10	X	X	X	X	X	X	X

$$\bar{J}_D = Q_C Q_B Q_A$$

J _C		Q _A _B _C		Q _A _B _C		Q _A _B _C	
Q _A _B _C	J _C	00	01	11	10	00	01
00	0	0	0	1	0	0	X
01	X	X	(X)	X	X	0	0
11	0	0	1	0	X	0	1
10	0	0	0	0	0	1	X

$$K_D = Q_C Q_B Q_A$$

$$J_C = Q_B Q_A$$

K _C		Q _A _B _C		Q _A _B _C		Q _A _B _C	
Q _A _B _C	K _C	00	01	11	10	00	01
00	X	X	X	X	X	X	X
01	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0
10	X	X	X	X	X	X	X

$$K_C = Q_B Q_A$$

J _B		Q _A _B _C		Q _A _B _C		Q _A _B _C	
Q _A _B _C	J _B	00	01	11	10	00	01
00	0	1	X	X	X	0	0
01	0	1	X	X	X	0	0
11	0	1	X	X	X	0	0
10	X	X	1	0	0	X	X

$$\bar{J}_B = Q_A$$

J _A		Q _A _B _C		Q _A _B _C		Q _A _B _C	
Q _A _B _C	J _A	00	01	11	10	00	01
00	1	X	X	1	0	0	0
01	1	X	X	1	0	0	0
11	1	X	X	1	0	0	0
10	1	X	X	1	0	0	0

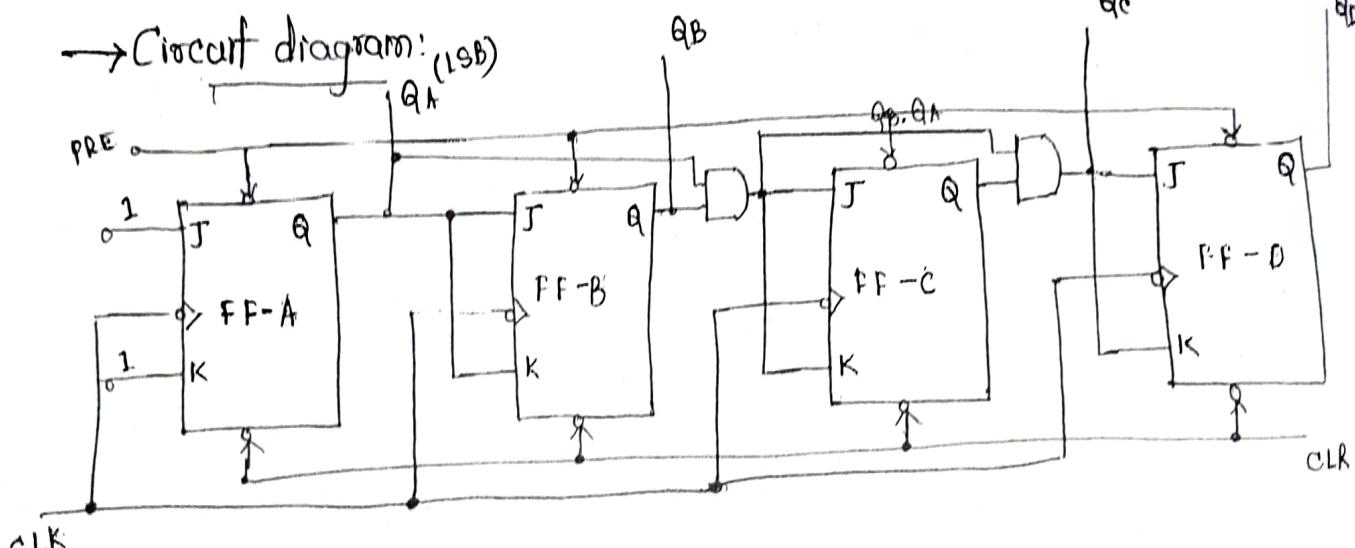
$$K_B = Q_A$$

J _A		Q _A _B _C		Q _A _B _C		Q _A _B _C	
Q _A _B _C	J _A	00	01	11	10	00	01
00	1	1	1	1	0	0	0
01	1	1	1	1	0	0	0
11	1	1	1	1	0	0	0
10	1	1	1	1	0	0	0

$$\bar{J}_A = 1$$

$$K_A = 1$$

→ Circuit diagram: (ISB)



Ex: d: Design a 4-bit synchronous down counter using JK flip-flop.

The truth table of 4-bit synchronous down counter using JK flip-flop is as shown below (12)

CLK	Present State				Next State				Flip-flop inputs							
	Q _D	Q _C	Q _B	Q _A	Q _D ⁺	Q _C ⁺	Q _B ⁺	Q _A ⁺	J _D	K _D	J _C	K _C	J _B	K _B	J _A	K _A
0	0	0	0	0	1	1	1	1	J	X	1	X	1	X	1	X
1	1	1	1	1	1	1	0	X	0	X	0	X	0	X	1	X
2	1	1	1	0	1	1	0	J	X	0	X	0	X	1	1	X
3	1	1	0	1	1	1	0	0	X	0	X	0	X	X	1	X
4	1	1	0	0	1	0	1	1	X	0	X	1	1	X	1	X
5	1	0	1	1	1	0	1	0	X	0	0	X	X	1	1	X
6	1	0	1	0	1	0	0	1	X	0	0	X	0	X	X	1
7	1	0	0	1	1	0	0	0	X	0	0	X	0	X	X	1
8	1	0	0	0	0	1	1	1	X	1	1	X	1	X	1	X
9	0	1	1	1	0	1	1	0	0	X	X	0	X	1	1	X
10	0	1	1	0	0	1	0	1	0	X	X	0	0	X	X	1
11	0	1	0	1	0	1	0	0	0	X	X	1	1	X	1	X
12	0	1	0	0	0	0	1	1	0	X	X	1	1	X	1	X
13	0	0	1	1	0	0	1	0	0	X	0	X	0	X	1	X
14	0	0	1	0	0	0	0	1	0	X	0	X	1	X	0	X
15	0	0	0	1	0	0	0	0	0	X	1	0	X	0	X	1

→ K-map:

J _D :				
Q _D Q _C Q _B Q _A	00	101	11	10
00	1	0	0	0
01	0	0	0	0
11	X	X	X	X
10	X	X	X	X

$$J_D = \bar{Q}_C \bar{Q}_B \bar{Q}_A$$

K _D :				
Q _D Q _C Q _B Q _A	00	101	11	10
00	X	X	X	X
01	X	X	X	X
11	0	0	0	0
10	1	0	0	0

$$K_D = \bar{Q}_C \bar{Q}_B \bar{Q}_A$$

J _C :				
Q _D Q _C Q _B Q _A	00	101	11	10
00	1	0	0	0
01	X	X	X	X
11	X	X	X	X
10	0	0	0	0

$$J_C = \bar{Q}_B \bar{Q}_A$$

K _C :				
Q _D Q _C Q _B Q _A	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	1	0	0	0
10	X	X	X	X

$$K_C = \bar{Q}_B \bar{Q}_A$$

J _B :				
Q _D Q _C Q _B Q _A	00	01	11	10
00	1	0	X	X
01	1	0	X	X
11	1	0	X	X
10	1	0	X	X

$$J_B = \bar{Q}_A$$

K _B :				
Q _D Q _C Q _B Q _A	00	01	11	10
00	X	X	0	1
01	X	X	0	1
11	X	X	0	1
10	X	X	0	1

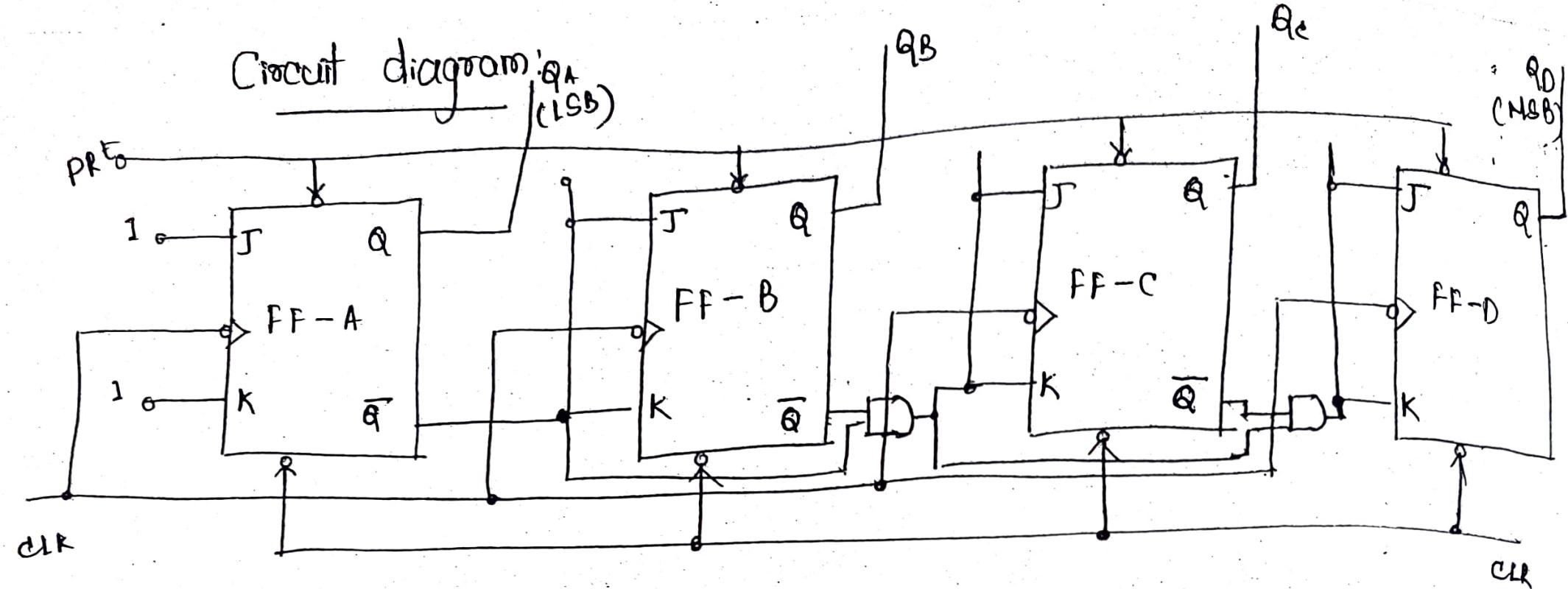
$$J_B = \bar{Q}_A$$

J _A :				
Q _D Q _C Q _B Q _A	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	1	1	X
10	X	1	1	X

$$J_A = 1$$

Circuit diagram
 Q_A
(LSB)

Q_D
(MSB)



Design a 4-bit synchronous UP counter using SR flip-flop.

(13)

The truth table of 4-bit synchronous UP counter using SR flip-flop is as shown below.

CLK	Present State				Next Stat.				Inputs to flip-flops							
	Q _D	Q _C	Q _B	Q _A	Q _D ⁺	Q _C ⁺	Q _B ⁺	Q _A ⁺	S _D	R _D	S _C	R _C	S _B	R _B	S _A	R _A
0	0	0	0	0	0	0	0	1	0	x	0	x	0	x	1	0
1	0	0	0	1	0	0	1	0	0	x	0	x	1	0	0	1
2	0	0	1	0	0	0	1	1	0	x	0	x	x	0	1	0
3	0	0	1	1	0	1	0	0	0	x	1	0	0	1	0	1
4	0	1	0	0	0	1	0	1	0	x	x	0	0	x	1	0
5	0	1	0	1	0	1	1	0	0	x	x	0	1	0	0	1
6	0	1	1	0	0	1	1	1	0	x	x	0	x	0	1	0
7	0	1	1	1	1	0	0	0	1	0	0	1	0	1	0	1
8	1	0	0	0	1	0	0	1	x	0	0	x	0	x	1	0
9	1	0	0	1	1	0	1	0	x	0	0	x	1	0	0	1
10	1	0	1	0	1	0	1	1	x	0	0	x	x	0	1	0
11	1	0	1	1	1	1	0	0	x	0	1	0	0	1	0	1
12	1	1	0	0	1	1	0	1	x	0	x	0	0	x	1	0
13	1	1	0	1	1	1	1	0	x	0	x	0	1	0	0	1
14	1	1	1	0	1	1	1	1	x	0	x	0	x	0	1	0
15	1	1	1	1	0	0	0	0	0	1	0	1	0	1	0	1

Excitation Table
of SR f/F

Q _n → Q _{n+1}	S	R
0	0	0
0	1	1
1	0	0
1	1	x

→ K-map:

S _D :	
Q _D	Q _D
00	00
01	00
11	00
10	x

$$S_D = \bar{Q}_D Q_C Q_B Q_A$$

R _D :	
Q _D	Q _D
00	00
01	x
11	x
10	x

$$R_D = Q_D Q_C Q_B Q_A$$

S _C :	
Q _C	Q _C
00	00
01	x
11	x
10	x

$$S_C = \bar{Q}_C Q_B Q_A$$

R _C :	
Q _C	Q _C
00	00
01	x
11	x
10	x

$$R_C = Q_C \cdot Q_B \cdot Q_A$$

S _B :	
Q _B	Q _B
00	00
01	x
11	x
10	x

$$S_B = \bar{Q}_B Q_A$$

R _B :	
Q _B	Q _B
00	x
01	x
11	x
10	x

$$R_B = Q_B Q_A$$

S _A :	
Q _A	Q _A
00	00
01	0
11	1
10	0

$$S_A = \bar{Q}_A$$

R _A :	
Q _A	Q _A
00	0
01	1
11	1
10	0

$$R_A = Q_A$$

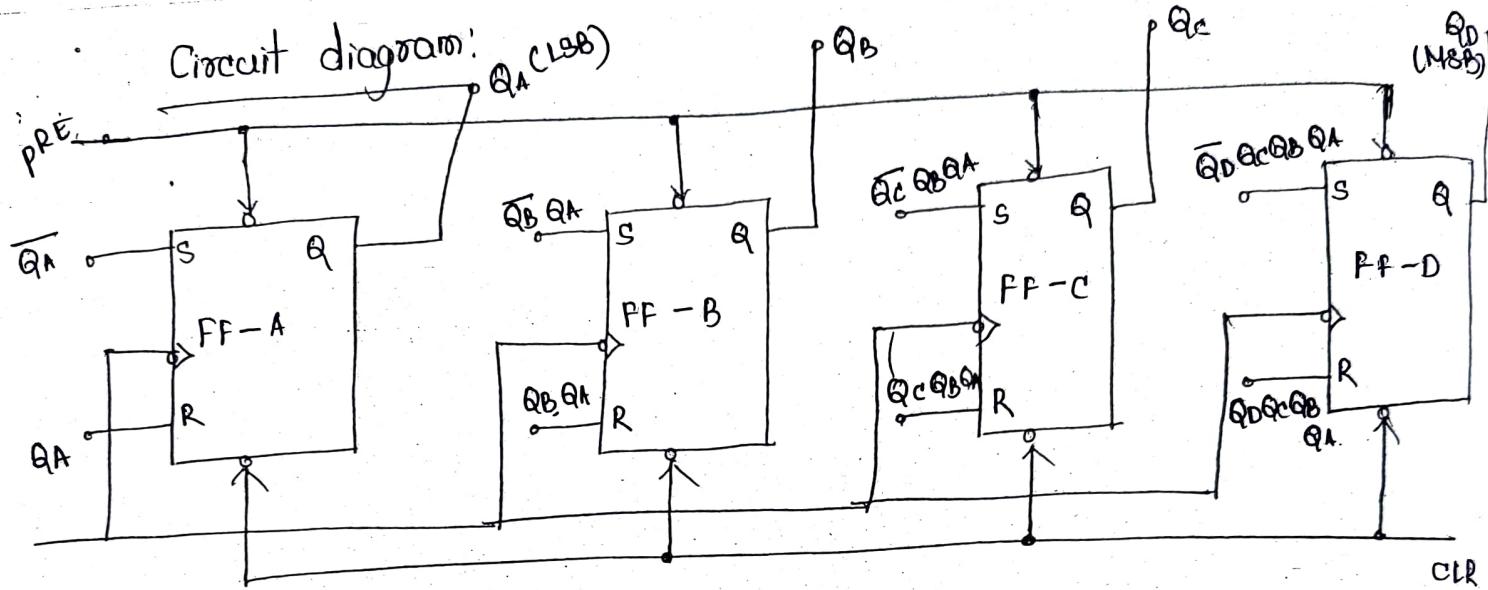


Fig. 1 4-bit synchronous UP counter

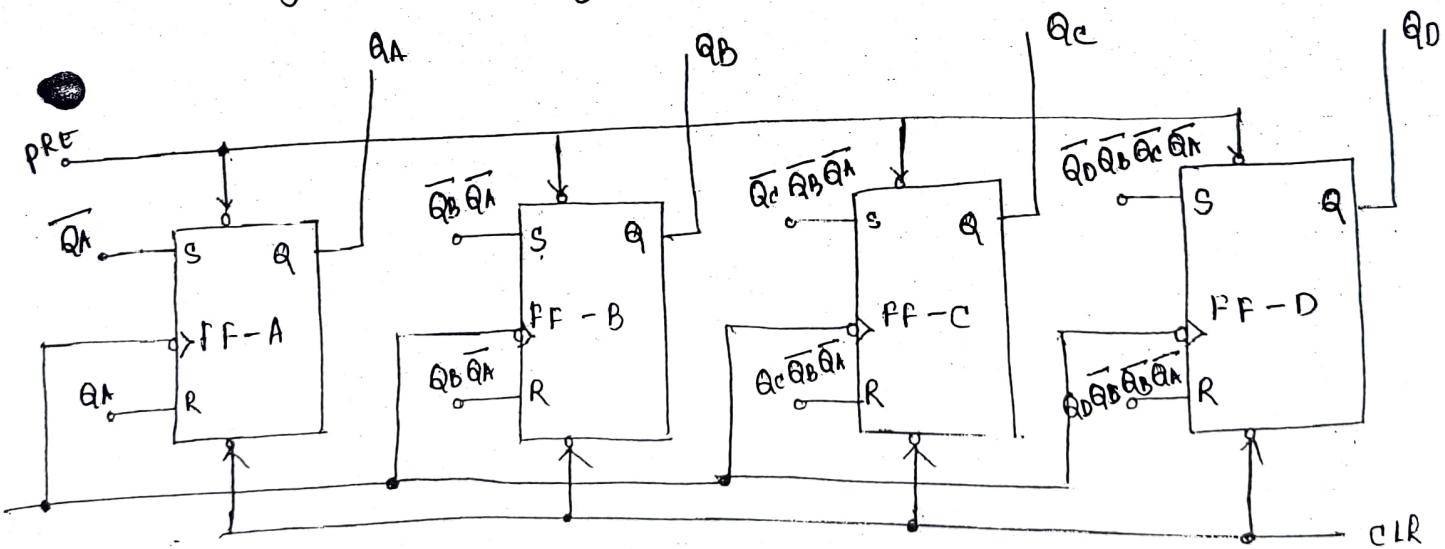


Fig. 2 4-bit synchronous DOWN counter

Q1. Design a 4-bit Synchronous DOWN counter using SR flip-flop

Q2. The truth table of 4-bit synchronous DOWN counter using SR flip-flop is as shown below (15)

CLK	Present State				Next State				Inputs to flip-flops								
	Q _D	Q _C	Q _B	Q _A	Q _D ⁺	Q _C ⁺	Q _B ⁺	Q _A ⁺	S _D	R _D	S _C	R _C	S _B	R _B	S _A	R _A	
0	1	1	1	1	1	1	1	0	X	0	X	0	X	0	0	1	
1	1	1	1	0	1	1	0	1	X	0	X	0	0	1	1	0	
2	1	1	0	1	1	1	0	0	X	0	X	0	0	X	0	1	
3	1	1	0	0	1	0	1	1	X	0	0	1	1	0	1	0	
4	1	0	1	1	1	0	1	0	X	0	0	X	X	0	0	1	
5	1	0	1	0	1	0	0	1	X	0	0	X	0	1	1	0	
6	1	0	0	1	1	0	0	0	X	6	0	X	0	X	0	1	
7	1	0	0	0	0	1	1	1	0	1	1	0	1	0	1	0	
8	0	1	1	1	0	1	1	0	X	X	0	X	X	0	0	1	
9	0	1	1	0	0	1	0	1	0	X	X	0	0	1	1	0	
10	0	1	0	1	0	1	0	0	0	X	X	0	0	X	0	1	
11	0	1	0	0	0	0	1	1	0	X	0	1	1	0	1	0	
12	0	0	1	1	0	0	0	0	0	X	0	X	X	0	0	1	
13	0	0	1	0	0	0	1	0	X	0	X	0	1	1	0		
14	0	0	0	1	0	0	0	0	0	X	0	X	0	X	0	1	
15	0	0	0	0	1	1	1	1	1	0	1	0	1	0	1	0	

Excitation Table of SR flip-flop

$Q_n \rightarrow Q_{n+1}$	S	R
0	0	0
0	1	1
1	0	0
1	1	X

→ Plot the K-map for flip-flop inputs.

S _D :	
Q _D ⁰⁰	00 01 11 10
00	1 0 0 0
01	0 0 0 0
11	X X X X
10	X X X X

$$S_D = \bar{Q}_D \bar{Q}_C \bar{Q}_B \bar{Q}_A$$

R _D :	
Q _D ⁰⁰	00 01 11 10
00	0 X X X
01	X X X X
11	0 0 0 0
10	1 0 0 0

$$R_D = Q_D \bar{Q}_C \bar{Q}_B \bar{Q}_A$$

S _C :	
Q _C ⁰⁰	00 01 11 10
00	1 0 0 0
01	0 X X X
11	0 X X X
10	1 0 0 0

$$S_C = \bar{Q}_C \bar{Q}_B \bar{Q}_A$$

R _C :	
Q _C ⁰⁰	00 01 11 10
00	X X X X
01	1 0 0 0
11	1 0 0 0
10	0 X X X

$$R_C = Q_C \bar{Q}_B \bar{Q}_A$$

S _B :	
Q _B ⁰⁰	00 01 11 10
00	0 X X X
01	X 0 X 0
11	0 X 0 1
10	0 X 0 1

$$S_B = \bar{Q}_B \bar{Q}_A$$

R _B :	
Q _B ⁰⁰	00 01 11 10
00	1 1 0 0
01	0 1 1 0
11	0 1 1 0
10	0 1 1 0

$$R_B = Q_B \bar{Q}_A$$

S _A :	
Q _A ⁰⁰	00 01 11 10
00	1 1 0 0
01	0 1 1 0
11	0 1 1 0
10	1 1 0 0

$$S_A = \bar{Q}_A$$

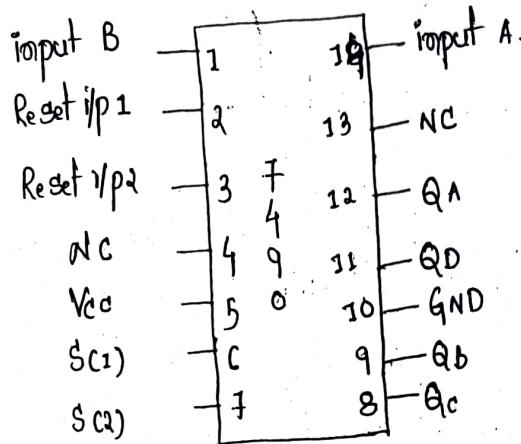
R _A :	
Q _A ⁰⁰	00 01 11 10
00	1 1 0 0
01	0 1 1 0
11	0 1 1 0
10	1 1 0 0

→ Circuit diagram (Refer page no. 14)

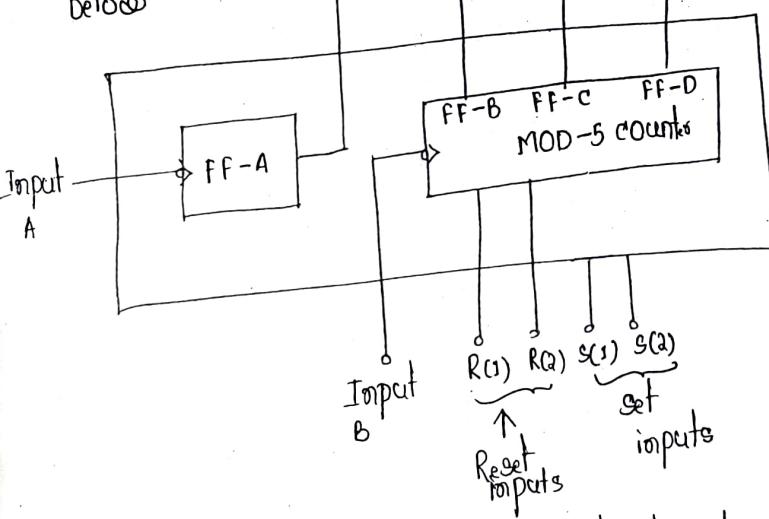
IC 7490 (Decade binary counter):

(16)

- IC 7490 is a decade binary counter. It consists of four master-slave flip flops and a three stage binary counter for which the count cycle length is divide by five.
- The pin diagram of IC 7490 is as shown below



- The internal architecture of IC 7490 is as shown below



- Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes.

i) BCD Decade counter

- The B input must be externally connected to the Q_A output and A input receives the incoming count and a BCD count sequence is produced.

Decade counter Truth Table:

CD4017	outputs
	Q _D Q _C Q _B Q _A
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1

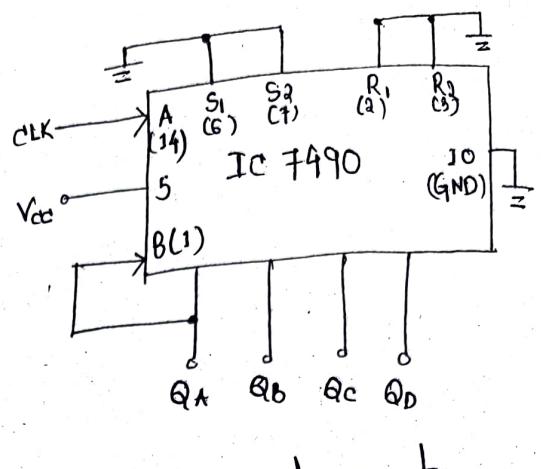


Fig. Decade counter.

ii) Divide by two and divide by five counter.

→ No external connections required.

→ FF-A; Divide by two counter

→ FF-B, FF-C, FF-D; Divide by five counter

E1: i) Design a divide by 97 counter using IC 7490.

→ IC 7490 is a decade counter. When two such ICs are cascaded, it becomes a divide by 100 counter.

→ To get a divide by 97 counter, the counter is reset as soon as it becomes 1001 0110.

→ The diagram is as shown below

