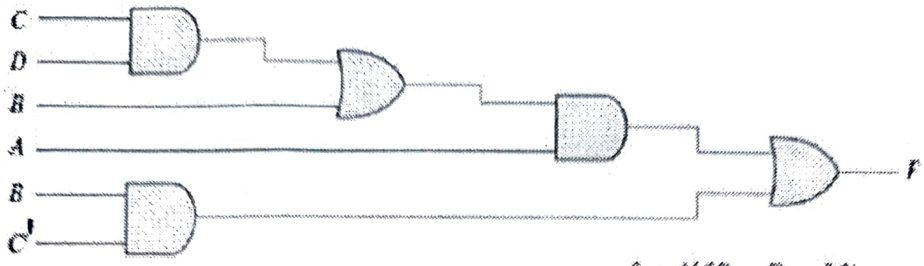
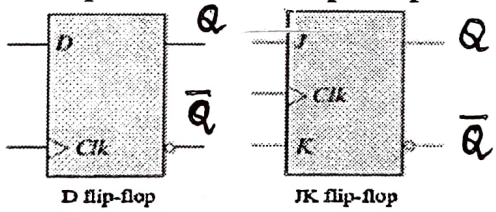
Vivekananda College of Engineering & Technology, Puttur [A Unit of Vivekananda Vidyavardhaka Sangha Puttur ®] Affiliated to VTU, Belagavi & Approved by AICTE New Delhi			
CRM08	Rev 1.15 (2024 rev)	<CS>	<14.10.2024>

CONTINUOUS INTERNAL EVALUATION - 1

Dept: AI/ CD/ CS	Sem / Div: **3 AI/ CD/ CS A & B**	Sub: **Digital Design and Computer Organization**	S Code: **BCS302**
Date: 18.10.2024	Time: 2:30-4:00	Max Marks: 50	Elective: N

Note: Answer any 2 full questions, choosing one full question from each part.

QN		Questions	Marks	RBT	CO's
		PART A			
1	a	Identify the prime implicants and essential prime implicants of the following functions: (i) $F(A, B, C, D) = \sum m(1, 3, 4, 5, 10, 11, 12, 13, 14, 15)$ (ii) $F(W, X, Y, Z) = \sum m(0, 1, 2, 5, 7, 8, 10, 15)$	10	L3	CO1
	b	With neat diagram, explain the basic operational concepts between processor and memory	9	L2	CO3
	c	Simplify and implement the following Boolean function using *NAND* Gates: $F(x, y, z) = \sum m(1, 2, 3, 4, 5, 7)$	6	L3	CO1
		OR			
2	a	Determine the minimum *SOP* form from using Karnaugh Map and draw the circuit diagram: (i) $F = A'B'C' + B'CD' + A'BCD' + AB'C'$ (ii) $F = x'z' + wyz + w'y'z' + x'y + wxy'z' + w'xyz$	10	L3	CO1
	b	Explain the following: (i) Processor time & Processor cache (ii) Basic performance equation (iii) Performance measurement	9	L2	CO3

	c	Using gate-level description & continuous assignment statements (data flow description), write a Verilog description of the circuit shown in the following Figure:  Figure Q2c $F = A(CD + B) + BC'$	6	L3	CO1
		PART B			
3	a	Implement the design of combinational circuit – *BCD* to *Excess-3* Code Converter	10	L2	CO2
	b	Realize the following Boolean functions using *8:1 MUX* with *A*, *B*, *C* as Select lines and *4:1 MUX* with *A*, *B* as Select lines: $Y(A, B, C, D) = \sum m(0, 1, 5, 6, 7, 11, 15)$	9	L3	CO2
	c	Write Verilog descriptions for *D* flip-flop and *JK* flip-flop  D flip-flop JK flip-flop	6	L3	CO2
		OR			
4	a	Design and explain four-bit adder	10	L2	CO2
	b	Define decoder. Describe the working principle of a *3:8* decoder. Draw the logic diagram of the *3:8* decoder with enable input. Realize the following Boolean expressions using a 3:8 decoder and multi-input OR gates: $F1(A, B, C) = \sum m(1, 3, 7)$ $F2(A, B, C) = \sum m(2, 3, 5)$	9	L3	CO2
	c	What is a Latch? With neat diagram, explain *SR* latch using *NOR* Gate.	6	L3	CO2

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