Vivekananda College of Engineering & Technology, Puttur [A Unit of Vivekananda Vidyavardhaka Sangha Puttur ®] Affiliated to VTU, Belagavi & Approved by AICTE New Delhi			
CRM08	Rev 1.16 (2024 rev)	CS	10-12-2024

CONTINUOUS INTERNAL EVALUATION - 2

Dept: **AI / CD / CS**	Sem / Div: **3 AI / CD / CS A / CS B**	Sub: **Digital Design and Computer Organization**	S Code: **BCS302**
Date: **18/12/2024**	Time: **2:30-4:00 PM**	Max Marks: 50	Elective: N

Note: Answer any 2 full questions, choosing one full question from each part.

QN		Questions	Marks	RBT	CO's
		PART A			
1	a	Define Addressing Mode. Explain any four addressing modes with an example.	5	L2	CO3
	b	What is Bus arbitration? Explain different bus arbitration techniques	10	L2	CO4
	c	Explain the following i. Hardware interrupt ii. Enabling/ disabling of interrupt iii. Sequence of events in handling interrupt request from a single device	10	L2	CO4
		OR			
2	a	Show how the arithmetic statement Y = (A * B) + (C * D) is executed using three address, two address, and one address instructions	5	L2	CO3
	b	Explain different types of cache mapping functions	10	L2	CO4
	c	Explain the Direct Memory Access technique with an example	10	L2	CO4
		PART B			

3	a	Explain the following: i. Byte Addressability ii. Word Addressability	5	L2	CO3
	b	Explain the single-bus organization of the data path inside a processor with a neat diagram.	10	L2	CO5
	c	Explain complete execution steps for branch instruction along with control sequence.	10	L2	CO5
		OR			
4	a	Explain the following: i. Big-endian assignment ii. Little-endian assignment	5	L2	CO3
	b	Define instruction pipeline? Explain four stage pipelining with hardware organization.	10	L2	CO5
	c	Explain the complete set of operations involved in executing the instruction ADD (R3), R1 along with control sequence.	10	L2	CO5

Prepared by: Mr. Mohan A R

13/12/24

HOD