Vivekananda College of Engineering & Technology, Puttur

[A Unit of Vivekananda Vidyavardhaka Sangha Puttur ®]
Affiliated to VTU, Belagavi & Approved by AICTE New Delhi

			04/05/05
CRM08	Rev 1.16	C5	24/05/25
01111100			

CONTINUOUS INTERNAL EVALUATION - 2

Dept: CS/CD	Sem / Div: 4 th	Sub: Microcontrollers	S Code: BCS402
Date: 28/05/2025	Time: 3:00-4:30	Max Marks: 50	Elective: N

Note: Answer any 2 full questions, choosing one full question from each part.

Qì	N	Questions	Marks	RBT	CO's
		PART A			
1		Explain ARM processors exceptions and modes with a neat diagram.	10	L2	CO4
	b	Explain IRQ and FIQ Exceptions and also code snippets to enable and disable IRQ and FIQ interrupts	10	L2	CO4
		Explain optimization with respect to Pointer aliasing with example.	5	L2	CO3
		OR			
2	a	What is firmware? Explain firmware execution flow steps	10	L2	CO4
	b	Explain sandstone and its execution flow briefly	10	L2	CO4
	С	Explain portability issues with respect to optimization.	5	L2	CO3
,		PART B			
3	a	Explain basic architecture of cache memory with neat diagram	10	L2	CO5
	b	Explain memory hierarchy and cache memory in detail	10	L2	CO5
	c	Explain Structure arrangement to be done in order to	5	L2	CO3

Page: 1 / 2

access structure members efficiently with example

access structure mensor		
he memory with diagram		L2 CO5
4 a Explain set associative cache memory with diagram b Explain how main memory is mapped to a cache	10	L2 CO5
b Explain how man in memory with diagram emory with diagram c Explain function call and argument passing procedure in	5	L2 CO3
ARM		Jun 26

Prepared by:

Dinesh Prasanna

Jones 105/25