Vivekananda College of Engineering & Technology, Puttur
[A Unit of Vivekananda Vidyavardhaka Sangha Puttur ®]
Affiliated to VTU, Belagavi & Approved by AICTE New Delhi

CRM08	Rev 1.16	<CS>	<04.04.2025>

CONTINUOUS INTERNAL EVALUATION – 1

Dept: CD/ CS	Sem / Div: 4th A & B	Sub: Microcontrollers	S Code: BCS402
Date: 15.04.2025	Time: 3:00-4:30	Max Marks: 50	Elective: N

Note: Answer any 2 full questions, choosing one full question from each part.

QN		Questions	Marks	RBT	CO's
		PART A			
1	a	Differentiate: (i) Microprocessor vs Microcontroller (ii) *CISC* vs *RISC*.	8	L2	CO1
	b	With neat diagram characterize the hardware components of embedded systems.	8	L2	CO1
	c	Explain the different basic data types in *C*. Provide examples of how each data type can be used in a *C* program.	9	L2	CO3
		OR			
2	a	With neat diagram, explain *ARM* core dataflow model.	8	L2	CO1
	b	What is pipeline in *ARM*? Illustrate with an example the pipeline stage of *ARM 9* and *ARM 10*.	8	L2	CO1
	c	Develop an assembly level program (i) for data transfer, arithmetic and logical operations (ii) to find the sum of first two integer numbers.	9	L2	CO3
		PART B			
3	a	Explain different logical instructions in *ARM* processor with example.	8	L2	CO2
	b	Explain single register load store addressing mode syntax, table, index mode with an example.	8	L2	CO2

	c	How compiler handles a "for loop" with variable number of interations *N* and loop controlling with an example.	9	L2	
		OR			
4	a	Explain stack operations.	8	L2	CO2
	b	Write a note on – (i) Software interrupt instruction (ii) Program status register instruction (iii) Coprocessor instructions.	8		CO2
	c	Discuss the concept of register allocation in compiler optimization. Illustrate its significance with an example.	9	L2	CO3

Prepared by: Dr. Mahesh Prasanna K

04/04/25

HOD