CBCS SCHEME

USN 4 V I

BCS402

Fourth Semester B.E./B.Tech. Degree Examination, June/July 2025
Microcontrollers

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Explain the major design rules to implement the RISC design philosophy.	08	L2	CO1
	b.	Differentiate between RISC and CISC processors.	04	L2	CO1
	c.	Explain ARM core data flow model, with neat diagram.	08	L2	CO1
		OR			
Q.2	a.	With the help of bit layout diagram, explain Current Program Status Register (CPSR) of ARM.	08	L2	CO1
	b.	With an example, explain the pipeline in ARM.	05	L2	CO1
	c.	Discuss the following with diagrams: (i) Von-Neuman architecture with cache (ii) Harvard architecture with TCM	07	L2	CO1
		Module – 2			
Q.3	a.	Explain the different data processing instructions in ARM.	08	L2	CO2
	b.	Explain the different branch instructions of ARM.	04	L2	CO2
	c.	Explain the following ARM instructions: (i) MOV r_1, r_2 (ii) ADDS r_1, r_2, r_4 (iii) BIC r_3, r_2, r_5 (iv) CMP r_3, r_4 (v) UMLAL r_1, r_2, r_3, r_4	08	L2	CO2
		OR			
Q.4	a.	Explain the different load store instructions in ARM.	08	L2	CO2
	b.	With an example, explain full descending stack operations.	07	L2	CO2
	c.	Develop an ALP to find the sum of first 10 integer numbers.	05	L3	CO2
		Module – 3			
Q.5	a.	List out basic C data types used in ARM. Develop a C program to obtain checksums of a data packet containing 64 words and write the compiler output for the above function.	08	L2	CO3
	b.	Explain the C looping structures in ARM.	08	L2	CO3
	c.	Explain pointer aliasing in ARM.	04	L2	CO2

		OR			
Q.6	**a.**	With an example, explain function calls in ARM.	**08**	**L2**	**CO3**
	b.	Explain register allocation in ARM.	**07**	**L2**	**CO3**
	c.	Write a brief note on portability issues when porting C code to ARM.	**05**	**L2**	**CO3**
		Module – 4			
Q.7	**a.**	Explain the ARM processor exceptions and modes, vector table and exception priorities.	**10**	**L2**	**CO4**
	b.	Explain the interrupts in ARM.	**10**	**L2**	**CO4**
		OR			
Q.8	**a.**	Explain the ARM firmware suite and red hat redboot.	**10**	**L2**	**CO4**
	b.	Explain the sandstone directory layout and sandstone code structure.	**10**	**L2**	**CO4**
		Module – 5			
Q.9	**a.**	Explain the basic architecture of a cache memory and basic operation of a cache controller.	**10**	**L2**	**CO5**
	b.	With a neat diagram, explain a 4 KB, four way set associative cache.	**10**	**L2**	**CO5**
		OR			
Q.10	**a.**	Explain the write buffers and measuring cache efficiency.	**08**	**L2**	**CO5**
	b.	Explain the cache policy.	**12**	**L2**	**CO5**

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