COMPUTER SYSTEM ARCHITECTURE SET 1

Questions 1 To 10

1.	For two variables, n=2 , the number of possible Boolean functions is (a) 4 (b) 8 (c) 16 (d) 12 (e) 2.
2.	The one major advantage of CMOS is its, (a) Low propagation delay (b) High propagation delay (c) Very low propagation delay (d) Very high propagation delay (e) No delay.
3.	64K memory contains how many words of 8 bits each? (a) 65,536 (b) 64,536 (c) 65,436 (d) 65,546 (e) 65,556.
4.	The simplest way to determine cache locations in which to store memory blocks is the, (a) Associative Mapping technique (b) Direct Mapping technique (c) Set-Associative Mapping technique (d) Indirect Mapping technique (e) Paging technique.
5.	The sum of -6 and -13 using 2's complement addition is, (a) 11100011 (b) 11110011 (c) 11001100 (d) 11101101 (e) 11100001.
6.	Which one of the following CPU registers holds the address of the instructions (instructions in the program stored in memory) to be executed next? (a) MAR (Memory address register) (b) MBR (Memory Buffer Register) (c) AC (Accumulator) (d) IR (Instruction Register) (e) PC (Program Counter).
7.	What are the major components of a CPU? (a) Control Unit, Register Set, Arithmetic Logic Unit (b) Control Unit, Memory Unit, Arithmetic Logic Unit (c) Memory Unit, Arithmetic Logic Unit, Auxiliary Memory (d) Register Set, Control Unit, Memory Unit

	(e) Register Set, Control Unit, Auxiliary Memory.
8.	Given the characteristic table of a JK flip-flop, find the missing output value. J K Q(t+1) 0 0 Q(t) 0 1 0 1 0 1 1 1 --- (a) Q(t) (b) Q'(t+1) (c) 1 (d) Q'(t) (e) Q(t+1).
9.	What is Q, when S = 1 and R = 1 for SR flip-flop? (a) No Change (b) Clear to 0 (c) Set to 1 (d) Complement of previous output (e) Indeterminate.
10.	What does T stands for in T flip-flop? (a) Top (b) Type (c) Toggle (d) Tickle (e) Tip.

Answers

1.	Answer : (a) Reason : The AND, and OR functions are only two of a total of 16 possible functions formed with two binary variables. Therefore, for two variables n=2, and the number of possible Boolean functions is 16.
2.	Answer : (a) Reason : This means that it is not practical for use in systems requiring high-speed operations. The characteristic parameters for the CMOS gate depend on the power supply voltage VDD that is used. The power dissipation increases with increase in voltage supply. The propagation delay decreases with increase in voltage supply and the noise margin is estimated to be about 40% of the voltage supply value.
3.	Answer : (a) Reason : Consider the 20-bit logical address. The 4-bit segment number specifies one of 16 possible segments. The 8-bit page number can specify up to 256 pages, and the 8-bit word field implies a page size of 256 words. This configuration allows each segment to have any number of pages up to 256. the smallest possible segment will have one page of 256 words. The largest possible segment will have 256 pages, for a total of 256*256 = 65,536 which means 64K words.
4.	Answer : (b) Reason : Associative memories are expensive compared to random-access memories because of the added logic associated with each cell. Therefore, the simplest way to determine cache locations in which to store memory blocks is the Direct Mapping.
5.	Answer : (d) Reason : 2's complement of -6 = 11111010 2's complement of -13 = 11110011

	Add the two numbers in their 2's complement form, including their sign bits and discard any carry out of the sign (leftmost) bit position. So the answer is 11101101 (-19). -6 11111010 -13 11110011 ---------- -19 11101101
6.	Answer : (e) Reason : Program Counter (PC) keeps track of the instruction of the program stored in memory.
7.	Answer : (a) Reason : The major components of CPU are Control Unit, Register Set, and Arithmetic Logic Unit.
8.	Answer : (d) Reason : The next state is a complement state.
9.	Answer : (e) Reason : When R = 1 and S = 1, race will always end with Master Latch in the logic 1 state, but this will not be certain with real components.
10.	Answer : (c) Reason : Toggle flip-flop as it changes its output on each clock edge.

COMPUTER SYSTEM ARCHITECTURE SET 2

Questions 11 To 20

11.	In which type of flip-flop the indeterminate condition of the SR flip-flop (when S=R=1) is eliminated? (a) Edge-triggered flip-flop (b) JK flip-flop (c) D flip-flop (d) T flip-flop (e) Master-slave flipflop.
12.	The bulk of the binary information in a digital computer is stored in memory, but all computations are done in (a) Timing Control (b) Memory Registers (c) Processor Registers (d) Program Control (e) Secondary Memory.
13.	Information transfer from one register to another is designated in symbolic form by means of (a) Control Function (b) Op Code (c) Registers (d) Replacement Operator (e) Arrow Operator.
14.	The registers found in the processor unit are (a) Operational registers (b) Memory registers (c) Storage registers

	(d) Binary registers (e) Temporary registers.
15.	Techniques that automatically move program and data blocks into the physical main memory when they are required for execution are called (a) Associative-Mapping techniques (b) Main Memory techniques (c) Virtual Memory techniques (d) Cache Memory techniques (e) Paging techniques.
16.	What digit is added to the Excess-3 code generation? (a) 3 (b) 4 (c) 2 (d) 1 (e) 0.
17.	The processor, ---------- and I/O Devices are interconnected by means of a common bus. (a) Cache Memory (b) Auxiliary Memory (c) Virtual Memory (d) Main Memory (e) Extended Memory.
18.	System Software usually includes a program called a --------, which helps the programmer find errors in a program. (a) Write Buffer (b) Read Buffer (c) Debugger (d) Both (a) and (c) above (e) Both (b) and (c) above.
19.	To convert octal code to binary code which of the following digital functions should be used? (a) Decoder (b) Encoder (c) Multiplexer (d) Demultiplexer (e) Binary adder.
20.	A full-adder is simply a connection of two half-adders joined by (a) AND gate (b) OR gate (c) NAND gate (d) NOR gate (e) XOR gate.

Answers

11.	Answer : (b) Reason : To SR flip-flop two new connections from Q and Q' outputs back to original input gates eliminate the indeterminate condition.
12.	Answer : (c)

	Reason : The operation part of an instruction code specifies the operation to be performed. This operation must be executed on some data stored in memory and/or processor registers. An instruction code, therefore, must specify not only the operation, but also the register or memory words where the operands are to be found, as well as the register or memory words where the result is to be stored. For this reason, the bulk of binary information in a digital computer is stored in memory, but all computations are done in Processor Registers.
13.	Answer : (d) Reason : A replacement operator consisting of the information transfer from one register to another, is designated in symbolic form.
14.	Answer : (a) Reason : Registers found in processor are called operational registers and in memory unit are called storage registers.
15.	Answer : (c) Reason : A virtual memory system provides a mechanism for translating program-generated addresses into correct main memory locations. This is done dynamically, while programs are being executed in the CPU. The translation or mapping is handled automatically by the hardware by means of a mapping table.
16.	Answer : (a) Reason : Excess-3code generation takes 3 as excess to the binary code.
17.	Answer : (a) Reason : The Bus master is allowed to initiate data transfer on the bus.
18.	Answer : (c) Reason : Debugger is a program, which finds errors in program.
19.	Answer : (a) Reason : Multiplexer is called as Data Selector in computers where Dynamic memory uses the same address lines for both row and column addressing and a set of multiplexers is used to first select row address and then switch to column address.
20.	Answer : (b) Reason : A full-adder is simply a connection of two half-adders joined by a OR gate, and other half-adder simplify the AND gate also.

Questions 21 to 30

21.	A combinational circuit that converts binary information from n input lines to a maximum of unique output lines is, (a) Decoder (b) Encoder (c) Full-adder (d) Full-subtractor (e) Half-subtractor.
22.	The correspondence between the main memory blocks and those in the cache is specified by (a) Mapping function

	(b) Replacement algorithm (c) Hit rate (d) Miss penalty (e) Segment function.
23.	The CPU nearly delays its operation for one memory cycle, to allow direct memory I/O transfer. This process is called, (a) Burst transfer (b) Cycle waiting (c) Cycle stealing (d) Cycle interrupting (e) Cycle execution.
24.	The control condition is terminated with (a) Comma (b) Semicolon (c) Colon (d) Hash (e) Dot.
25.	What are the missing values in the truth table of a half-adder given below? x y C S 0 0 -- -- 0 1 0 1 1 0 0 1 1 1 1 0

	(a) x (b) y (c) 0 (d) 1 (e) Indeterminate.
26.	What are the building blocks of combinational circuits? (a) Flip-flops (b) Logical gates (c) Latches (d) Registers (e) Decoders.
27.	x + xy = x is called, (a) Commutative Law (b) Associative Law (c) Distributive Law (d) Absorption Law (e) Identity Law.
28.	What is BCO equivalent of 011111000? (a) 370 (b) 307 (c) 703 (d) 730 (e) None of the above.

29.	Boolean functions expressed as a --------- of minterms or ---------- of maxterms are said to be in a canonical form. (a) Product, Sum (b) Sum, Product (c) Subtract, Divide (d) Divide, Subtract (e) Product, Divide.
30.	Which of the following modes are used to handle data transfer to and from peripherals? (a) Programmed I/O (b) Interrupted-initiated I/O (c) Direct memory access (d) Programmed I/O, Interrupted-initiated I/O, Direct memory access (e) Programmed I/O, Direct memory access.

Answers

21.	Answer : (a) Reason : Decoder uses address inputs as binary numbers and produces an output signal.
22.	Answer : (a) Reason : The correspondence between the main memory blocks and those in the cache is specified by a mapping function, because the basic characteristic of cache memory is fast access time. Therefore, very little or no time must be wasted when searching for words in the cache.
23.	Answer : (c) Reason : A technique called cycle stealing allows the DMA controller to transfer one data word at a time, after which it must return control of buses to the CPU.

24.	Answer : (c) Reason : The control condition is terminated with a colon.
25.	Answer : (c) Reason : When x = 0, y = 0 the corresponding carry and sum are 0,0.
26.	Answer : (b) Reason : Logical gates are building blocks of combinational circuits whereas, flipflops are combination of logic gates, registers are memory storages.
27.	Answer : (d) Reason : Absorption law :- x + xy = x = x (1+y) = x. 1 = x.
28.	Answer : (a) Reason : The binary number 011 111 000 represents the octal digits 3, 7, 0 from left to right distrubution by three bits.
29.	Answer : (b) Reason : Boolean functions expressed as a sum (ORing of terms) of minterms or maxterms (ANDing of terms) are said to be in canonical form.
30.	Answer : (d) Reason : All the options are used to handle data transfer to and from peripherals.

COMPUTER SYSTEM ARCHITECTURE SET 4

Questions 31 To 40

31.	The gray code of a given binary number 1001 is (a) 1110 (b) 0110 (c) 1101 (d) 1111 (e) 0000.
32.	Which of the following representation requires the least number of bits to store the

	number +255? (a) BCD (b) 2's complement (c) 1's complement (d) Unsigned binary (e) Signed binary.
33.	For two variables, n=2 , the number of possible Boolean functions is (a) 4 (b) 8 (c) 16 (d) 12 (e) 2.
34.	The one major advantage of CMOS is its, (a) Low propagation delay (b) High propagation delay (c) Very low propagation delay (d) Very high propagation delay (e) Super High propagation delay.
35.	64K memory contains how many words of 8 bits each? (a) 65,536 (b) 64,536 (c) 65,436 (d) 65,546 (e) 65,556.
36.	The simplest way to determine cache locations in which to store memory blocks is the, (a) Associative Mapping technique (b) Direct Mapping technique (c) Set-Associative Mapping technique (d) Indirect Mapping technique (e) Indirect associative mapping technique.
37.	The sum of -6 and -13 using 2's complement addition is, (a) 11100011 (b) 11110011 (c) 11001100 (d) 11101101 (e) 11100001.
38.	Which one of the following CPU registers holds the address of the instructions (instructions in the program stored in memory) to be executed next? (a) MAR (Memory address register) (b) MBR (Memory Buffer Register) (c) AC (Accumulator) (d) IR (Instruction Register) (e) PC (Program Counter).
39.	What are the major components of a CPU?

(a) (b) (c) (d) (e)	Control Unit, Register Set, Arithmetic Logic Unit Control Unit, Memory Unit, Arithmetic Logic Unit Memory Unit, Arithmetic Logic Unit, Auxiliary Memory Register Set, Control Unit, Memory Unit Register Set, Control Unit, Auxiliary Memory.
40.	Given the characteristic table of a JK flip-flop, find the missing output value. J K Q(t+1) 0 0 Q(t) 0 1 0 1 0 1 1 1 ---
(a) (b) (c) (d) (e)	Q(t) Q'(t+1) 1 Q'(t) Q(t+1).

Answers

31.	Answer : (c)
Reason:	The gray code of 1001 is 1101
32.	Answer : (d)
Reason:	Unsigned binary representation occupies less space to store the number +255.
33.	Answer : (c)
Reason:	The AND, and OR functions are only two of a total of 16 possible functions formed with two binary variables. Therefore, for two variables n=2, and the number of possible Boolean functions is 16.
34.	Answer : (b)
Reason:	This means that it is not practical for use in systems requiring high-speed operations. The characteristic parameters for the CMOS gate depend on the power supply voltage VDD that is used. The power dissipation increases with increase in voltage supply. The propagation delay decreases with increase in voltage supply and the noise margin is estimated to be about 40% of the voltage supply value.
35.	Answer : (a)
Reason:	Consider the 20-bit logical address. The 4-bit segment number specifies one of 16 possible segments. The 8-bit page number can specify up to 256 pages, and the 8-bit word field implies a page size of 256 words. This configuration allows each segment to have any number of pages up to 256. the smallest possible segment will have one page of 256 words. The largest possible segment will have 256 pages, for a total of 256*256 = 65,536 which means 64K words.
36.	Answer : (b)
Reason:	Associative memories are expensive compared to random-access memories because of the added logic associated with each cell. Therefore, the simplest way to determine cache locations in which to store memory blocks is the Direct Mapping.
37.	Answer : (d) Reason: 2's complement of -6 = 11111010 2's complement of -13 = 11110011 Add the two numbers in their 2's complement form, including their sign bits and discard any carry out of the sign (leftmost) bit position. So the answer is 11101101 (-19). -6 11111010

	-13 11110011 ---------- -19 11101101
38.	Answer : (e)
Reason:	Program Counter (PC) keeps track of the instruction of the program stored in memory.
39.	Answer : (a)
Reason:	The major components of CPU are Control Unit, Register Set, and Arithmetic Logic Unit.
40.	Answer : (d)
Reason:	

COMPUTER SYSTEM ARCHITECTURE SET 5

Questions 41 To 50

41.	What is Q, when S = 1 and R = 1 for SR flip-flop?
(a)	No Change
(b)	Clear to 0
(c)	Set to 1
(d)	Complement of previous output
(e)	Indeterminate.
42.	What does T stands for in T flip-flop?
(a)	Top
(b)	Type
(c)	Toggle
(d)	Tickle
(e)	Bottom.
43.	In which type of flip-flop the indeterminate condition of the SR flip-flop (when S=R=1) is eliminated?
(a)	Edge-triggered flip-flop
(b)	JK flip-flop
(c)	D flip-flop
(d)	T flip-flop
(e)	KJ flip-flop.
44.	The bulk of the binary information in a digital computer is stored in memory, but all computations are done in
(a)	Timing Control
(b)	Memory Registers
(c)	Processor Registers
(d)	Program Control
(e)	Processor Control.
45.	Information transfer from one register to another is designated in symbolic form by means of a
(a)	Control Function

(b)	Op Code
(c)	Registers
(d)	Replacement Operator
(e)	Flip-flops.
46.	The registers found in the processor unit are
(a)	Operational registers
(b)	Memory registers
(c)	Storage registers
(d)	Binary registers
(e)	Control registers.
47.	Techniques that automatically move program and data blocks into the physical main memory when they are required for execution are called
(a)	Associative-Mapping techniques
(b)	Main Memory techniques
(c)	Virtual Memory techniques
(d)	Cache Memory techniques
(e)	Primary Memory techniques.
48.	Given below are the octal numbers and their Binary Coded Decimal (BCD) equivalents, which are not in order. Match the following octal numbers with their respective BCD equivalents and select the correct sequence. Octal number BCD equivalent 10 i. 111111 9 ii. 110010 20 iii. 001001 50 iv. 010100 77 v. 001010
(a)	iii, ii, i, iv, v
(b)	v, iv, ii, iii, i
(c)	v, iv, i, iii, ii
(d)	i, ii, iv, v, iii
(e)	v, iv, iii, ii, i.
49.	The processor, _____ and I/O Devices are interconnected by means of a common bus.
(a)	Cache Memory
(b)	Auxiliary Memory
(c)	Virtual Memory
(d)	Main Memory
(e)	Primary Memory.
50.	System Software usually includes a program called a _____ , which helps the programmer to find errors in a program.
(a)	Write Buffer
(b)	Read Buffer
(c)	Debugger
(d)	Both (a) and (c) above
(e)	Both (b) and (c) above.

Answers

41.	Answer : (e)
Reason:	When R = 1 and S = 1, race will always end with Master Latch in the logic 1 state, but this will not be certain with real components.
42.	Answer : (c)
Reason:	Toggle flip-flop as it changes its output on each clock edge.
43.	Answer : (b)
Reason:	To SR flip-flop two new connections from Q and Q' outputs back to original input gates eliminate the indeterminate condition.
44.	Answer : (c)
Reason:	The operation part of an instruction code specifies the operation to be performed. This operation must be executed on some data stored in memory and/or processor registers. An instruction code, therefore, must specify not only the operation, but also the register or memory words where the operands are to be found, as well as the register or memory words where the result is to be stored. For this reason, the bulk of binary information in a digital computer is stored in memory, but all computations are done in Processor Registers.
45.	Answer : (d)
Reason:	A replacement operator consisting of the information transfer from one register to another, is designated in symbolic form.
46.	Answer : (a)
Reason:	Registers found in processor are called operational registers and in memory unit are called storage registers.
47.	Answer : (c)
Reason:	A virtual memory system provides a mechanism for translating program-generated addresses into correct main memory locations. This is done dynamically, while programs are being executed in the CPU. The translation or mapping is handled automatically by the hardware by means of a mapping table
48.	Answer : (b)
Reason:	The octal number and their binary coded equivalent BCD is a straight assignment of binary equivalent. It is possible to assign weights to the binary bits according to their position as per conversion of octal number to binary number.
49.	Answer : (a)
Reason:	The processor, cache memory and I/O devices are interconnected by means of a common bus.
50.	Answer : (c)
Reason:	Debugger is a program, which finds errors in program.

COMPUTER SYSTEM ARCHITECTURE SET 6

Questions 51 To 60

51.	To convert octal code to binary code which of the following digital functions should be used?
(a)	Decoder
(b)	Encoder

(c)	Multiplexer
(d)	Demultiplexer
(e)	Half adder.

52.	A full-adder is simply a connection of two half-adders joined by a,
(a)	AND gate
(b)	OR gate
(c)	NAND gate
(d)	NOR gate
(e)	XOR gate.

53.	The correspondence between the main memory blocks and those in the cache is specified by a
(a)	Miss penalty
(b)	Replacement algorithms
(c)	Hit rate
(d)	Page fault
(e)	Mapping functions.

54.	The number of 256*4 RAM chips required to construct 2KB CACHE is
(a)	8
(b)	2
(c)	4
(d)	16
(e)	32.

55.	The set of physical addresses is called
(a)	Disk Space
(b)	Address Space
(c)	Pages
(d)	Frames
(e)	Location.

56.	What is the name of device that is allowed to initiate data transfer on the bus?
(a)	Bus Master
(b)	Bus Arbitration
(c)	Bus Cycle
(d)	Bus Request
(e)	Parallel Bus.

57.	The DMA transfer technique where transfer of one word data at a time is called
(a)	Cycle stealing
(b)	Memory stealing
(c)	Hand-shaking
(d)	Inter-leaving
(e)	Bus stealing.

58.	What interface is used to connect the processor to I/O devices that require transmission of data one bit at a time?
(a)	Parallel
(b)	Serial
(c)	Output

(d) Input
(e) Bus

59. What are the building blocks of combinational circuits?

(a) Flip-flops
(b) Logic gates
(c) Latches
(d) Registers
(e) Inputs.

60. The transfer of new information into the register is called

(a) Execution
(b) Loading
(c) Shifting
(d) Configuring
(e) Uploading.

Answers

51.	Answer : (a)
Reason:	Decoder.
52.	Answer : (b)
Reason:	A full-adder is simply a connection of two half-adders joined by a OR gate, and other half-adder simplify the AND gate also.
53.	Answer : (e)
Reason:	The corresponding between the main memory blocks and those in the cache is specified by a mapping function, because the basic characteristic of cache memory is fast access time. Therefore, very little or no time must be wasted when searching for words in the cache.
54.	Answer : (d) Reason: 16 RAM chips of size 256*4 are needed to construct a CACHE of size 2KB
55.	Answer : (b)
Reason:	The collection of address spaces in a physical memory is called address space.
56.	Answer : (a)
Reason:	The Bus master is allowed to initiate data transfer on the bus.
57.	Answer : (a)
Reason:	Transfer of one word data at a time using DMA transfer technique is called Cycle Stealing.
58.	Answer : (b)
Reason:	Serial interface transfers one bit at a time, whereas others can handle more than one bit.
59.	Answer : (b)
Reason:	In a based Logical gates are building blocks of combinational circuits whereas, flipflops are combination of logic gates, registers are memory storages.
60.	Answer : (b)
Reason:	Entering new information into a register is called loading.

Questions 61 To 70

61. **Convert decimal value** $(888)_{10}$ **to base-5.**

(a) $(444)_5$
(b) $(12023)_5$
(c) $(131313)_5$
(d) $(12021)_5$
(e) $(31320)_5$.

62. Consider the following logic function f(ABC).
f(A,B,C) = (A + B + C') . (A + B'+ C')
Which of the following would be the result if the above logic function is to be simplified using k-maps?

(a)	C' + A
(b)	C + C'A'
(c)	C.A'
(d)	C'.A
(e)	C'.A' + B.

63. What is the equivalent in hexadecimal for the decimal number 973?

(a)	4BC
(b)	CB4
(c)	6D
(d)	3CD
(e)	4CD.

64. What is the word size of a 8086 processor?

(a)	8 bits
(b)	16 bits
(c)	32 bits
(d)	64 bits
(e)	128 bits.

65. What kind of Information is stored inside the computer?

(a)	Binary form
(b)	ASCII code form
(c)	Decimal form
(d)	Alpha numeric
(e)	Numeric form.

66. What is a parity bit?

(a)	It is used to indicate uppercase letters
(b)	It is used to detect errors
(c)	It is the first bit in a byte
(d)	It is the last bit in a byte
(e)	It is used to indicate lowercase letters.

67. What is the minimum number of bits required to store the Hexadecimal number FF?
(a) 2
(b) 4
(c) 8

(d) 16
(e) 32.

68. What is the purpose of the floating point unit(FPU)?

(a)	Makes integer arithmetic faster
(b)	Makes pipelining efficient
(c)	Increases RAM capacity
(d)	Makes some arithmetic calculations faster
(e)	Decreases RAM capacity.

69. Which of the following is **not** a type of processor?

(a)	PowerPC 601
(b)	Motorola 8086
(c)	Motorola 68000
(d)	Intel Pentium
(e)	Z80.

70. Cycle stealing is/are used in which concept?

(a)	Programmed I/O
(b)	DMA
(c)	Interrupts
(d)	Memory mapped I/O
(e)	All of the above.

Answers

61.	Answer : (b) Reason : Divide the given number 888 by 5 and write all the remainder terms from the bottom to up and finally we will get (12023) to the base 5
62.	Answer : (a) Reason : C' + A
63.	Answer : (d) Reason : 3CD
64.	Answer : (b) Reason : 8086 is a 16 bit processor.
65.	Answer : (a) Reason : The data inside a computer is represented in Binary form i.e (0's and 1's).
66.	Answer : (b) Reason : A parity bit is used to detect errors.
67.	Answer : (b) Reason : The minimum number of bits required to store a Hexadecimal number FF is 4.
68.	Answer : (d) Reason : Makes some arithmetic calculations faster.

69.	Answer : (b) Reason : Motorola 8086 is not a processor.
70.	Answer : (b) Reason : Cycle Stealing concept is used in DMA .

COMPUTER SYSTEM ARCHITECTURE SET 8

Questions 71 To 80

71. **What is an optical storage?**

(a)	Has faster access time than disk storage
(b)	Smaller capacity than CD-ROM
(c)	Greater capacity than DAT storage
(d)	Smaller capacity than DAT storage
(e)	Greater capacity than CD-ROM.

72. What is the purpose of RAID system?

(a)	It increases the processor speed
(b)	It increases the disk storage capacity
(c)	It increases the disk storage capacity and availability
(d)	It increases operating system efficiency
(e)	It decreases operating system efficiency.

73. What is the purpose of Stack Pointer (SP) register?

(a)	It is used for accessing strings
(b)	It is used for accessing memory
(c)	It is used for accessing stack
(d)	It is used for accessing data segment
(e)	It is used for accessing code segment.

74. Which of the following statements is **wrong**

(a)	Combinational circuits has memory
(b)	Sequential circuits has memory
(c)	Sequential circuits is a function of time
(d)	Combinational circuits does not require feed back paths
(e)	Sequential circuits require feed back paths.

75. Which of the following is **not** involved in memory write operation?

(a)	MAR
(b)	PC
(c)	IR
(d)	MDR
(e)	Data Bus.

76. Which of the following is responsible for coordinating various operations using timing signals?

(a) Arithmetic-logic unit
(b) Control unit
(c) Memory unit

(d) Input unit
(e) Output unit.

77. What is LRU algorithm?

(a)	Pages out pages that have been used recently
(b)	Pages out pages that have not been used recently
(c)	Pages out pages that have been least used recently
(d)	Pages out the first page in given data
(e)	Pages out the last page in given data.

78. Which of the following is **true** about ROM?

(a)	ROM is faster to access than RAM
(b)	ROM is non-volatile memory
(c)	ROM stores more information than RAM
(d)	ROM is used for cache memory
(e)	ROM is temporary memory.

79. Cache memory enhances

(a)	Memory capacity
(b)	Memory access time
(c)	Secondary storage capacity
(d)	Secondary storage access time
(e)	Data transfer time.

80. An OR gate generates a low output when

(a)	Any one of its inputs is low
(b)	Any one of its inputs is high
(c)	All of its inputs are low
(d)	Power fails
(e)	Either of the inputs are high.

Answers

71.	Answer : (a) Reason : optical storage has faster access time than disk storage.
72.	Answer : (c) Reason : It increases the disk storage capacity and availability.
73.	Answer : (c) Reason : It is used for accessing stack.
74.	Answer : (a) Reason : Combinational circuits has memory.
75.	Answer : (e) Reason : Data Bus is not involved in memory write operation.
76.	Answer: (b) Reason : Arithmetic-logic unit is responsible for coordinating various operations using timing signals
77.	Answer : (c) Reason : pages out pages that have been least used recently
78.	Answer : (b) Reason : ROM is a non-volatile memory.
79.	Answer : (b) Reason : Cache memory enhances memory access time.

80.	Answer : (c) Reason : When all of its inputs are low and high.

COMPUTER SYSTEM ARCHITECTURE SET 9

Questions 81 To 90

81. **A machine cycle refers to**

(a)	Fetching an instruction
(b)	Clock speed
(c)	Fetching, decoding and executing an instruction
(d)	Executing and instruction
(e)	Decoding an instruction.

82. The System bus is made up of

(a)	Control bus
(b)	Address bus
(c)	Both Control bus and Address bus
(d)	Control bus, Data bus and Address bus
(e)	Data bus.

83. The code used to boot up a computer is stored in

(a)	RAM
(b)	ROM
(c)	PROM
(d)	EPROM
(e)	EEPROM.

84. In accessing a disk block the longest delay is due to

(a)	Rotation time
(b)	Seek time
(c)	Transfer time
(d)	Clock speed
(e)	Access time.

85. Which of the following is/are **not** part(s) of the CPU?

(a) ALU
(b) The Control unit
(c) The Registers
(d) System bus
(e) All of the above.

86. Memory mapped I/O involves transferring of

(a) Information between memory locations
(b) Information between registers and memory
(c) Information between CPU and I/O devices
(d) Information between CPU and Memory
(e) Information between I/O devices and CPU.

87. Name the type of memory that can be erased with the electric discharge?

(a) ROM

(b) EPROM
(c) RAM
(d) EEPROM
(e) PROM.

8. What is the units for measuring the CPU performance?
(a) BPS
(b) MIPS
(c) MHz
(d) VLSI
(e) KHz.

89. The read/write line belongs to
(a) The data bus
(b) The control bus
(c) The address bus
(d) CPU bus
(e) System bus.

90. Busy waiting is a technique
(a) To allow the CPU wait for a busy device
(b) To allow a busy device wait for the CPU
(c) To keep an idle device busy
(d) To improve CPU performance
(e) To keep a device busy.

Answers

81.	Answer : (c) Reason : A machine cycle refers to Fetching, decoding and executing an instruction.
82.	Answer : (d) Reason : System bus consists of a Control bus, Data bus and a Address bus.
83.	Answer : (b) Reason : The bootable code is stored in ROM.
84.	Answer : (e) Reason : Access time.
85.	Answer : (d) Reason : System bus is not a part of a cpu .
86.	Answer : (e) Reason : Memory mapped I/O involves transferring information between I/O devices and CPU .
87.	Answer : (d) Reason : EEPROM is the type of memory whose contents is erased with the passage of electiricity.
88.	Answer : (c) Reason : CPU performance is measured in MHz
89.	Answer : (c) Reason : The read / write line belongs to the address bus.a
90.	Answer : (a) Reason : Busy waiting is to allow the CPU wait for a busy device.

COMPUTER SYSTEM ARCHITECTURE SET 10

Questions 91 To 100

91.	Which of the following Addressing Modes specifies a register which contains the memory address of the operand? (a) Indirect Addressing Mode (b) Register Addressing Mode (c) Register Indirect Addressing Mode (d) Index Addressing Mode (e) Base Address Register Addressing Mode.
92.	Identify the term, which indicate a set of Logical Addresses. (a) Memory space (b) Disk space (c) Address space (d) Location (e) Page frame.
93.	Which of the following is **false** related to Stack? (a) Stack Pointer points to the top most element of the stack (b) Only PUSH and POP operations are applicable (c) Implements FIFO (d) Useful for nested loops, subroutine calls etc (e) Efficient for arithmetic expression evaluation.
94.	Which of the following is the method in which the unit receiving the data responds with another control signal? (a) Timing sequence (b) Synchronous (c) Strobe (d) Short message service (e) Handshaking.
95.	What is the page replacement algorithm in which there is a replacement of a page, which will not be used for the longest period of time? (a) MFU (b) LRU (c) OPT (d) FIFO (e) LFU.
96.	Of the following, what is an input device for which finger shows the cursor movement? (a) Mouse (b) Scanner (c) Microphone (d) Trackball (e) Glide pad.
97.	Consider the following unsigned decimal numbers: i. 6543. ii. 4444. What is the result after subtracting (**i)** by taking the 10's complement of (**ii)**? (a) 2098

	(b) 2099 (c) 2096 (d) 2097 (e) 2095.
98.	What is the octal equivalent of given binary number? **011001** (a) 32 (b) 31 (c) 34 (d) 33 (e) 35.
99.	Which of the following describes the Mnemonic SPA? (a) Skip If (Address Resister) Positive (b) Skip If (Accumulator) Positive (c) Skip If (Adder-Subtractor) Positive (d) Skip If (Associative Mapping) Positive (e) Skip If (Assembler) Positive.
100.	Which of the following is **correct** related to the circuit diagrams? (a) Sequential circuit is an interconnection of only logic gates (b) Sequential circuit is an interconnection of only flip flops (c) Combinational circuit is an interconnection of logic gates (d) Combinational circuit is an interconnection of flip flops (e) Part of a combinational circuit is a sequential circuit.

Answers

91.	Answer : (c) Reason: Addressing mode that specifies a register which contains the memory address of the operand is Register Indirect Addressing Mode.
92.	Answer : (c) Reason: Address space indicate a set of Logical Addresses.
93.	Answer : (c) Reason: Stack does not Implement FIFO but implements LIFO.
94.	Answer : (e) Reason: Handshaking is the method in which the unit receiving the data responds with another control signal.
95.	Answer : (c) Reason: The page replacement algorithm in which there is a replacement of a page, which will not be used for the longest period of time is OPT.
96.	Answer : (e) Reason: The input device for which finger shows the cursor movement is Glide pad.
97.	Answer : (b) Reason: 6543- 4444= 2099
98.	Answer : (b) Reason: The octal equivalent of 011001 =31.
99.	Answer : (b)

Reason:	SPA stands for Skip If (Accumulator) Positive
Answer:	(c)
Reason:	Combinational circuit is an interconnection of logic gates.

COMPUTER SYSTEM ARCHITECTURE SET 11

Questions 101 To 110

101.	Of the following, identify the memory usually written by the manufacturer. (a) RAM (b) DRAM (c) SRAM (d) ROM (e) Cache Memory.
102.	What does D stands for in D-flip flop? (a) Direct (b) Don't care (c) Double (d) Delay (e) Data.
103.	Consider that the program is executed from main memory until it attempts to reference a page that is still in auxiliary memory. Identify this condition. (a) Page Found (b) Page Fault (c) Page Hit (d) Page Miss (e) Page Replace.
104.	DMA stands for (a) Direct Memory Address (b) Direct Main Address (c) Direct Memory Access (d) Direct Main Access (e) Device Memory Access.
105.	What is the symbol to represent a state in the state diagram?
106.	Consider DR ← M [AR], Identify the operation. (a) Arithmetic Operation (b) Shift Operation (c) Memory Write (d) Memory Read (e) Memory Cycle.
107.	A computer has memory of 256k words of 32 bits each, how many bits are required to specify the address part?

	(a) 16 bits (b) 12 bits (c) 8 bits (d) 18 bits (e) 10 bits.
108.	Which one of the following can be called as a peripheral? (a) Control Unit (b) Arithmetic Unit (c) Speakers (d) Logic Unit (e) Main Memory.
109.	is a symbol for (a) OR (b) XOR (c) AND (d) NAND (e) NOR.
110.	What is the operation sets to 1 the bits in one register where there are corresponding 1's in the second register? (a) Selective Complement (b) Selective Clear (c) Selective Set (d) Mask (e) Insert.

Answers

Answer: 101.	(d) Reason: ROM is the memory usually written by the manufacturer.
102.	Answer : (e) Reason: D stands in D-flip flop stands for Data.
Answer: 103.	(b) Reason: The program is executed from main memory until it attempts to reference a page that is still in auxiliary memory called Page Fault.
Answer: 104.	(c) Reason: DMA stands for Direct Memory Access.
Answer: 105.	(b) Reason: The symbol to represent a state in the state diagram is
Answer: 106.	(d) Reason: DR ← M [AR] is Memory Read.
Answer: 107.	(d) Reason: A computer has memory of 256k words of 32 bits each, 18 bits are required to specify the address part.
Answer: 108.	(c)

	Reason: Speakers can be called as a peripheral.
109.	Answer: (c)
	Reason: is a symbol for AND.
110.	Answer: (c)
	Reason: Selective Set is the operation sets to 1 the bits in one register where there are corresponding 1's in the second register.

COMPUTER SYSTEM ARCHITECTURE SET 12

Questions 111 To 120

111.	What is represented by $D_7I'T$ in the instruction cycle? (a) Register – Reference Instructions (b) Program Interrupt (c) Input-Output Instructions (d) Branch Instruction (e) Memory Reference Instructions.
112.	What is the (r-1)'s complement of 345 in octal number system? (a) 342 (b) 234 (c) 243 (d) 432 (e) 423.
113.	What is described by the Mnemonic SHRA? (a) Arithmetic shift left (b) Logical shift right (c) Logical shift left (d) Circular shift right (e) Arithmetic shift right.
114.	Which of the following terms describe that the information which will be used in near future is likely to be in use already? (a) Spatial Locality (b) Locality (c) Hit ratio (d) Temporal Locality (e) Effective access time.
115.	CISC stands for (a) Control Instruction Set Completeness (b) Complex Instruction Set Conversion (c) Complex Instruction Set Computer (d) Control Instruction Set Computer (e) Complex Instruction Set Control.

116.	What are the three state gates in a digital circuit? (a) Logic 0, Logic 1 Complement, High Impedance (b) Logic 0 Complement, Logic 1, High Impedance (c) Logic 0 Complement, Logic 1 Complement, High Impedance (d) Logic 0, Logic 1, Low Impedance (e) Logic 0, Logic 1, High Impedance.
117.	What is the table that lists the required inputs for a given change of state? (a) Characteristic table (b) Truth table (c) Null table (d) Excitation table (e) Binary table.
118.	Microphone is a/an (a) Output device (b) Storage device (c) Input device (d) Processing device (e) Printing device.
119.	Of the following phases, identify the phase in which the programs must reside in the main memory. (a) Deletion (b) Execution (c) Printing (d) Reading (e) Insertion.
120.	(x')'=_____ (a) x^2 (b) 0 (c) 1 (d) x (e) x'.

Answers

Answer 111:	(a) Reason: D7I'T in the instruction cycle represents Register –reference instructions.
Answer 112:	(d) Reason: (r-1)'s complement of 345 in octal number system is 432.
Answer 113:	(e) Reason: SHRA stands for Arithmetic shift right.
Answer 114:	(d) Reason: Temporal Locality describe that the information which will be used in near future is likely to be in use already.
Answer 115:	(c) Reason: CISC stands for Complex Instruction Set Computer.
Answer 116:	(e)

	Reason: The three state gates in a digital circuit Logic 0, logic 1, high impedance
117	Answer: (d) Reason: The table that lists the required inputs for a given change of state is Excitation Table.
118	Answer: (c) Reason: Microphone is a Input device.
119	Answer: (b) Reason: Execution is the phase in which the programs must reside in the main memory.
120	Answer: (d) Reason: (x')' = x.

COMPUTER SYSTEM ARCHITECTURE QUESTIONS AND ANSWERS 121 TO 130

Computer System Architecture

Questions 121 To 130

121.	Of the following, what is a input device for which finger shows the cursor movement. (a) Mouse (b) Scanner (c) Trackball (d) Glide pad (e) Microphone.
122.	Which of the following describes the Mnemonic SPA? (a) Skip If (Accumulator) Positive (b) Skip If (Adder-Subtractor) Positive (c) Skip If (Associative Mapping) Positive (d) Skip If (Assembler) Positive (e) Skip If (Address Resister) Positive.
123.	Of the following, identify the memory usually written by the manufacturer. (a) RAM

	(b) ROM (c) DRAM (d) SRAM (e) Cache Memory.
124.	Consider that the program is executed from main memory until it attempts to reference a page that is still in auxiliary memory. Identify this condition. (a) Page Found (b) Page Fault (c) Page Hit (d) Page Miss (e) Page Replace.
125.	What is the symbol to represent a state in the state diagram?
126.	A computer has memory of 256k words of 32 bits each, how many bits are required to specify the address part? (a) 16 bits (b) 12 bits (c) 8 bits (d) 18 bits (e) 10 bits.
127.	**V** is a symbol for (a) OR (b) XOR (c) AND (d) NAND (e) NOR.

128.	What is represented by $D_7I'T$ in the instruction cycle? (a) Input-Output Instructions (b) Register–reference instructions (c) Program interrupt (d) Branch instruction (e) Memory Reference Instructions.
129.	What is described by the Mnemonic SHRA? (a) Arithmetic shift left (b) Logical shift right (c) Logical shift left (d) Arithmetic shift right (e) Circular shift right.
130.	CISC stands for: (a) Control Instruction Set Completeness (b) Complex Instruction Set Computer (c) Complex Instruction Set Conversion (d) Control Instruction Set Computer (e) Complex Instruction Set Control.

Answers

	Answer	Reason
121. D		Is the input device for which finger shows the cursor movement
122. A		SPA stands for Skip If (Accumulator) Positive
123. B		ROM is the memory usually written by the manufacturer.

124. B		The program is executed from main memory until it attempts to reference a page that is still in auxiliary memory called Page Fault.
125.	B	is the symbol which represent a state in the state diagram
126. A		A computer has memory of 256k words of 32 bits each, 18 bits are required to specify the address part.
127. A		**V** is a symbol for **OR**
128. B		$D_7I'T$ in the instruction cycle represents Register –reference instructions
129. D		SHRA stands for Arithmetic shift right
130. B		CISC stands for complex instruction set computer.

COMPUTER SYSTEM ARCHITECTURE SET 14

Questions 131 To 140

131.	Of the following phases, Identify the phase in which the programs must reside in the main memory. (a) Deletion (b) Printing (c) Execution (d) Reading (e) Insertion.
132.	What are the three state gates in a digital circuit? (a) Logic 0, Logic 1 Complement, high impedance (b) Logic 0 Complement, Logic 1, high impedance (c) Logic 0 Complement, Logic 1 Complement, high impedance (d) Logic 0, logic 1, Low impedance (e) Logic 0, logic 1, high impedance.
133.	Which of the following is **false** related to Stack? (a) Stack Pointer Points to the top most element of the stack (b) Only PUSH and POP operations are applicable (c) Implements FIFO (d) Useful for nested loops, subroutine calls etc., (e) Efficient for arithmetic expression evaluation.
134.	Which of the following is the method in which the unit receiving the data responds with another control signal? (a) Timing Sequence (b) Synchronous (c) Strobe (d) Short message service (e) Handshaking.
135.	Consider the following unsigned decimal numbers

	i. 6543 ii. 4444 Subtract (**i)** by taking the 10's complement of (**ii)** (a) 2098 (b) 2099 (c) 2096 (d) 2097 (e) 2095.
136.	(x')' = (a) x^2 (b) 0 (c) 1 (d) x (e) x'.
137.	Which of the following addressing modes specifies a register which contains the memory address of the operand? (a) Indirect Addressing Mode (b) Register Addressing Mode (c) Register Indirect Addressing Mode (d) Index Addressing Mode (e) Base Address Register Addressing Mode.
138.	What is the octal equivalent of given binary number? 011001 (a) 32 (b) 31 (c) 34 (d) 33 (e) 35.
139.	Which of the following is correct related to the circuit diagrams? (a) Sequential circuit is an interconnection of only logic gates (b) Sequential circuit is an interconnection of only flip flops (c) Combinational circuit is an interconnection of logic gates (d) Combinational circuit is an interconnection of flip flops (e) Part of a combinational circuit is a sequential circuit.
140.	What does D stands for in D-flip flop? (a) Direct (b) Don't care (c) Double (d) Delay (e) Data.

Answers

131.	**C**	Is the phase in which the programs must reside in the main memory.
132.	**E**	Is the three state gates in a digital circuit
133.	**C**	Stack does not Implement FIFO but implements LIFO
134.	**E**	Hand shaking is the method in which the unit receiving the data responds with another control signal

135	B	6543- 4444= 2099
136	D	(x')' = x
137	C	Register indirect addressing mode. Is the addressing mode that specifies a register which contains the memory address of the operand
138	B	The octal equivalent of 011001 =31
139	C	Combinational circuit is an interconnection of logic gates.
140	E	D stands in D-flip flop stands for Data

OMPUTER SYSTEM ARCHITECTURE SET 15

Questions 141 To 150

141.	Identify the term, which indicate a set of Logical Addresses. (a) Memory space (b) Disk space (c) Address space (d) Location (e) Page Frame.
142.	DMA stands for: (a) Direct Memory Address (b) Direct Main Address (c) Direct Memory Access (d) Direct Main Access (e) Device Memory Access.
143.	Consider DR ← M [AR], Identify the operation. (a) Arithmetic Operation (b) Shift Operation (c) Memory Write (d) Memory Read (e) Memory Cycle.
144.	What is the (r-1)'s complement of 345 in octal number system? (a) 342 (b) 234 (c) 243 (d) 423 (e) 432.
145.	Which of the following terms describe that the information which will be used in near future is likely to be in use already? (a) Spatial Locality (b) Locality (c) Hit ratio (d) Temporal Locality (e) Effective access time.
146.	What is the table that lists the required inputs for a given change of state? (a) Characteristic table (b) Truth table (c) Null table

	(d) Excitation table (e) Binary table.
147.	Microphone is a\an (a) Output device (b) Storage device (c) Input device (d) Processing device (e) Printing device.
148.	What is the operation sets to 1 the bits in one register where there are corresponding 1's in the second register? (a) Selective Complement (b) Selective Clear (c) Selective Set (d) Mask (e) Insert.
149.	Which one of the following can be called as a peripheral? (a) Control unit (b) Speakers (c) Arithmetic Unit (d) Logic unit (e) Main Memory.
150.	What is demonstrated in the given figure? (a) MICR (b) Bar Code Reader (c) Joy Stick (d) Track Ball (e) Wand Reader.

Answers

141C		Address spaces Indicate a set of Logical Addresses.
142C		DMA stands for Direct Memory Access
143D		DR ← M [AR] is Memory Read
144E		(r-1)'s complement of 345 in octal number system is 432
145D		Temporal Locality describe that the information which will be used in near future is likely to be in use already.
146D		Excitation table is the table that lists the required inputs for a given change of state
147C		Microphone is a Input device
148C		Selective Set is the operation sets to 1 the bits in one register where there are corresponding 1's in the second register
149B		Speakers can be called as a peripheral.
150B		Bar code reader.

COMPUTER SYSTEM ARCHITECTURE SET 16

Questions 151 To 160

151.	Which of the following binary number is equivalent to 20? (a) 10100 (b) 100 (c) 000010 (d) 11111 (e) 10111.
152.	The Hexadecimal number system has a radix of (a) 10 (b) 2 (c) 8 (d) 16 (e) 5.
153.	What is equivalent of -35_{10} in 8-bit 2's complement representation? (a) 01011101 (b) 11011111 (c) 11011101 (d) 00101101 (e) 11001101.
154.	The BCD equivalent of decimal number 32.94 is (a) 0011 0010 . 1001 0100 (b) 1011 0010 . 1001 0100 (c) 0011 0010 . 1001 0010 (d) 100010 . 1001 0100 (e) 0010 0010 . 1001 0010.
155.	The code which can represent numbers, characters, and special characters are called (a) Gray code (b) BCD code (c) EBCDIC code (d) Alphanumeric code (e) ASCII code.
156.	In a Hamming code for transmitting a data of 4-bit, how many parity bit(s) is/are used? (a) One (b) Two (c) Three (d) Four (e) Zero.
157.	The Boolean expression F = AB'C'D + AB'CD' + A'BCD can be written as (a) F = $\sum$m (7, 8, 9) (b) F = $\sum$m (7, 9, 10) (c) F = $\sum$m (7, 8, 10) (d) F = $\sum$m (7, 6, 10) (e) F = $\sum$m (6, 9, 10).
158.	The Boolean expression F(A,B,C,D) = $\sum$m(0, 3) is (a) (A + B + C' + D') (A + B + C + D) (b) (A + B'+ C' + D') (A'+ B'+ C' + D') (c) (A'+ B'+ C' + D') (A'+ B'+ C + D) (d) (A + B' + D') (A' + B + C + D')

	(e) (A + B + D') (A' + B' + C + D').
159.	In a Karnaugh map the adjacent minterms can be combined only if the configuration is (a) 2 (b) 4 (c) 2 x n (d) 2^n (e) 2^{n-1}.
160.	For realizing the Boolean expression AC + AD + BC + BD how many number of inputs are needed ? (a) 8 (b) 4 (c) 12 (d) 16 (e) 2.

Answers

Answer:	(a)
Reason :	10100 is the binary number which is equivalent to 20.
Answer:	(d)
Reason :	The Hexadecimal number system has a radix of 16.
Answer:	(c)
Reason :	The equivalent of -35_{10} in 8-bit 2's complement representation is 11011101.
Answer:	(a)
Reason :	The BCD equivalent of decimal number 32.94 is 0011 0010 .1001 0100.
Answer:	(d)
Reason :	The code which can represent numbers, characters, and special characters are called Alphanumeric code.
Answer:	(c)
Reason :	In a Hamming code for transmitting a data of 4-bit, three parity bits are used.
Answer:	(b)
Reason :	The Boolean expression F = AB'C'D + AB'CD' + A'BCD can be written as F = ∑m (7, 9, 10).
Answer:	(a)
Reason :	The Boolean expression F(A,B,C,D) =∑m(0, 3) is (A + B + C' + D') (A + B + C + D)
Answer:	(a)
Reason :	In a Karnaugh map the adjacent minterms can be combined only if the configuration of 2.
Answer:	(c)
Reason :	For realizing the Boolean expression AC + AD + BC + BD the number of inputs needed are 12.

COMPUTER SYSTEM ARCHITECTURE SET 17

Questions 161 To 170

161.	Using Karnaugh map SOP form of the expression (B + C + D) (B' + C + D') (A' + B + C' + D') (A + B' + E') (A + B' + D') will be (a) BCD + B'CD + A'BC'D' + AB'E' + AB'D' (b) B'C'D' + BC'D + AB'CD + A'BE' + A'BD (c) B'C'D + A'B'C + ABC + BD'E' + ACD' + ABD' (d) B'C'D' + BCD + AB'CD + A'BE + A'BD

	(e) BCD + B'C'D + A'BCD' + ABE + AB'D'.
162.	The number of input variables which a NOT gate can have is (a) One (b) Two (c) Three (d) Four (e) Any number.
163.	The unique output for a NAND logic gate is a 0 (a) When all inputs are 0 (b) When all the inputs are 1 (c) When any one input is 0 (d) When any one input is 1 (e) All of the above.
164.	The states of a bus may be (a) Logic 0, logic 1 and Low impedence (b) Logic 0, logic –1 and high impedence (c) Logic –2, logic –1 and high impedence (d) Logic –1, logic 1 and high impedence (e) Logic 0, logic 1 and high impedence.
165.	The binary pattern 101110 is an answer received after adding two numbers in a 6-bit two's complement system. The answer in decimal system is (a) – 45 (b) – 44 (c) – 18 (d) – 13 (e) + 45.
166.	A 4-bit ALU which is based on 1'complement arithmetic is used to do the following addition. 1101 +1011 The answer should be: (a) Range overflow (b) 16 (c) –16 (d) 8 (e) 24.
167.	Using Boolean algebra the reduced expression for function AB'C + ABC can be realized by using how many number of gates? (a) 7 (b) 3 (c) 2 (d) 11 (e) 8.
168.	RISC stands for (a) Reduced Instruction Sign Computers (b) Reduced Instruction Set Computers (c) Reduced Instruction Set Carry (d) Reduced Invalid Set Computers (e) Reset Instruction Set Computers.

169.	A binary system based on Two's complement arithmetic gives the answer 110010. The decimal equivalent(s) of this answer is (a) 13 (b) –13 (c) –16 (d) –18 (e) –14.
170.	Which of the following statement is **false**? (a) Combinational circuits has memory (b) Sequential circuits has memory (c) Sequential circuits is a function of time (d) Combinational circuits does not require feed back paths (e) Sequential circuits require feed back paths.

Answers

Answer:	(c)
Reason :	Using Karnaugh map SOP form of the expression (B + C + D) (B' + C + D') (A' + B + C' + D') (A + B' + E') (A + B' + D') will be B'C'D + A'B'C + ABC + BD'E' + ACD' + ABD'.
Answer:	(a)
Reason :	The number of input variables which a NOT gate can have is One.
Answer:	(b)
Reason :	The unique output for a NAND logic gate is a 0 when all the inputs are 1.
Answer:	(e)
Reason :	States of bus may be Logic 0,logic 1 and high impedence
Answer:	(c)
Reason :	The binary pattern 101110 is an answer received after adding two numbers in a 6-bit two's complement system. The answer in decimal system is – 18.
Answer:	(a)
Reason :	The answer results in Range overflow when a 4-bit ALU which is based on 1'complement arithmetic is used to the addition 1101 + 1011.
Answer:	(b)
Reason :	The function AB'C + ABC can be realized by using 3 gates.
Answer:	(a)
Reason :	The equivalent binary number of 11.8125_{10} is 1011.1101.
Answer:	(b)
Reason :	The decimal equivalent of 110010 based on Two's complement arithmetic is –13.
Answer:	(a)
Reason :	Combinational circuits has memory.

COMPUTER SYSTEM ARCHITECTURE SET 18

Questions 171 to 180

171.	Which of the following is responsible for coordinating various operations using timing signals? (a) Arithmetic-logic unit (b) Control unit

	(c) Memory unit (d) Input unit (e) Output unit.
172.	What kind of Information is stored inside the computer? (a) Binary form (b) ASCII code form (c) Decimal form (d) Alpha numeric (e) Numeric form.
173.	A parity bit (a) Is used to indicate uppercase letters (b) Is used to detect errors (c) Is the first bit in a byte (d) Is the last bit in a byte (e) Is used to indicate lowercase letters.
174.	A four input multiplexer has inputs A, B, C and D and select lines S_0 and S_1. Which of the following statement(s) where the output F is given by Which of the above statements is/are **true**? (a) Only (I) above (b) Only (II) above (c) Only (III) above (d) Both (I) and (II) above (e) Both (II) and (III) above.

175.	Consider the following Karnaugh map: Which of the following is the most compact form of Boolean expression which corresponds to the map? .
176.	What do you call the given statement as? “The information which will be used in near future is likely to be in use already is” (a) Spatial Locality (b) Locality (c) Hit ratio (d) Temporal Locality (e) Effective access time.
177.	In which page replacement algorithm where there is a replacement of a page, which will not be used for the longest period of time? (a) MFU (b) LRU (c) OPT (d) FIFO (e) LFU.
178.	Which of the following is supplied by one unit to indicate to other unit when the transfer has to occur? (a) Strobe pulse (b) Time slice (c) Access right (d) Logic gate (e) Program.

179.	A Set of Logical Addresses as is called (a) Memory space (b) Disk space (c) Address space (d) Location (e) Pages.
180.	Which of the following can be used for checking errors in transmission? (a) Full duplex (b) Half duplex (c) CRC (d) Full adder (e) Binary adder.

Answers

Answer 171. :	(b)
Reason :	Arithmetic-logic unit is responsible for coordinating various operations using timing signals.
Answer 172. :	(a)
Reason :	The data inside a computer is represented in Binary form i.e (0's and 1's).
Answer 173. :	(b)
Reason :	A parity bit is used to detect errors.
Answer 174. :	(d)
Reason :	only (I) and (II) are correct.
Answer 175. :	(a)
Reason :	The most compact form of Boolean expression which corresponds to the map is
Answer 176. :	(d)

Reason :	The information which will be used in near future is likely to be in use already is Temporal Locality
Answer: 177.	(c)
Reason :	The page replacement algorithm where thee is a replacement of a page ,which will not be used for the longest period of time is OPT
Answer: 178.	(a)
Reason :	A Strobe pulse is supplied by one unit to indicate the other unit when the transfer has to occur
Answer: 179.	(c)
Reason :	A Set of Logical Addresses is called Address Space.
Answer: 180.	(c)
Reason :	CRC is used for checking errors in transmission.

COMPUTER SYSTEM ARCHITECTURE SET 19

Questions 181 To 190

181.	The computer architecture having stored program is _____. (a) Harvard (b) Von-Neumann (c) Pascal (d) Ada (e) Cobol.
182.	The key technology used in IV generation computers is _____. (a) MSI (b) SSI (c) LSI &VLSI (d) Transistors (e) Vacuum Tubes.
183.	**x** and **y** are two digit BCD numbers. It is known that **x + y** is equal to **82(BCD)** and **x - y** is equal to**04(BCD)**. The value of x is _____. (a) 01000011 (b) 00001010 (c) 00101011 (d) 00100111 (e) 00110010.
184.	The gray code of a given binary number 1001 is (a) 1110 (b) 0110 (c) 1101 (d) 1111 (e) 0000.
185.	When the addition of two +ve numbers results in a –ve value, then _____ flag will be set. (a) Over-flow (b) Carry (c) Parity (d) E (e) Sign.
186.	The digital circuit that generates the arithmetic sum of two binary numbers of any length is _____ . (a) Binary-Adder (b) Full-Adder (c) Half-Adder (d) Adder (e) OR-gate.
187.	Which of the following representation requires the least number of bits to store the number +255? (a) BCD (b) 2's complement (c) 1's complement (d) Unsigned binary (e) Signed binary.

188.	The number of select input lines in an 8-to-1 multiplexer is _____.
(a)	1 (b) 8 (c) 2 (d) 4 (e) 3.
189.	If F= AB' + C'D then F'= _____.
(a)	(A+B')(C'+D) (b) (A'B)+(CD') (c) (AB')(CD')
(d)	(A'+B)(C+D') (e) (A'+B)+(C+D').
190.	Serial to parallel data conversion is done using
(a)	Accumulator (b) Shift Register (c) Counter
(d)	CPU (e) Control Unit.

Answers

181.	Answer : (b) Reason : The first computer architecture having stored program is Von-Neumann
182.	Answer : (c) Reason : Large-scale integrated and very large-scale integrated circuits are used in the IV generation.
183.	Answer : (a) Reason : The x value is 01000011
184.	Answer : (c) Reason : The gray code of 1001 is 1101
185.	Answer : (a) Reason : Over –flow flag will be set .
186.	Answer : (a) Reason : The binary adder is used to add binary numbers of any length
187.	Answer : (d) Reason : Unsigned binary representation occupies less space to store the number +255.
188.	Answer : (e) Reason : If 2^n data inputs lines are connected to a MUX then there will be n Selection lines. For 8-to -1 MUX 2^3 input lines and 3 selection lines are possible
189.	Answer : (d) Reason : The complement of AB' +C'D is (A'+B) (C+D')
190.	Answer : (b) Reason : Shift registers are used for serial to parallel data. Conversion.

COMPUTER SYSTEM ARCHITECTURE SET 20

Questions 191 to 200

191.	What does D stand for in a D flip-flop?
(a)	Direct (b) Don't care (c) Data (d) Device (e)

	Disk.
192.	Which of the following is **not** an advantage of asynchronous circuits? (a) Higher speed (b) Low power consumption (c) Smaller design effort (d) No need to provide clock generation circuitry (e) Simple functions.
193.	Carry in half-adder can be obtained using _____. (a) X-OR gate (b) AND gate (c) OR gate (d) X-NOR gate (e) Inverter.
194.	CACHE memory is implemented using _____. (a) Dynamic RAM (b) Static RAM (c) EA RAM (d) ED RAM (e) EP RAM.
195.	CISC stands for _____. (a) Control Instruction Set Completeness (b) Complex Instruction Set Conversion (c) Complex Instruction Set Computer (d) Control Instruction Set Conversion (e) Complex Instruction Set Control.
196.	BUN instruction stands for_____ (a) Branch conditionally (b) Branch unconditionally (c) Boot unconditionally (d) Begin unconditionally (e) Branch and save return address.
197.	Information transfer from one register to another is designated in symbolic form by means of _____. (a) Control functions (b) OP-Code (c) Registers (d) Stack operation (e) Replacement operator.
198.	DMA stands for_____. (a) Direct Memory Address (b) Direct Main Address

(c)	Direct Memory Access (d) Direct Main Access
(e)	Device Memory Access.
199.	_____ is a symbol to denote a part of a register.
(a)	{ } (b) ( ) (c) < >
(d)	à (e)
200.	_____ structure is useful in the evaluation of postfix arithmetic expression.
(a)	Stack (b) Queue (c) Linked List (d) Graph (e) Tree.

Answers

200(a)

191-c
192-a
193-d
194-b
195-c
196-b
197-b
198-c

COMPUTER SYSTEM ARCHITECTURE SET 21

Questions 201 To 210

201.	When a large number of registers is included in the CPU, it is most efficient to connect them through a _____.
(a)	ALU (b) Memory Register (c) STACK
(d)	QUEUE (e) Bus system.
202.	The register that keeps track of the address of next instruction to be executed is _____ .
(a)	AC (b) PC (c) IR (d) AR (e) DR.
203.	The correspondence between the main memory blocks and those in the cache is specified by _____.
(a)	Miss penalty (b) Replacement algorithms (c) Hit rate

(d)	Page fault (e) Mapping functions.
204.	Which one of the following can be called as a peripheral?
(a)	Control unit (b) Arithmetic unit (c) Speaker
(d)	Logic unit (e) Main memory.
205.	The set of physical addresses is called
(a)	Disk Space (b) Address Space (c) Pages
(d)	Frames (e) Location.
206.	The device that is allowed to initiate data transfer on the bus is called _____.
(a)	Bus master (b) Bus arbitration (c) Bus cycle
(d)	Bus request (e) Parallel bus.
207.	The DMA transfer technique where transfer of one word data at a time is called _____.
(a)	Cycle stealing (b) Memory stealing (c) Hand-shaking
(d)	Inter-leaving (e) Bus stealing.
208.	_____ interface is used to connect the processor to I/O devices that require transmission of data one bit at a time.
(a)	Parallel (b) Serial (c) Output (d) Input (e) Bus.
209.	In based addressing mode, instruction contains _____.
(a)	Base address (b) Displacement (c) Absolute address
(d)	Relative address (e) Indirect address.
210.	A hand-shake based protocol for data transfer is an example of _____ type of data transfer.
(a)	Synchronous (b) Asynchronous (c) Serial
(d)	Parallel (e) Indirect.

Answers

201.	Answer : (a) Reason : All registers in a CPU are connected through ALU..
202.	Answer : (b) Reason : Program Counter contains the address of the next instruction to be executed..
203.	Answer : (e) Reason : The corresponding between the main memory blocks and those in the cache is specified by a mapping function, because the basic characteristic of cache memory is fast access time. Therefore, very little or no time must be wasted when searching for words in the cache.
204.	Answer : (c) Reason : **Speakers** can be called as a peripheral as all others are part of the system.
205.	Answer : (b) Reason : The collection of address spaces in a physical memory is called address space.
206.	Answer : (a) Reason : The Bus master is allowed to initiate data transfer on the bus.
207.	Answer : (a) Reason : Transfer of one word data at a time using DMA transfer technique is called Cycle Stealing.

208.	Answer : (b) Reason : Serial interface transfers one bit at a time, whereas others can handle more than one bit.
209.	Answer : (b) Reason : In a based addressing mode the displacement is the address field.
210.	Answer : (b) Reason : Asynchronous data transfer

COMPUTER SYSTEM ARCHITECTURE SET 22

Questions 211 to 220

211.	_____bits are used to denote a character. (a) 16 (b) 7 (c) 2 (d) 8 (e) 32.
212.	The fastest processor chips today have an internal clock rate of at least _____. (a) 100 MHZ (b) 200 MHZ (c) 400 MHZ (d) 250 MHZ (e) 300 MHZ.
213.	Octal number 736.4 is converted to decimal as (a) $(475.5)_{10}$ (b) $(479.5)_{10}$ (c) $(478.5)_{10}$ (d) $(476.3)_{10}$ (e) $(477.5)_{10.}$
214.	Conversion of the decimal 41.6875 into binary number will be (a) 110001.1101 (b) 10000.1011 (c) 101001.1011 (d) 101101.1011 (e) 101111.1011.
215.	The addition of two binary numbers in 2's complement x=1010100 and y=1000011 (a) 11010110 (b) 11110011 (c) 01111011 (d) 10010001 (e) 11000111.
216.	Floating point is always interpreted to represent a number in the following form (a) $M * r^e$ (b) $M^e * r$ (c) $E^r * m$ (d) M * e (e) $E^m * r$.
217.	If 1's are mapped in a k-map the Boolean function is in the form (a) Sum of products (b) Product of sums (c) Subtraction and divide (d) Addition and subtraction (e) Sum of sums.
218.	A combinational circuit that performs the addition of two input bits and a carry from

	the previous lower significant position is called (a) Full-adder (b) Half-adder (c) Full-subtractor (d) Half-subtractor (e) Full-Divider.
219.	Which of the following gates is called as a universal gate as any digital system can be implemented with it? (a) AND gate (b) NAND gate (c) OR gate (d) SR gate (e) XOR gate.
220.	A combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines is (a) Decoder (b) Encoder (c) Full adder (d) Half adder (e) Half-Subtractor.

Answers

211.	Answer : (d) Reason : Every character is represented with 8 bits in the main memory
212.	Answer : (c) Reason : The fastest processor chips today have an internal clock of at least 200MHZ
213.	Answer : (c) Reason : $7*8^2+3*8^1+6*8^0+4*8^{-1}$ $=7*64+3*8+6*1+0.5$ $=448+24+6+0.5$ $=478.5$
214.	Answer : (c) Reason : The binary equivalent of 41.6875 is $(101001.1011)_2$
215.	Answer : (d) Reason : x= 1010100 The 2's complement of y is 0111101 ----------

	10010001
216.	Answer : (a) Reason : Floating point is always interpreted to represent a number in the following form $M*r^e$
217.	Answer : (a) Reason : To get the Boolean function in sum of products form we should group 1's in the k-map.
218.	Answer : (a) Reason : Two inputs are directed, one towards XOR gate and towards AND gate and also a combinational circuit that performs the addition o two input bits.
219.	Answer : (b) Reason : NAND gate is generally called as universal gate.
220.	Answer : (a) Reason : Decoder uses address inputs as binary numbers and produces output signal on.

COMPUTER SYSTEM ARCHITECTURE SET 23

Questions 221 to 230

221.	The outputs of sequential circuits are functions of (a) External inputs (b) Present state of flip-flops (c) Next state of the flip-flop (d) External outputs (e) Logic gates.
222.	In which type of flip-flop the intermediate condition of the SR flip-flop(When S=R=1) is eliminated? (a) Edge-triggered flip-flop (b) JK flip-flop (c) D flip-flop (d) S flip-flop (e) T flip-flop.
223.	How many flip-flops make up a register of 8 bits? (a) 6 (b) 7 (c) 8 (d) 16 (e) 32.
224.	What is the maximum count achieved by a counter with four flip-flops? (a) 10 (b) 15 (c) 9 (d)

16 (e) 8.

225. Given the characteristic table of a JK flip-flop. Find the missing output value

J	K	Q(t +1)
0	0	Q(t)
0	1	0
1	0	1
1	1	---

(a) Q(t) (b) Q'(t + 1) (c) 1 (d) Q'(t) (e) 0.

226. Which of the following digital circuit is called a data selector?

(a) Multiplexer (b) De-multiplexer (c) Half-adder

(d) Full-adder (e) Decoder.

227. Information transfer from one register to another in designated in symbolic form by means of a _____

(a) Control functions (b) OP-Code (c) Registers

(d) Stack operation (e) Replacement operator.

228. The control condition is terminated with a _____.

(a) Comma (b) Semicolon (c) Colon (d) Hash (e) Dot.

229. _____ is the address of the operand in a computation-type instruction or the target address in a branch type instruction.

(a) Indirect address (b) Effective address (c) Branch address

(d) Return address (e) Direct address.

230. Stack is a _____list.

(a) FIFO (b) LIFO (c) FILO (d) OFLI (e) LFIO.

Answers

221.	Answer : (b) Reason : The present state of a flip-flop is generally the outputs of a sequential circuit.
222.	Answer : (b) Reason : In RS flip-flop two new connections from Q and Q' back to original input gates eliminate the intermediate condition.
223.	Answer : (c) Reason : 8 flip-flops require to make up a register of 8 bits.
224.	Answer : (b) Reason :
225.	Answer : (d) Reason : 15 is the maximum count achieved by the counter with 4 flip-flops.
226.	Answer : (a) Reason : Complement state of Q(t)
227.	Answer : (e) Reason : A replacement operator consist of the information transfer from one register to another is designated in symbolic form
228.	Answer : (c) Reason : The control condition is terminated with a colon
229.	Answer : (b) Reason : Effective address is the address of the operand in a computation-type instruction or the target address in a branch type instruction.
230.	Answer : (b) Reason : The Stack is opened only one end. The operation of a Stack is Last In First Out.

COMPUTER SYSTEM ARCHITECTURE SET 24

Questions 231 To 240

231.	When a large number of registers are included in the CPU, it is most efficient to

	connect then through a _____. (a) ALU (b) Memory Register (c) STACK (d) QUEUE (e) Bus system.
232.	The ROM position of main memory is needed for storing an initial program is called_____. (a) BOIS (b) Bootstrap loader (c) Flash (d) Complier (e) Assembler.
233.	The correspondence between the main memory blocks and those in the cache is specified by a _____. (a) Miss penalty (b) Replacement algorithms (c) Hit rate (d) Page fault (e) Mapping functions.
234.	Techniques that automatically move programs and data blocks into the physical memory when they are required for execution are called _____. (a) Associative mapping (b) Main memory (c) Virtual memory (d) Cache memory (e) Logical memory.
235.	Virtual memory is used to increase the apparent size of the _____memory. (a) Secondary (b) Main (c) Auxiliary (d) Associative (e) Cache.
236.	The device that in allowed to initiate data transfer on the bus is called _____. (a) Bus Master (b) Bus Arbitration (c) Bus cycle (d) Bus request (e) Parallel Bus.
237.	The routine executed in response to an interrupt request is called _____routine. (a) Sub-routine (b) Interrupt acknowledge (c) Vectored interrupt (d) Serial interrupt (e) Interrupt Service.
238.	_____ interface is used to connect the processor to I/O devices that require transmission of data one bit at a time. (a) Parallel (b) Serial (c) Output (d) Input (e) Bus.
239.	The selected target controller responds by asserting (a) DB6 (b) SEL (c) DB5 (d) DB8 (e) BSY.
240.	_____ technique allows the DMA controller to transfer one data word at a time after which must return control of the buses to the CPU. (a) Cycle stealing (b) Bus stealing (c) Memory stealing (d) Burst transfer (e) Bus controlling.

Answers

231.	Answer : (a)
Reason :	Bus system connect different component s whereas ALU performs arithmetic and logical calculations and memory register is for storage purpose.
232.	Answer : (b)
Reason :	ROM portion of main memory is needed for storing an initial program is called Boot Strap Loader program. It will load

	operating system files from disk to main memory.
233.	Answer : (e)
Reason :	The corresponding between the main memory blocks and those in the cache is specified by a mapping function, because the basic characteristic of cache memory is fast access time. Therefore, very little or no time must be wasted when searching for words in the cache.
234.	Answer : (c)
Reason :	A virtual memory system provides a mechanism for translating program generated address into correct main memory locations. This is done dynamically, while programs are being executed in the CPU. The translation or mapping is handled automatically by the hardware by means of a mapping table.
235.	Answer : (b)
	Reason : Virtual memory is used to increase the apparent size of the main memory.
236.	Answer : (a)
	Reason : The Bus master is allowed to initiate data transfer on the bus.
237.	Answer : (e)
	Reason : Interrupt service routine is executed in response to an interrupt request.
238.	Answer : (b)
	Reason : Serial interface transfers one bit at a time, whereas others can handle more than one bit.
239.	Answer : (e)
	Reason : BSY is the selected target controller responds by asserting.
240.	Answer : (a)
Reason :	Cycle Stealing is the technique allows the DMA controller to transfer 1 data word at a time, after which must return control of the buses to the CPU.

COMPUTER SYSTEM ARCHITECTURE SET 25

Questions 241 To 250

241.	Specify the Complement for the equation, F=AB+C'D'+B'D.` (a) (A+B')(C'+D)(B+D') (b) (A'+B')(C+D)(B+D') (c) (A'+B')(C'+D')+(B+D') (d) (A'+B')+(C+D)+(B'+D) (e) (A'+B')(C'+D')(B+D').
242.	Identify the input device in which finger shows the cursor movement. (a) Mouse (b) Scanner (c) Glide pad (d) Microphone (e) Trackball.
243.	Name the keyword to specify the number of pixels displayed on the screen. (a) Cell (b) Color depth (c) Monitor size (d) Resolution (e) Refresh rate.
244.	Subtract the given unsigned decimal numbers by taking the 10's complement of the subtrahend. 5250 - 1321 (a) 3928 (b) 3828 (c) 3929 (d) 3927 (e) 3729.

245.	From the given k-map, give the simplified equation for F. (a) D + B'C (b) D'+BC (c) D + B'C' (d) D + BC' (e) D + BC.
246.	If XY = 0 then what is the value of X Y ? (a) X (b) Y (c) (X'+Y') (d) (X+Y) (e) XY.
247.	Specify the hexadecimal equivalent of a decimal number , 10. (a) A (b) B (c) C (d) D (e) E.
248.	Identify the 2's complement of 101010101. (a) 010101010 (b) 101010101 (c) 010101000 (d) 110101011 (e) 010101011.
249.	Name the operation represented by . (a) OR (b) AND (c) XOR (d) COMPLEMENT (e) NOR.
250.	Which one of the following instructions represents . (a) Memory reference (b) Register reference (c) I/O instruction (d) A and C above (e) None of the above.

Answers

241.	Answer : (b)
Reason:	As OR gates becomes AND gates & values change to their complements F' = (A'+B)(C+D)(B+D').
242.	Answer : (c)
Reason:	Glide pad is a input device for which finger shows the cursor movement.
243.	Answer : (d)
Reason:	Resolution is the number of pixels displayed on the screen.
244.	Answer : (c)
Reason:	10's complement as 1321 = 8679 5250 + 8679 3929 – discard the carry.
245.	Answer : (a)
Reason:	Simplify eight 1's grouped toget D and remaining four 1's to get B'C D + B'C.
246.	Answer : (d)
Reason:	If XY = 0 X Y = X + Y.
247.	Answer : (a)
Reason:	The Hexadecimal equivalent of a decimal number, 10 is A.
248.	Answer : (e)
Reason:	2's complement of 101010101 is 010101011.
249.	Answer : (b)
Reason:	' denotes AND.
250.	Answer : (b)

Reason:	As 15th bit is 0 and Opcode 111 Register reference.

COMPUTER SYSTEM ARCHITECTURE SET 26

Questions 251 To 260

251.	Specify the expansion for ISZ. (a) Invalid to skip if Zero (b) Increment and set if Zero (c) Increment and sign if Zero (d) Increment and skip if Zero (e) Increment and save if Zero.
252.	Only Push and Pop operations are applicable to which one of the following. (a) Queue (b) Tree (c) Stack (d) Array (e) Table.
253.	Identify the addressing mode, which has instruction specifying a register which contains the memory address of the operand. (a) Register mode (b) Direct addressing mode (c) Relative addressing mode (d) Indirect addressing mode (e) Register indirect mode.
254.	Specify the Mnemonic SHRA description. (a) Arithmetic shift right (b) Arithmetic shift left (c) Logical shift right (d) Logical shift left (e) Circular shift right.
255.	Identify the expansion for RISC. (a) Reduced Instruction Sign Computers (b) Reduced Instruction Set Computers (c) Reduced Instruction Set Carry (d) Reduced Invalid Set Computers (e) Reset Instruction Set Computers.
256.	What are the states of a bus in a computer system? (a) Logic 0,logic 1 and low impedence (b) Logic 0,logic -1 and high impedence (c) Logic -2,logic -1 and high impedence (d) Logic -1,logic 1 and high impedence (e) Logic 0,logic 1 and high impedence.
257.	Which one of the following gives the information about, the data used in near future is likely to be in use already? (a) Spatial locality (b) Locality (c) Hit ratio (d) Temporal locality (e) Effective access time.
258.	What is the page replacement algorithm where thee is a replacement of a page ,which will not be used for the longest period of time? (a) MFU (b) LRU (c) OPT (d) FIFO (e) LFU.
259.	Which one of the following is supplied by one unit to indicate the other unit when the transfer has to occur? (a) Strobe pulse (b) Time slice (c) Access right (d) Logic

	gate (e) Program.
260.	Specify, what is a Set of Logical Addresses? (a) Memory space (b) Disk space (c) Address space (d) Location (e) Pages.

Answers

251.	Answer : (d)
Reason:	ISZ means increment and skiping zero
252.	Answer : (c)
Reason:	Stack has Push and POP operations.
253.	Answer : (e)
Reason:	It is Register indirect mode as the memory address is stored in the register.
254.	Answer : (a)
Reason:	SHRA discribes Arithmetic Shift Right.
255.	Answer : (b)
Reason:	RISC stands for Reduced Instruction Set Computers.
256.	Answer : (e)
Reason:	The status as a bus is Logic 0,logic 1 and high impedence.
257.	Answer : (d)
Reason:	Temporal Locality specifies the information which will be used in near future is likely to be in use already.
258.	Answer : (c)
Reason:	OPT is the algorithm where there is a replacement of a page, which will not be used for the longest period of time.
259.	Answer : (a)
Reason:	Strobe pulse is supplied by one unit to indicate the other unit when the transfer has to occur.
260.	Answer : (c)
Reason:	A Set of Logical Addresses is called Address spece.

COMPUTER SYSTEM ARCHITECTURE SET 27

Questions 261 To 270

261.	Which one of the following is a memory whose duty is to store most frequently used data? (a) Main memory (b) Cache memory (c) ROM (d) Auxiliary memory (e) PROM.
262.	What is demonstrated in the given figure? (a) MICR (b) Bar Code Reader (c) Joy Stick (d) Track Ball (e) Wand Reader.
263.	How many bytes equals Petabyte (PB)?

	(a) Quadrillion (b) Million (c) Trillion (d) Billion (e) 1000.
264.	What is stored in the Stack Pointer? (a) Operations (b) Addressing method (c) Stack data values (d) Address of top item (e) Address of next instruction.
265.	Which one of the following is used to specify the floating point representation? (a) $r+m^e$ (b) $m*r$ (c) $r*m^e$ (d) $m+r^e$ (e) $m*r^e$.
266.	Name the organization in which, the control information is stored in the control memory to initiate the required sequence of micro-operations. (a) Computer (b) Hardwired (c) Internal (d) Microprogrammed (e) Control.
267.	Identify the method in which the unit receiving the data responds with another control signal. (a) Handshaking (b) Timing sequence (c) Synchronous (d) Strobe (e) Short message service.
268.	Which one of the following can be used for checking errors in transmission? (a) Full duplex (b) Half duplex (c) CRC (d) Full adder (e) Binary adder.
269.	Name the gate given in the diagram. (a) AND gate (b) OR gate (c) NAND gate (d) Inverted AND gate (e) Inverted OR gate.
270.	Which of the following can be called as universal gate? (a) NOT (b) NOR (c) OR (d) AND (e) XOR.

Answers

261.	Answer : (b)
Reason:	Cache memory is a memory whose duty is to store most frequently used data.
262.	Answer : (b)
Reason:	Bar Code Reader is shown in the figure.
263.	Answer : (a)
Reason:	Petabyte (PB) is about 1 Quadrillion bytes.
264.	Answer : (d)
Reason:	Stack Pointer stores Address of top item.
265.	Answer : (e)
Reason:	Floating point number has $m*r^e$ i.e. mantissa is multiplied by dadix to the power of exponent.
266.	Answer : (d)
Reason:	In a Microprogrammed organization, the control information is stored in the control memory to initiate the required

	sequence of micro-operations.
267.	Answer : (a)
Reason:	The method in which the unit receiving the data, responds with another control signal is referred as Handshaking.
268.	Answer : (c)
Reason:	CRC – Cyclic Redundancy Check can be used for checking errors in transmission.
269.	Answer : (d)
Reason:	The figure represents Inverted AND gate.
270.	Answer : (b)
Reason:	NOR is a universal gate.

COMPUTER SYSTEM ARCHITECTURE SET 28

Questions 271 To 280

271.	According to the Demorgan's Theorem, what is the value of F', where F=P'Q+RS. (a) (P+Q')(R'+S') (b) (P'+Q')(R'+S') (c) (P+Q')(R+S) (d) (P+Q)(R'+S') (e) (P'+Q')(R'+S).
272.	_____ is a input device, which involves to demonstrate speech recognition. (a) Speakers (b) Scanner (c) Light pen (d) Microphone (e) CD-Player.
273.	Identify the circuit which gives one output from n number of inputs. (a) Demultiplexer (b) Multiplexer (c) Decoder (d) Encoder (e) Sequential Circuit.
274.	Subtract the given unsigned decimal numbers by taking the 10's complement of the subtrahend. 6543-4444. (a) 2098 (b) 2099 (c) 2096 (d) 2097 (e) 2095.
275.	From the given k-map, the simplified equation for F is _____. (a) ac+ab' (b) a'c+ab (c) a'c+ab' (d) a'c'+ab' (e) a'c+a'b'.
276.	Simplify AB+AB'. (a) A (b) B (c) (A'+B') (d) (A+B) (e) AB.
277.	The octal number of 011001 is _____. (a) 32 (b) 31 (c) 34 (d) 33 (e) 35.
278.	The 10's complement of 9999 is _____. (a) 9999 (b) 0000 (c) 1111 (d) 0001 (e) 1000.
279.	Which of the following depicts the figure below 15 14 13 12 11 0 1 1 1 1

	(a) Register reference instruction (b) I/O (c) Memory reference C (d) A and (e) A or C.
280.	Identify the formula for XNOR gate. (a) A'B+B'A (b) A'B'+AB (c) A+B (d) A.B (e) A'B.

Answers

271.	Answer : (a) Reason: According to the Demorgan's Theorem , the value of F', where F=P'Q+RS is (P+Q')(R'+S').
272.	Answer : (d) Reason: Microphone is a input device , which involves to demonstrate speech recognition.
273.	Answer : (b) Reason: The circuit which gives one output from n number of inputs is Multiplexer.
274.	Answer : (b) Reason: The subtraction of given unsigned decimal numbers by taking the 10's complement of the subtrahend , 6543-4444 is 2099.
275.	Answer : (c) Reason: From the given k-map, the simplified equation for F is a'c+ab'
276.	Answer : (a) Reason: AB + AB' = A(B + B') = A.
277.	Answer : (b) Reason: The octal number of 011001 is 31.
278.	Answer : (d) Reason: The 10's complement of 9999 is 0001.
279.	Answer : (b) Reason: The figure depicts Input output instruction as the last four bits are 1's.
280.	Answer : (b) Reason: The formula for XNOR gate is A'B'+AB.

COMPUTER SYSTEM ARCHITECTURE SET 29

Questions 281 To 290

281.	Name the addressing mode, which involves PC content to know the address of the operand. (a) Implied Mode (b) Relative addressing mode (c) Indirect addressing mode (d) Register Indirect mode (e) Immediate mode.
282.	The Mnemonic SPA describes _____. (a) Skip If (Address Resister) Positive (b) Skip If (Accumulator) Positive

	(c) Skip If (Adder-Subtractor) Positive (d) Skip If (Associative Mapping) Positive (e) Skip If (Assembler) Positive.
283.	The states of a bus may be as follows (a) Logic 0,logic 1 and Low impedence (b) Logic 0,logic -1 and high impedence (c) Logic 0,logic 1 and high impedence (d) Logic -2,logic -1 and high impedence (e) Logic -1,logic 1 and high impedence.
284.	Acronym for CAR is (a) Control Address Register (b) Content Address Register (c) Control Adder Register (d) Control Address Routine (e) Cache Address Register.
285.	The page replacement algorithm where there is a replacement of a page ,which has not been used more frequently is _____. (a) MFU (b) LRU (c) OPT (d) FIFO (e) LFU.
286.	A _____is supplied by one unit to indicate the other unit when the transfer has to occur. (a) Time slice (b) Access right (c) Logic gate (d) Strobe pulse (e) Program.
287.	A page frame is also called as _____. (a) Page (b) Block (c) Disk (d) Hit (e) Print document.
288.	demonstrates _____. (a) Glide Pad (b) Joy Stick (c) Bar Code Reader (d) Mouse (e) Wand Reader.
289.	1 GB is _____bytes. (a) 1 073 741 826 (b) 1 073 741 828 (c) 1 073 741 821 (d) 1 073 741 822 (e) 1 073 741 824.
290.	Stack Pointer stores _____. (a) Address of top item (b) Operations (c) Addressing Method (d) Stack data values (e) Address of next instruction.

Answers

281.	Answer : (b) Reason: The addressing mode, which involves PC content to know the address of the operand is Relative addressing mode.
282.	Answer : (b) Reason: The Mnemonic SPA describes Skip If (accumulator) Positive.
283.	Answer : (c) Reason: The states of a bus may be Logic 0,logic 1 and high impedance.
284.	Answer : (a) Reason: Acronym for CAR is Control Address Register.
285.	Answer : (e)

Reason:	The page replacement algorithm where there is a replacement of a page ,which has not been used more frequently is Least Frequently used.
286.	Answer : (d)
Reason:	A Strobe pulse _____is supplied by one unit to indicate the other unit when the transfer has to occur.
287.	Answer : (b) Reason: A page frame is also called as Block.
288.	Answer : (b) Reason: demonstrates joy stick
289.	Answer : (e) Reason: 1 GB is 1 073 741 824 bytes.
290.	Answer : (a) Reason: Stack Pointer stores Address of top item.

COMPUTER SYSTEM ARCHITECTURE SET 30

Questions 291 To 300

291. Name the binary code where there is only one bit of difference between two consecutive numbers.

(a) Excess-3 code (b) EBCDIC code (c) ASCII code
(d) Gray code (e) 2421 code.

292. Which one of the following is **correct**?

(a) Sequential circuit is an interconnection of only logic gates
(b) Sequential circuit is an interconnection of only flip flops
(c) Combinational circuit is an interconnection of logic gates
(d) Combinational circuit is an interconnection of flip flops
(e) Part of a combinational circuit is a sequential circuit.

293. SC←0, specifies_____.

(a) Seconds is assigned with 0 (b) Signal counter is assigned with 0
(c) Sequence counter is assigned with 0 (d) Synchronous clear
(e) Subroutine call.

294. _____ is the memory usually written by the manufacturer.

(a) RAM (b) ROM (c) DRAM
(d) SRAM (e) Cache Memory.

295. is _____.

(a) AND gate (b) OR gate (c) NAND gate
(d) NOR gate (e) Inverted OR gate.

296. Which of the following is **false** related to the logic gates?

(a) NOT=BUFFER (b) NOR=OR+NOT
(c) NAND=AND+NOT (d) XNOR=XOR+NOT
(e) Inverted OR=NOT+OR.

297. Transistors belong to _____ generation of the computer evolution.

(a) First (b) Second (c) Third (d) Fourth

(e) Fifth.

298. Identify the law for the given Boolean function, x(y+z)=xy+xz.

(a) Commutative law (b) Associative law (c) Demorgan's Law
(d) Distributive law (e) Involution law.

299. BCD code is also called as _____.

(a) EBCDIC (b) 2421 (c) Excess -3 (d) Excess-3 gray (e) 8421.

300. Identify the equation for the sum in the full adder.

(a) A B C (b) A B (c) A B'
(d) A' B' C' (e) A' C'.

Answers

291. Answer : (d)

Reason: Gray Code is the binary code where there is only one bit of difference between two consecutive numbers.

292. Answer : (c)

Reason: Combinational circuit is an interconnection of logic gates but sequential includes both flip flops and logic gates and part of sequential circuit is a combinational circuit.

293. Answer : (c)
Reason: SC←0, specifies sequence counter is assigned with 0.

294. Answer : (b)
Reason: ROM is the memory usually written by the manufacturer.

295. Answer : (d)
Reason: is NOR gate.

296. Answer : (a)

Reason: NOT=BUFFER is false and all other are true as not gives complement of the values where as buffer is simply a storage area.

297. Answer : (b)
Reason: Transistors belong to second generation of the computer evolution.

298. Answer : (d)
Reason: The law for the given Boolean function, x(y+z)=xy+xz is distributive law.

299. Answer : (e)
Reason: BCD code is also called as 8421 code.

300. Answer : (a)
Reason: The equation for the sum in the full adder is A B C.

COMPUTER SYSTEM ARCHITECTURE SET 31

Questions 301 To 310

301. Specify the Complement for the equation, F=AB+C'D'+B'D.`

(a) (A+B')(C'+D)(B+D') (b) (A'+B')(C+D)(B+D')
(c) (A'+B')(C'+D')+(B+D') (d) (A'+B')+(C+D)+(B'+D)
(e) (A'+B')(C'+D')(B+D').

302. Identify the input device in which finger shows the cursor movement.

(a) Mouse (b) Scanner (c) Glide pad (d) Microphone
(e) Trackball.

303. Name the keyword to specify the number of pixels displayed on the screen.

(a) Cell (b) Color depth (c) Monitor size (d) Resolution
(e) Refresh rate.

304. Subtract the given unsigned decimal numbers by taking the 10's complement of the subtrahend. 5250 - 1321

(a) 3928 (b) 3828 (c) 3929 (d) 3927 (e) 3729.

305. From the given k-map, give the simplified equation for F.

(a) D + B'C (b) D'+BC (c) D + B'C' (d) D + BC' (e) D + BC.

306. If XY = 0 then what is the value of XY ?

(a) X (b) Y (c) (X'+Y') (d) (X+Y) (e) XY.

307. Specify the hexadecimal equivalent of a decimal number , 10.

(a) A (b) B (c) C (d) D (e) E.

308. Identify the 2's complement of 101010101.

(a) 010101010 (b) 101010101 (c) 010101000
(d) 110101011 (e) 010101011.

309. Name the operation represented by .

(a) OR (b) AND (c) XOR (d) COMPLEMENT (e) NOR.

310. Which one of the following instructions represents .

(a) Memory reference (b) Register reference
(c) I/O instruction (d) A and C above
(e) None of the above.

Answers

301. Answer : (b)

Reason: As OR gates becomes AND gates & values change to their complements
F' = (A'+B')(C+D)(B+D').

302. Answer : (c)

Reason: Glide pad is a input device for which finger shows the cursor movement.

303. Answer : (d)

Reason: Resolution is the number of pixels displayed on the screen.

304. Answer : (c)

Reason: 10's complement as 1321 = 8679 5250 + 8679
3929 – discard the carry.

305. Answer : (a)

Reason: Simplify eight 1's grouped toget D and remaining four 1's to get B'C D + B'C.

306. Answer : (d)

Reason: If XY = 0 XY = X + Y.

307. Answer : (a)

Reason: The Hexadecimal equivalent of a decimal number, 10 is A.

308. Answer : (e)

Reason: 2's complement of 101010101 is 010101011.

309. Answer : (b)

Reason: '' denotes AND.

310. Answer : (b)

Reason: As 15th bit is 0 and Opcode 111 Register reference.

COMPUTER SYSTEM ARCHITECTURE SET 32

Questions 311 To 320

311. Specify the expansion for ISZ.

(a) Invalid to skip if Zero (b) Increment and set if Zero
(c) Increment and sign if Zero (d) Increment and skip if Zero
(e) Increment and save if Zero.

312. Only Push and Pop operations are applicable to which one of the following.

(a) Queue (b) Tree (c) Stack (d) Array (e) Table.

313. Identify the addressing mode, which has instruction specifying a register which contains the memory address of the operand.

(a) Register mode (b) Direct addressing mode
(c) Relative addressing mode (d) Indirect addressing mode
(e) Register indirect mode.

314. Specify the Mnemonic SHRA description.

(a) Arithmetic shift right (b) Arithmetic shift left
(c) Logical shift right (d) Logical shift left
(e) Circular shift right.

315. Identify the expansion for RISC.

(a) Reduced Instruction Sign Computers (b) Reduced Instruction Set Computers
(c) Reduced Instruction Set Carry (d) Reduced Invalid Set Computers
(e) Reset Instruction Set Computers.

316. What are the states of a bus in a computer system?

(a) Logic 0,logic 1 and low impedance (b) Logic 0,logic -1 and high impedance
(c) Logic -2,logic -1 and high impedance (d) Logic -1,logic 1 and high impedance
(e) Logic 0,logic 1 and high impedance.

317. Which one of the following gives the information about, the data used in near future is likely to be in use already?

(a) Spatial locality (b) Locality (c) Hit ratio
(d) Temporal locality (e) Effective access time.

318. What is the page replacement algorithm where thee is a replacement of a page ,which will not be used for the longest period of time?

(a) MFU (b) LRU (c) OPT (d) FIFO (e) LFU.

319. Which one of the following is supplied by one unit to indicate the other unit when the transfer has to occur?

(a) Strobe pulse (b) Time slice (c) Access right (d) Logic gate
(e) Program.

320. Specify, what is a Set of Logical Addresses?

(a) Memory space (b) Disk space (c) Address space (d) Location (e) Pages.

Answers

311. Answer : (d)
Reason: ISZ means increment and skipping zero
312. Answer : (c)
Reason: Stack has Push and POP operations.
313. Answer : (e)
Reason: It is Register indirect mode as the memory address is stored in the register.
314. Answer : (a)
Reason: SHRA describes Arithmetic Shift Right.
315. Answer : (b)
Reason: RISC stands for Reduced Instruction Set Computers.
316. Answer : (e)
Reason: The status as a bus is Logic 0,logic 1 and high impedance.
317. Answer : (d)
Reason: Temporal Locality specifies the information which will be used in near future is likely to be in use already.
318. Answer : (c)
Reason: OPT is the algorithm where there is a replacement of a page, which will not be used for the longest period of time.
319. Answer : (a)
Reason: Strobe pulse is supplied by one unit to indicate the other unit when the transfer has to occur.
320. Answer : (c)
Reason: A Set of Logical Addresses is called Address space.

COMPUTER SYSTEM ARCHITECTURE SET 33

Questions 321 to 330

321. Which one of the following is a memory whose duty is to store most frequently used data?

(a) Main memory (b) Cache memory (c) ROM

(d) Auxiliary memory (e) PROM.

322. What is demonstrated in the given figure?

(a) MICR (b) Bar Code Reader (c) Joy Stick

(d) Track Ball (e) Wand Reader.

323. How many bytes equals Petabyte (PB)?

(a) Quadrillion (b) Million (c) Trillion (d) Billion (e) 1000.

324. What is stored in the Stack Pointer?

(a) Operations (b) Addressing method

(c) Stack data values (d) Address of top item

(e) Address of next instruction.

325. Which one of the following is used to specify the floating point representation?

(a) $r+m^e$ (b) m*r (c) $r*m^e$ (d) $m+r^e$ (e) $m*r^e$.

326. Name the organization in which, the control information is stored in the control memory to initiate the required sequence of micro-operations.

(a) Computer (b) Hardwired (c) Internal (d) Microprogrammed

(e) Control.

327. Identify the method in which the unit receiving the data responds with another control signal.

(a) Handshaking (b) Timing sequence

(c) Synchronous (d) Strobe

(e) Short message service.

328. Which one of the following can be used for checking errors in transmission?

(a) Full duplex (b) Half duplex (c) CRC

(d) Full adder (e) Binary adder.

329. Name the gate given in the diagram.

(a) AND gate (b) OR gate (c) NAND gate

(d) Inverted AND gate (e) Inverted OR gate.

330. Which of the following can be called as universal gate?

(a) NOT (b) NOR (c) OR (d) AND (e) XOR.

Answers

321. Answer : (b)

Reason: Cache memory is a memory whose duty is to store most frequently used data.

322. Answer : (b)

Reason: Bar Code Reader is shown in the figure.

323. Answer : (a)

Reason: Petabyte (PB) is about 1 Quadrillion bytes.

324. Answer : (d)

Reason: Stack Pointer stores Address of top item.

325. Answer : (e)

Reason: Floating point number has $m*r^e$ i.e. mantissa is multiplied by dadix to the power of exponent.

326. Answer : (d)

Reason: In a Microprogrammed organization, the control information is stored in the control memory to initiate the required sequence of micro-operations.

327. Answer : (a)

Reason: The method in which the unit receiving the data, responds with another control signal is referred as Handshaking.

328. Answer : (c)

Reason: CRC – Cyclic Redundancy Check can be used for checking errors in transmission.

329. Answer : (d)

Reason: The figure represents Inverted AND gate.

330. Answer : (b)

Reason: NOR is a universal gate.

COMPUTER SYSTEM ARCHITECTURE SET 34

Questions 331 To 340

331. (x')' is _____

(a) x^2 (b) 0 (c) 1 (d) x (e) x'.

332. A combinational circuit that converts binary information from n- input lines to a maximum of 2^nunique output lines is _____

(a) Multiplexer (b) Full adder (c) Half adder (d) Encoder (e) Decoder.

333. What does D stand for in D-flip flop?

(a) Direct (b) Don't care (c) Data (d) Double (e) Delay.

334. The binary cell capable of storing one bit of information is called _____

(a) Combination circuit (b) Sequential circuit (c) Clock
(d) Latch (e) Flip flop.

335. 'n' number of bits gives _____ number of combinations in a binary system.

(a) 2n (b) 2_n (c) 2^n (d) 2+n (e) 2-n.

336. The performance of the cache memory is measured in terms of a quantity called _____

(a) Initialization Ratio (b) Address Ratio (c) Hit Ratio
(d) Instruction Ratio (e) Miss Ratio.

337. Which of the following is an example of sequential access media?

(a) Main Memory (b) Cache memory (c) Magnetic disk
(d) Magnetic tape (e) CD.

338. The expanded form of ASCII is _____

(a) American Standard Code for Information Inventory
(b) American Standard Code for Information Interchange

(c) American Standard Code for Interchange Information
(d) American Standard Code for Inventory Interchange
(e) American Standard Code for Interchange Inventory.

339. Floating point is always interpreted to represent a number in the following form.

(a) $m * r^e$ (b) $m^e * r$ (c) $e^r * m$ (d) $m * e$ (e) $e^m * r$.

340. _____ is the number system understood by the computer.

(a) Octal (b) Hexa decimal (c) Decimal (d)Binary (e) Assembly.

Answer:

331. Answer : (d)
Reason : The complement of x' is x itself

332. Answer : (e)
Reason : A combinational circuit that converts binary information from n- input lines to a maximum of 2^n unique output lines is Decoder

333. Answer : (c)
Reason : The D stands for Data.

334. Answer : (e)
Reason : The binary cell capable of storing one bit of information is called Flip flop.

335. Answer : (c)
Reason : 'n' number of bits gives 2^n number of combinations in a binary system.

336. Answer : (c)
Reason : The performance of the cache memory is measured in terms of a quantity called Hit ratio

337. Answer : (d)
Reason : Example of sequential access media is Magnetic tape

338. Answer : (b)
Reason : Acronym for ASCII is American Standard Code for Information Interchange

339. Answer : (a)
Reason : Floating point is always interpreted to represent a number as $m * r^e$

340. Answer : (d)
Reason : Binary is the number system understood by the computer.

COMPUTER SYSTEM ARCHITECTURE SET 35

Questions 341 To 350

341. Given the characteristic table of a JK flip-flop, find the missing output value.

S R Q (t+1)

0	0	Q (t)
0	1	0
1	0	1
1	1	-----

(a) Q(t) (b) Q'(t+1) (c) 1 (d) Undetermined (e) Q'(t).

342. _____ is a symbol to denote a part of a register

(a) { } (b) ( ) (c) < > (d) (e) .

343. The register that keeps track of the address of next instruction to be executed is -----

(a) AC (b) PC (c) IR (d) AR (e) DR.

344. If all the bits of the register are loaded simultaneously with a common clock pulse, then it is known as _____

(a) Loading (b) Parallel Loading (c) Serial Loading
(d) Transfer (e) Increment.

345. CISC stands for _____

(a) Control Instruction Set Completeness
(b) Complex Instruction Set Conversion
(c) Complex Instruction Set Computer
(d) Control Instruction Set Computer
(e) Complex Instruction Set Control.

346. The program is executed from main memory until it attempts to reference a page that is still in auxiliary memory, this condition is called as _____

(a) Page Found (b) Page Fault (c) Page Hit (d) Page Miss (e) Page Replace.

347. DMA stands for_____

(a) Direct Memory Address (b) Direct Main Address
(c) Direct Memory Access (d) Direct Main Access
(e) Device Memory Access.

348. _____ is a memory whose duty is to store least frequently used data.

(a) Main memory (b) Cache memory (c) Auxiliary memory
(d) ROM (e) PROM.

349. _____ is a symbol to represent a state in the state diagram

(a) (b) (c) (d) (e) .

350. is a symbol for _____

(a) OR (b) XOR (c) AND (d) NAND (e) NOR.

Answers

341. Answer : (d)

Reason : The missing in that is undetermined.

342. Answer : (b)

Reason : The symbol to denote a part of a register is ( )

343. Answer : (b)

Reason : The register that keeps track of the address of next instruction to be executed is Program Counter

344. Answer : (b)

Reason : If all the bits of the register are loaded simultaneously with a common clock pulse, then it is known as parallel loading

345. Answer : (c)

Reason : CISC stands for Complex Instruction Set Computer

346. Answer : (b)

Reason : The program is executed from main memory until it attempts to reference a page that is still in auxiliary memory, this condition is called as page fault

347. Answer : (c)

Reason : DMA stands for Direct Memory Access

348. Answer : (c)

Reason : Auxiliary memory is a memory whose duty is to store least frequently used data.

349. Answer : (b)

Reason : is a symbol to represent a state in the state diagram

350. Answer : (a)

Reason : The given symbol is for OR

COMPUTER SYSTEM ARCHITECTURE SET 36

Questions 351 To 360

351. The function of the _____ is to store programs and data.

(a) CU (Control Unit) (b) Secondary Memory
(c) ALU (Arithmetical Logic Unit) (d) INPUT device (e) OUTPUT device.

352. Formula for r's complement is _____

(a) $((r^n-1)-N)$ (b) (r^n-N) (c) $(r^n-1)N$ (d) $(r^n)^2-N$
(e) $(r^n-1)+N$.

353. Unicode is a _____

(a) Uniform Code (b) Union Code (c) Universal Condition
(d) Universal Code (e) Unit Code

354. is a symbol for _____ gate?

(a) NOR (b) XOR (c) XNOR (d) NAND
(e) OR.

355. MUTIPLEXER consists of how many number of outputs?

(a) Only one (b) No output (c) Depends on the input
(d) Depends on the select lines (e) Two outputs.

356. _____ is a formula for XOR gate

(a) A'B+AB (b) AB+BA (c) (A+B)(A-B) (d) A'B+B'A
(e) A^2+B^2.

357. Programs must reside in the main memory during _____

(a) Deletion (b) Execution (c) Printing (d) Reading
(e) Insertion.

358. The decimal number equivalent to 1100011 will be

(a) 98 (b) 100 (c) 96 (d) 99
(e) 97.

359. Instruction register stores_____

(a) Address of the current instruction (b) Address of the next instruction
(c) Instruction which is currently executed (d) Next Instruction which is to be executed
(e) Data of the current instruction.

360. Control unit is also called as _____

(a) Supervisor (b) Monitor (c) Manager (d) Controller (e) All of the above.

Answers

351. Answer : (b)
Reason : Secondary Memory is used to store programs and data
352. Answer : (b)
Reason : The formula for r's complement is (r^n–N)
353. Answer : (d)
Reason : Unicode is a universal code
354. Answer : (b)
Reason : the given gate is a symbol for XOR gate
355. Answer : (a)
Reason : MUTIPLEXER consists of only single output
356. Answer : (d)
Reason : A'B+B'A is a formula for XOR gate
357. Answer : (b)
Reason : Programs must reside in the main memory during execution
358. Answer : (d)
Reason : The decimal number equivalent to 1100011 will be 99
359. Answer : (c)
Reason : Instruction register stores instruction which is currently executed
360. Answer : (e)
Reason : Control unit is also called as Supervisor, Monitor, Manager and Controller.

COMPUTER SYSTEM ARCHITECTURE SET 37

Questions 361 To 370

361. According to Boolean algebra A+1 = _____

(a) A (b) 0 (c) 1 (d) A' (e) B.

362. According to Demorgan's Law (A·B)' = _____

(a) A'B' (b) AB (c) A' + B' (d) A'-B' (e) A+B.

363. The terms in the notation m r^e

(a) Mantissa, Round and Exponent
(b) Mantissa, Radix and Exponent
(c) Mantissa, Range and Exponent
(d) Mantissa, Radix and Element
(e) Mantissa, Range and Element.

364. The equivalent decimal number of hexadecimal C4 is obtained from one of the following

(a) C+4 (b) (C16)+(4+1) (c) (C16)+(40) (d) (C16)+(41) (e) C+(40).

365. The function of the _____ is to store programs and data.

(a) CU (Control Unit) (b) MU (Memory Unit)
(c) ALU (Arithmetical Logic Unit) (d) INPUT device
(e) OUTPUT device.

366. Gray Code is also called as _____

(a) Decimal Code (b) Binary Code
(c) 2421 Code (d) Reflected Binary Code
(e) Octal Code.

367. What does 'T' stands in T-flip flop

(a) Top (b) Type (c) Temporary (d) Tiny (e) Toggle.

368. MUX consists of how many number of outputs?

(a) Only one (b) No output
(c) Depends on the input (d) Depends on the select lines
(e) Two outputs.

369. The (r-1)'s complement of 345 in octal number system is

(a) 342 (b) 234 (c) 243 (d) 432 (e) 423.

370. The operation DR ← M[AR] is known as _____

(a) Arithmetic Operation (b) Shift Operation
(c) Memory Write (d) Memory cycle
(e) Memory Read.

Answers

361. Answer : (c)
Reason : According to Boolean algebra A+1 = 1

362. Answer : (c)
Reason : According to Demorgan's Law (A·B)' = A' + B'

363. Answer : (b)

Reason : The terms in the notation m* r^e are Mantissa, Radix and Exponent

364. Answer : (d)
Reason : The equivalent decimal number of hexadecimal C4 is obtained from C*16+4*1

365. Answer : (b)
Reason : The function of the Memory Unit is to store programs and data.

366. Answer : (d)
Reason : Gray Code is also called as Reflected Binary Code.

367. Answer : (e)
Reason : 'T' stands for Toggle in T-flip flop

368. Answer : (a)
Reason : MUX consists of only one output.

369. Answer : (d)
Reason : The (r-1)'s complement of 345 in octal number system is 432.

370. Answer : (e)
Reason : The operation DR ← M[AR] is known as Memory Read.

COMPUTER SYSTEM ARCHITECTURE SET 38

Questions 371 To 380

371. The performance of the cache memory is measured in terms of a quantity called _____

(a) Initialization Ratio (b) Address Ratio
(c) Hit Ratio
(d) Instruction Ratio (e) Miss Ratio.

372. A Set of Physical Addresses is called _____

(a) Memory space (b) Disk space (c) Address space
(d) Location (e) Pages

373. The program is executed from main memory until it attempts to reference a page that is still in auxiliary memory, this condition is called as _____

(a) Page Found (b) Page Fault (c) Page Hit (d) Page Miss (e) Page Replace.

374. DMA stands for_____

(a) Direct Memory Address
(b) Direct Main Address
(c) Direct Memory Access
(d) Direct Main Access
(e) Device Memory Access.

375. _____ is a memory whose duty is to store least frequently used data.

(a) Main memory (b) Cache memory (c) ROM
(d) Auxiliary memory (e) PROM.

376. ISZ is an example of _____ instructions

(a) I/O (b) Memory Reference (c) Register reference

(d) Any type (e) All types.

377. BUN instruction stands for------

(a) Branch Conditionally
(b) Branch Unconditionally
(c) Boot unconditionally
(d) Begin Unconditionally
(e) Branch and save return address.

378. If F= AB' + C'D then F'= ------

(a) (A+B')(C'+D) (b) (A'B)+(CD') (c) (AB')(CD')
(d) (A'+B)(C+D') (e) (A'+B)+(C+D').

379. RISC stands for _____

(a) Reduced Instruction Set Computer
(b) Risk Instruction Set Computer
(c) Reduced Instruction Set Carry
(d) Reset Instruction Set Cache
(e) Reduced Instruction Serial Computer.

380. The _____ operation sets to 1 the bits in one register where there are corresponding 1's in the second register.

(a) Selective Complement (b) Selective Clear (c) Selective Set
(d) Mask (e) Insert

Answers

371. Answer : (c)
Reason : The performance of the cache memory is measured in terms of a quantity called Hit Ratio

372. Answer : (a)
Reason : A Set of Physical Addresses is called Memory space.

373. Answer : (b)
Reason : The program is executed from main memory until it attempts to reference a page that is still in auxiliary memory; this condition is called as Page Fault.

374. Answer : (c)
Reason : DMA stands Direct Memory Access.

375. Answer : (d)
Reason : Auxiliary memory is a memory whose duty is to store least frequently used data.

376. Answer : (b)
Reason : ISZ is an example of Memory Reference instructions.

377. Answer : (b)
Reason : BUN instruction stands for Branch Unconditionally.

378. Answer : (d)
Reason : If F= AB' + C'D then F'= (A'+B)(C+D').

379. Answer : (a)
Reason : RISC stands for Reduced Instruction Set Computer.

380. Answer : (c)

Reason : The Selective Set operation sets to 1 the bits in one register where there are corresponding 1's in the second register.

COMPUTER SYSTEM ARCHITECTURE SET 39

Questions 381 To 390

381. The digital circuit that generates the arithmetic sum of two binary numbers of any length is _____

(a) Binary Adder (b) Full Adder (c) Half Adder (d) Adder (e) OR gate.

382. When the carry into the sign bit and the carry out of the sign bit are applied to _____gate, an overflow can be detected.

(a) EX-NOR (b) INVERTED OR (c) OR (d) NOR (e) X-OR.

383. is_____

(a) AND gate (b) OR gate (c) NAND gate (d) Inverted AND gate (e) Inverted OR gate.

384. Unicode is a _____

(a) Uniform Code (b) Union Code (c) Universal Condition (d) Universal Code (e) Unit Code

385. _____ is a combination of variables.

(a) Cell (b) Map (c) Digit (d) Minterm (e) a or d.

386. is an example for _____

(a) Input device (b) Output device (c) Input or output device (d) ROM (e) Internal storage.

387. Which of the following can be called as universal gate?

(a) NOT (b) NOR (c) OR (d) AND (e) XOR.

388. A table that lists the required inputs for a given change of state is _____

(a) Characteristic table (b) Excitation table (c) Truth table (d) Null table (e) Binary table.

389. is diagram for_____

(a) Encoder (b) Multiplexer (c) Demultiplexer (d) Full Adder (e) Half Subtractor.

390. Microphone is a _____

(a) Output device (b) Storage device (c) Input device (d) Processing device (e) Printing device.

Answers

381. Answer : (a)

Reason : The digital circuit that generates the arithmetic sum of two binary numbers of any length is Binary Adder

382. Answer : (e)

Reason : When the carry into the sign bit and the carry out of the sign bit are applied to X-OR gate,

an overflow can be detected.

383. Answer : (d)
Reason :
is Inverted AND gate

384. Answer : (d)
Reason : Unicode is a Universal Code.

385. Answer : (e)
Reason : A Cell or Minterm is a combination of variables.

386. Answer : (c)
Reason :
is an example for Input or output device.

387. Answer : (b)
Reason : NAND and NOR are both called as universal gates.

388. Answer : (b)
Reason : A table that lists the required inputs for a given change of state is Excitation table.

389. Answer : (c)
Reason :
is diagram for Demultiplexer

390. Answer : (c)
Reason : Microphone is a Input device.

END