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Verification of Hardware Accelerator for Cryptographic Applications

Mini-Project Report

submitted to

Manipal School of Information Sciences, MAHE, Manipal

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DECLARATION

We declare that this mini project, submitted for the evaluation of course work of Mini Project to Manipal School of Information Sciences, is our original work using the design model **"Implementation of Hardware Accelerators for Cryptographic Applications"** from **Mini Project team VL16**, conducted under the supervision of my guide Shridhar Nayak and panel members Shridhar Nayak, Dr. Mohan Kumar J. References, help and material obtained from other sources have been duly acknowledged.

ABSTRACT

Due to rapid development of internet and multimedia application, security is becoming an important issue to protect the ownership as well as integrity of information against third party attacks. Few of the traditional cryptosystems are RSA, DES, and AES are used for encrypting. In our proposed system, we are implementing DES for our core encryption block.

Hardware acceleration is the use of computer hardware specially made to perform some functions more efficiently than is possible in software running on a general-purpose central processing unit (CPU). The project proposed, which is being implemented here is a Hardware accelerator which has a core DES encryption block. The Hardware Accelerator is being enacted in a pipelined manner to achieve 1 GHz frequency for the total system.

The whole system would consist of an Encryption and Decryption Logic blocks as the core, within embedded is the pipelined architecture DES logic blocks. There is also a memory/cache block which is being connected to the Logic blocks through an Interface. The Interface will be running at 1GHz frequency clock, which enables for the fast operation of the whole system.

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ABBREVIATIONS

DES	Data Encryption Standard
RTL	Register Transfer Level
SV	System Verilog
UVM	Universal Verification Methodology
CPU	Central Processing Unit
DUT	Design Under Test

1 Objective

Functional Verification of an (RTL design) hardware accelerator for Cryptographic applications using System Verilog and UVM.

- Search and summarize approaches on the Hardware Accelerators and Verification (technical papers, publication, etc)
- Become familiar with the existing company Verification framework (Testbench Architecture) regarding the Hardware accelerator.
- Study the specification of the Design in a detailed manner to formulate the valid range of test cases for the verification.
- Define verify plan and coverage model for Specification of Hardware Accelerator.
- Set-up randomization constraints in the verification model.
- Set-up library of test sequences.

2 Introduction

Hardware acceleration is the use of computer hardware specially made to perform some functions more efficiently than is possible in software running on a general-purpose central processing unit (CPU). Any transformation of data or routine that can be computed, can be calculated purely in software running on a generic CPU, purely in custom-made hardware, or in some mix of both. An operation can be computed faster in application-specific hardware designed or programmed to compute the operation than specified in software and performed on a general-purpose computer processor. Each approach has advantages and disadvantages. The implementation of computing tasks in hardware to decrease latency and increase throughput is known as hardware acceleration.

Typical advantages of software include more rapid development (leading to faster times to market), lower non-recurring engineering costs, heightened portability, and ease of updating features or patching bugs, at the cost of overhead to compute general operations. Advantages of hardware include speedup, reduced power consumption, lower latency, increased parallelism and bandwidth, and better utilization of area and functional components available on an integrated circuit; at the cost of lower ability to update designs once etched onto silicon and higher costs of functional verification and times to market.

Due to rapid development of internet and multimedia application, security is becoming an important issue to protect the ownership as well as integrity of information against third party attacks. Image encryption manipulates the conversion of an image to another one that is unseeable, while the decryption of an image is the process that retrieves the original image from the image that has been encrypted using appropriate password or key. Therefore, image encryption is among an ultimate solution in protecting the privacy of an image. Unlike text encryption, the image acts as the plaintext. Thus, specific algorithms for image encryption are needed. Few of the traditional cryptosystems are RSA, DES, and AES are used for encrypting.

3 DES Hardware Accelerator RTL Block diagram

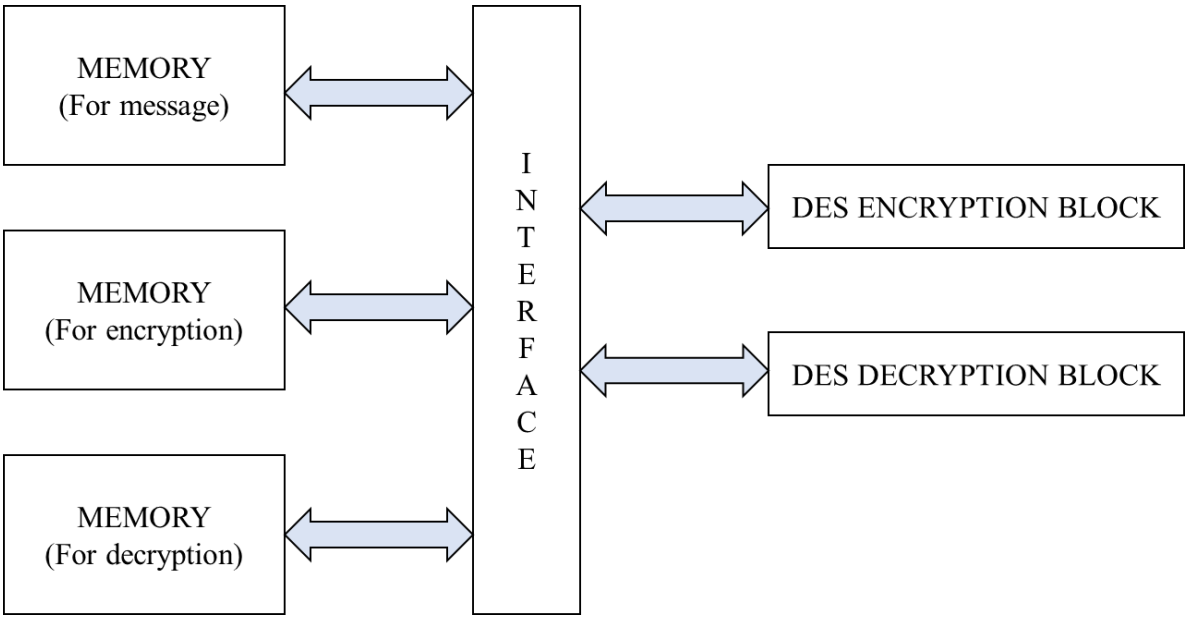

Figure 1.Hardware accelerator block diagram

The DES algorithm is a block cipher that uses the same binary key both to encrypt and decrypt data blocks, and thus is called a symmetric key cipher. DES operates on 64-bit plaintext data blocks, processing them under the control of a 56-bit key to produce 64 bits of encrypted ciphertext. Similarly, the DES decryption process operates on a 64-bit ciphertext block using the same 56-bit key to produce the original 64-bit plaintext block. DES uses a sequence of operations, including several substitution and permutation primitives, to encrypt a data block. These primitives are subsequently used to reverse the encryption operation.

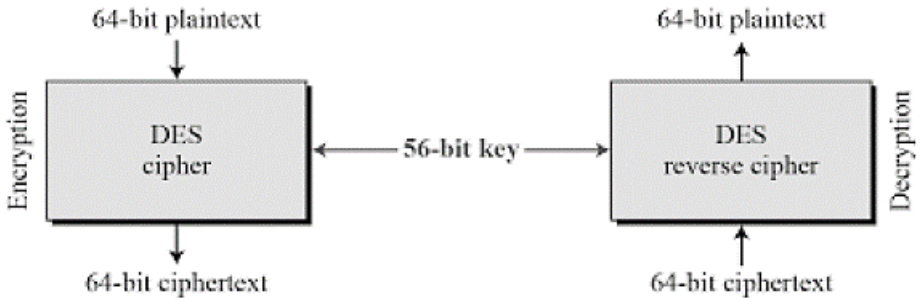

Figure 2. DES algorithm

It uses 16 rounds to ensure that the data are adequately scrambled to meet the security goals. The secret key is used to control the operation of the DES algorithm. Each key contains 56 bits of information, selected by each user to make the results of the encryption operations secret to that user. The message, encrypted data and decrypted data are each written and read from three different memory elements connected to each other by means of an interconnect. The process of encryption and decryption is sped up owing to the highly pipelined architecture used to implement it along with hardware parallelism for a wider range of concurrency.

4 Specification of Design

Encryption Block

- 1GHz operating frequency (clock)
- 115 pipelines stages
- 64-bitlength input data
- 64-bitlength Output data Encryption: cipher text.
- 64-bitlength Key

Decryption Block

- 1GHz operating frequency (clock)
- 115 pipelines stages
- 64-bitlength input data: cipher text from encryption
- 64-bitlength Output data decryption
- 64-bitlength Key

Memory Block

- 64-bit word length size
- 6-bit address line
- Dual port synchronus architecture

4.1 Pin Details

Design unit	Pin name	Direction	Pin description	Pin width (bits)
Encryption	Clk	Input	High Freq input upon which system speed depends on	1
Encryption	Msg	Input	Message data by user	64
Encryption	Key	Input	Cryptic key by user	64
Encryption	Cipher	Output	Cipher data output	64
Decryption	Clk	Input	High Freq input upon which system speed depends on	1
Decryption	Cipher	Input	Cipher data input (from encryption)	64
Decryption	Key	Input	Cryptic key by user (same as above)	64
Decryption	Decrypt	Output	Output message data at receiver (should be same as message data)	64

Design unit	Pin name	Direction	Pin description	Pin width (bits)
Memory	Clk	Input	High Freq input upon which system speed depends on	1
Memory	Reset	Input	Interrupt to the module to clear everything and go to initial state	1
Memory	Write enable	Input	Interrupt to the module to start writing the data to the memory	1
Memory	Read enable	Input	Interrupt to the module to start reading the data from the memory	1
Memory	Address line	Input	Input to the module to insert/read the data from that particular address	6
Memory	Data input line	Input	Message data by user	64
Memory	Key input line	Input	Cryptic key by user	64
Memory	Data output line	Output	Message data from memory	64
Memory	Key output line	Output	Key data from memory	64

Table 1. Pin Details of Encryption, Decryption, and memory Blocks

5 Verification Environment

5.1 Verification using System Verilog.

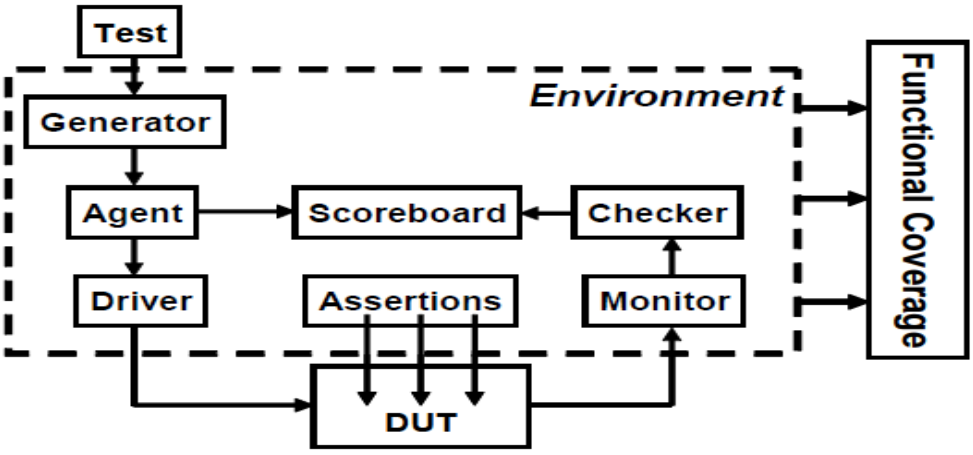

Figure 3. Verification Environment

Environment

The environment happens to be the top-level component in a verification test bench. It contains all the verification components. It also contains configuration properties that allow customization of topology and behaviour, making it reusable. Any verification component can have an environment-level monitor that performs checking and collection of coverage details not related to a single agent. Pre-existing uvm_env class can be extended and configured according to the project specifications. Environment class is responsible for modelling the behaviour of the DUT.

Transaction

This component is responsible for creating different meaningful tests for the DUT. These tests are basically the inputs given to the DUT. The inputs to the DUT are called as data items. Maximum test coverage is attained by intelligently randomizing the fields of the data items using System Verilog constraints.

Driver

This component is responsible for driving signals to the DUT. It receives data items repeatedly from the generator and subsequently drives signals to the DUT. Whatever transaction it gets, it samples them and finally issues them into the DUT. For example, in the case of the Encryption module, this component repeatedly receives message data and key where data items are randomized and feeds these inputs to the DUT.

Monitor

This component is responsible for sampling the DUT signals without driving them. It collects coverage details and does checking. Apart from collecting coverage and performing checks, it has other functionalities as given below.

- The Monitor collects data items from the DUT and translates it into a transaction making it available to other verification components and to the test writer.
- It notifies other components about the availability of transaction through an event emission.
- It also captures status information that are made available to other components and to the test writer.
- Trace information can also be printed using a monitor.

5.2 Verification Using UVM

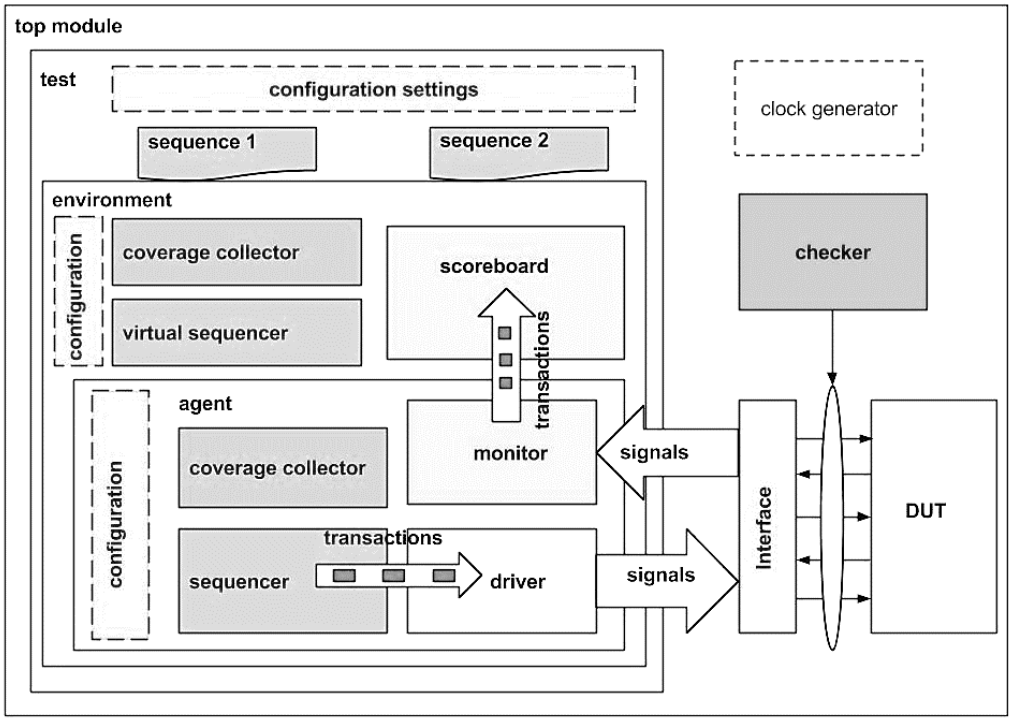

Figure 4. UVM Testbench Architecture

The Universal Verification Methodology (UVM) consists of class libraries needed for the development of well-constructed, reusable System Verilog based Verification environment. In simple words, UVM consists of a set of base classes with methods defined in it, the System Verilog verification environment can be developed by extending these base classes.

UVM Object

Core class based operational methods (create, copy, clone, compare, print, record, etc..), instance identification fields (name, type name, unique id, etc.) and random seeding were defined in it. All uvm_transaction and uvm_component was derived from the uvm_object.

UVM Transaction

Used in stimulus generation and analysis.

UVM Component

Components are quasi-static objects that exist throughout the simulation. Every uvm_component is uniquely addressable via a hierarchical path name, e.g. “env.agent.driver”. The uvm_component also defines a phased test flow, that components follow during the simulation. Each phase (build, connect, run, etc.) is defined by a call back that is executed in precise order. The uvm_component also defines configuration, reporting, transaction recording, and factory interfaces.

UVM Test

The test is the topmost class. the test is responsible for, configuring the testbench. Initiate the testbench components construction process by building the next level down in the hierarchy. Initiate the stimulus by starting the sequence.

UVM Environment

The environment is a container component for grouping higher level components like agent's and scoreboard.

UVM Agent

This component groups the uvm_components specific to an interface or protocol. The components of an agent are,

UVM Sequence Item

The sequence-item defines the pin level activity generated by agent (to drive to DUT through the driver) or the activity has to be observed by agent (Placeholder for the activity monitored by the monitor on DUT signals).

UVM Driver

Responsible for driving the packet level data inside sequence_item into pin level (to DUT).

UVM Sequence

Defines the sequence in which the data items need to be generated and sent/received to/from the driver.

UVM Sequencer

Responsible for routing the data packet's(sequence_item) generated in sequence to the driver or vice versa.

UVM Monitor

Observes pin level activity on interface signals and converts into packet level which is sent to components such as scoreboards.

UVM Scoreboard

Receives data items from monitor's and compares with expected values.

6 Verification Approaches

6.1 Constrained Random Verification (CRV)

Constrained Random Verification (CRV) is a methodology that is supported by System Verilog which has a built-in constraint solver. This allows you to constraint your stimulus to better target a design function, thereby allowing you to reach your coverage goal faster with accuracy. From that sense, coverage and CRV go hand in hand. You check your coverage and see where the coverage holes are. You then constrain your stimulus to target those holes and improve coverage.
As part of verification strategy, you start with direct testing to target “directly” features that you need to verify. But directed testing runs out of steam very fast. If you jump straight to random, you may or may not hit the corner cases of importance. Fully random can end up wasting a lot of simulation cycles without improving coverage. That is where constrained random comes into picture.

6.2 Assertion-based verification (ABV)

Assertion-based verification directly addresses the limitations of today's verification flows. It increases observability in simulation while providing targets for formal verification, which increases controllability. Furthermore, assertions facilitate design reuse through self-checking code.

In assertion-based verification, RTL assertions are used to capture design intent in a verifiable form as the design is created, providing portable monitors that check for correct behaviour. During simulation, assertions improve observability coverage, making the source of an error evident. Simulation debug time is greatly reduced. As targets for formal verification, assertions improve controllability coverage. When verifying assertions, formal verification algorithms explore the equivalent of billions and billions of input patterns without requiring test vector creation. And ideally, the same assertions are used for both simulation and formal verification so there is no need to repeatedly specify the same assertions multiplied different ways for different tools.

Assertion-based verification is a multi-faceted approach to verifying a collection of partial specifications more efficiently. Assertions enable capabilities for both simulation and formal verification and, in the case of open standard assertions, a common method of capturing intimate design knowledge for both.

6.3 Coverage Driven Verification

Coverage Driven Verification is a result-oriented approach to functional verification. In a nutshell, you define your functional coverage points, and then in an iterative process you run tests, analyse the functional coverage, and close in on the remaining functional coverage.

Used effectively coverage driven verification focuses the Verification team on measurable progress toward an agreed and comprehensive goal. Coverage Driven Verification has been used successfully on numerous projects across the industry from small projects to projects designed by hundreds of designers. Coverage driven verification is slowly becoming the predominate method of verification for advanced verification teams.

7 Verification Plan

The Verification Plan is the focal point for defining exactly what needs to be tested and drives the coverage criteria. Success of a verification project relies heavily on the completeness and accurate implementation of a verification plan. A good plan contains detailed goals using measurable metrics, along with optimal resource usage and realistic schedule estimates. Verification plan gives an opportunity to present and review the strategy for functional verification before the verification engineer have gone into detail to implement it.

- Project schedule

  In this stage, different blocks of the DUT are fitted inside the verification schedule. All the dependent and non-dependent components of the DUT are considered in such a way that the Verification of the whole happens in the most efficient manner in the very least time possible.

- Verification approach

  An idea of the DUT is the main deciding factor of the approach that will be used in the verification here. As per this project is considered, the top-level idea of how the DUT works or will perform exists. Hence, a Gray Box Verification approach is considered, which will be the most efficient method to almost verify all the specifications of the DUT.

- Test definitions and Constrained stimulus

  A various range of test cases exist for any form of DUT. But restriction of those unnecessary test cases which might never occur is the way of correctly verifying the DUT specification. A moderate idea of the DUT helps in understanding the randomized test cases to be applied. The stimulus generation section contains information about different types of transactions, sequences of transactions and various scenarios generated as per the specification.

- Testbench requirements

  A detailed Testbench architecture is essential for a robust verification environment. In this section describe the topology, about each component of the Testbench, special techniques that are used, IPs, Reused blocks, new blocks, and guidelines on how to reuse the Testbench components.

- Results Checking

  This section will explain the expected result checking in the Testbench. This can be done in monitor/checker.

- Issue tracking

  The way of checking whether the result from the Scoreboard/Monitor matches and if it does not match, the tracking of where the issue has taken place and bugs involved is covered under this topic.

8 Testcases

8.1 Encryption Block

TEST CASE NUMBER	TEST CASE	SIGNAL	SIGNAL VALUE	EXPECTED OUTPUT	EXPECTED RESULT
1	Negative clock edge	**clk**	LOW	**Cipher** is not changed; previous output is held as it is	PASS
	Positive clock edge		HIGH	**Cipher** should vary according to DES Algorithm	PASS
2	key given is 64 bits wide	**key**	64 bits	**Cipher** will be as expected according to DES Algorithm	PASS
	key length is less than 64 bits		<64 bits	An unknown value comes across the **Cipher** terminals	FAIL
	key length is more than 64 bits		>64 bits	The first 64 bits are considered from **key** and **Cipher** is as per DES Logic	FAIL
3	Message input is 64 bits wide	**msg**	64 bits	**Cipher** will be as expected according to DES Algorithm	PASS
	Message is less than 64 bits wide		<64 bits	An unknown value comes across **Cipher** terminals	FAIL
	Message is more than 64 bits wide		>64 bits	The first 64 bits are considered from **msg** and **Cipher** is as per DES Logic	FAIL
4	When keys are changed for the same message	**Msg, key**	64 bits	Different **Cipher** texts should be obtained.	PASS
5	When Same Key is used with different messages	**Msg, key**	64 bits	**Cipher** will occur as per DES Logic in different cycles	PASS

Table 2. Test Cases for Verification of Encryption Block

8.2 Decryption Block

TEST CASE NUMBER	TEST CASE	SIGNAL	SIGNAL VALUE	EXPECTED OUTPUT	EXPECTED RESULT
1	Negative clock edge	**clk**	LOW	**Decrypt** is not changed; previous output is held as it is	PASS
	Positive clock edge		HIGH	**Decrypt** should vary according to DES Algorithm	PASS
2	key given is 64 bits wide	**key**	64 bits	**Decrypt** will be as expected according to DES Algorithm	PASS
	key length is less than 64 bits		<64 bits	An unknown value comes across the **Decrypt** terminals	FAIL
	key length is more than 64 bits		>64 bits	The first 64 bits are considered from **key** and **Decrypt** is as per DES Logic	FAIL
3	cipher input is 64 bits wide	**cipher**	64 bits	**Decrypt** will be as expected according to DES Algorithm	PASS
	cipher is less than 64 bits wide		<64 bits	An unknown value comes across the **Decrypt** terminals	FAIL
	cipher is more than 64 bits wide		>64 bits	The first 64 bits are considered from **cipher** and **Decrypt** is as per DES Logic	FAIL
4	When keys are changed for the same message	**cipher, key**	64 bits	Original message should not be obtained at **Decrypt** for different Key	PASS
5	When Same Key is used with different messages	**cipher, key**	64 bits	**Decrypt** will occur as per DES Logic in different cycles	PASS

Table 3. Test Cases for verification of Decryption Block

8.3 Memory Block

TEST CASE NUMBER	TEST CASE	SIGNAL	SIGNAL VALUE	EXPECTED OUTPUT	EXPECTED RESULT
1	Negative clock edge	**clk**	LOW	Output lines should not change values even if Input given is changed.	PASS
	Positive clock edge		HIGH	Output lines should read data from memory as per the Read Enable input whereas Input lines should write data as per the Write Enable Input	PASS
2	Clearing the data	**reset**	HIGH	**Reset, when** high clears every bit of memory block and makes it 0.	PASS
	Storing the data		LOW	**Reset**, when low allows the memory to store data as per its operation	PASS
3	Stopping the data to be written to memory	**Wr_en**	LOW	**Input** lines should not be able to write any data into memory	PASS
	Allowing the data to be written to memory		HIGH	**Input** lines should be able to write the data into memory	PASS
4	Stopping the data to be read from memory	**r_en**	LOW	**Output** lines should not be able to read any data from memory	PASS
	Allowing the data to be read from memory		HIGH	**Output** lines should be able to read data from memory	PASS
5	When key/message input is less than 64 bits wide	**Msg, key_in**	<64bits	**Input Data lines** should be saved as it is and don't care(x) will fill the rest in those empty slots	FAIL
6	When key/message input is more than 64 bits wide	**Msg, key_in**	>64bits	**Input Data lines** will be taken till 64 bits and rest of the bits are truncated.	FAIL

Table 4. Test cases defined for Memory block

9 Implementation

9.1 Verification Framework using System Verilog

1. Transaction class

   This class consists of the input signals that must be passed to the DUT. For encryption block it contains 64 bits msg and key. These signals are declared as rand logic signals such that it can be varied in generation block. A function written to display the data transaction data packet.
2. Generator class

   This class randomises the transaction packet and puts this value to the mailbox. Mailbox is communicating in between the generator and driver. An integer variable Rptcount is set with some value, according to that data is randomized and fed into the monitor.
3. Driver class

   Driver gets the transaction packet from the mailbox. This class performs two tasks, First the data in the transaction packets are reset with an initial value. As soon as the reset signal gets low the data from the transaction packets are fed into the virtual interface which will be fed into the DUT.
4. Monitor class.

   Monitor creates a new transaction packet as it is received from the DUT. Transaction packets created will extract the values from the DUT and then it will be put into a mailbox connecting monitor to scoreboard.
5. Scoreboard class

   This extracts the data from the mailbox from monitor. These transaction input data are fed into the golden reference module. The output from the golden reference module is also recorded and validated with respect to the DUT output. If there is any variation it is displayed and if the results are as expected it is also displayed. A count of each transaction also recorded.
6. Environment class

   Environment Is the overall cover which combines generator driver monitor and scoreboard. It combines these logics to work together. It has three tasks, first is the pretest in which the transaction data will be reset, second is the test in which all the tasks are run from different components. These will be in a fork join_any which will work these functions parallelly. Finally, in posttest it is validated if the counts are equal with respected to the generator and the scoreboard. If these are equal, then the process is stopped.
7. Test program

   This comprises overall combination of the environment where different environments can be combined. A class is called inside a program to create a flow. Initial values of count of number of transactions are set, then main task is run from the test program.
8. Top module

   Top module acts a bridge between the verification framework and the DUT. Interface, clock reset pins are initialized and DUT instance is created and connected with verification framework. Similarly traces file of the module is also generated for further ASIC flow process.

9.2 Verification Framework using UVM

1. Sequence Item

   The sequence-item defines the pin level activity generated by agent or the activity must be observed by agent. Consisting of the 64bit key and message and cipher text, the signals are chosen as rand logic because the UVM driver can later randomize it as it sees.
2. Driver

   This is responsible for driving the packet level data inside sequence_item into pin level (to DUT). This generates an object of the sequence_item and the task run_phase executes it when the event occurs, triggered by the Interface clocking block.

3. Sequence block

   This block defines the sequence in which data items need to be generated and sent/received to/from. The number of times a sequence_item should be generated is chosen in the body task.
4. Sequencer

   This is responsible for routing the data packets generated in the sequence to the driver or vice versa.
5. Monitor

   This observes pin level activity on interface signals and converts into packet level which is sent to components such as scoreboards. The task run_phase monitors the output at the event triggered by the Interface clocking blocks.
6. Scoreboard

   This receives data of sequence_item from monitor and compares with expected values. There is a checker which asserts the value of received data with that of the golden reference module. This information is further sent to coverage analysis through the sequence_item.
7. Covergroup

   The covergroup construct encapsulates the specification of a coverage model. Coverage bins have been written for the signals that are required for coverage analysis. The level of coverage is defined by the number of times the sequence hits the value of coverage bin.

9.3 Interface

Interface is the one which communicates between the DUT and the verification environment. It consists of a clk pin, 64-bit msg and key input pins and 64-bit cipher output pins. The interface comprises of the clocking block which is synchronised with the clk which helps in setting up inputs and response from the verification environment to the DUT. Clocking blocks also can be used to set up slacks of clock to avoid data miss match in design units.

9.4 Golden reference

The inputs which are given into the DUT and validated against the already present reference module called as golden reference. It gets the same inputs which is fed into the Design unit. In this design we have consider a system Verilog approach of DES Algorithm as golden reference. This class also works on 64 bits encryption and decryption strategy.

9.5 Design Under Test (DUT)

Through a Grey box verification approach, knowledge regarding the overview of the design units the verification environment has been set up. As the design team finishes the development of the block, it has been handed over for verification. DUT is connected using the interface and driven by the verification environment. Various test cases are applied to verify the functionality and coverages of the Design unit.

10 Software & Hardware Requirements

Programming Language:

1. System Verilog.
2. UVM

Design Suites:

1. Cadence NC-Sim.
2. Mentor Graphics QuestaSim.
3. EDA-Playground.

11 Results of Verification using System Verilog

11.1 Encryption Block

```
---------------
[MONITOR] - ENC Input Generated
---------------
Msg:                    x
key:                    x
---------------
Output Observed
---------------
Cipher:                   0
---------------
---------------
[Driver - ENC ] Input Generated
---------------
Msg: 14643775950274165321
key: 13472828726326586992
---------------
Output Observed
---------------
Cipher:                   0
---------------
Wrong Result. ENC:
        Expected :                  x Actual:                   0

---------------
[ scoreboard - ENC ] Input Generated
---------------
Msg:                    x
key:                    x
---------------
Output Observed
---------------
Cipher:                   0
---------------
---------------
[MONITOR] - ENC Input Generated
---------------
Msg: 14643775950274165321
key: 13472828726326586992
---------------
```

```
---------------
Output Observed
---------------
Cipher: 10756936861419804621
---------------
---------------
[Driver - ENC ] Input Generated
---------------
Msg: 16144636008425789881
key:    78152815594937342
---------------
Output Observed
---------------
Cipher: 10756936861419804621
---------------
Result is as Expected
---------------
[ scoreboard - ENC ] Input Generated
---------------
Msg: 14643775950274165321
key: 13472828726326586992
---------------
Output Observed
---------------
Cipher: 10756936861419804621
---------------
---------------
[MONITOR] - ENC Input Generated
---------------
Msg: 16144636008425789881
key:    78152815594937342
---------------
Output Observed
---------------
Cipher: 15818365332459960971
---------------
---------------
[Driver - ENC ] Input Generated
---------------
Msg:  3253416903612027591
key: 17846942369046761233
---------------
```

```
---------------
Output Observed
---------------
Cipher: 15818365332459960971
---------------
Result is as Expected
---------------
[ scoreboard - ENC ] Input Generated
---------------
Msg: 16144636008425789881
key:    78152815594937342
---------------
Output Observed
---------------
Cipher: 15818365332459960971
---------------
---------------
[MONITOR] - ENC Input Generated
---------------
Msg:  3253416903612027591
key: 17846942369046761233
---------------
Output Observed
---------------
Cipher: 16359270421751669271
---------------
---------------
[Driver - ENC ] Input Generated
---------------
Msg:  6032319518772486038
key: 12883110298986591852
---------------
Output Observed
---------------
Cipher: 16359270421751669271
---------------
Result is as Expected
---------------
```

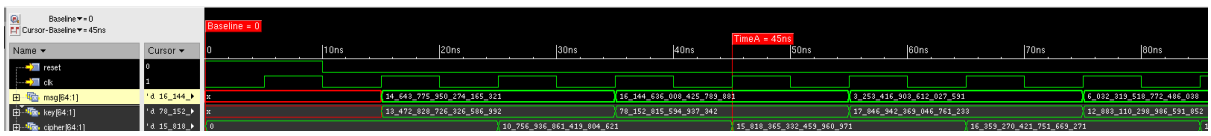

Figure 5. Output observed for Verification of DES Encryption – System verilog

11.2 Decryption block

```
[Driver]--Reset Started--
[Driver]--Reset Ended--
---------------
[MONITOR] - DEC Input Generated
---------------
Cipher:                    0
key:                     x
---------------
Output Observed
---------------
Decrypt:                    0
---------------
---------------
[Driver - DEC ] Input Generated
---------------
Cipher: 13472828726326586992
key: 14643775950274165321
---------------
Output Observed
---------------
Decrypt:                    0
---------------
Wrong Result. DEC:
         Expected :                    x Actual:                    0

---------------
[ scoreboard - DEC ] Input Generated
---------------
Cipher:                    0
key:                     x
---------------
Output Observed
---------------
Decrypt:                    0
---------------
```

```
---------------
[MONITOR] - DEC Input Generated
---------------
Cipher: 13472828726326586992
key: 14643775950274165321
---------------
Output Observed
---------------
Decrypt: 12964919662365805260
---------------
---------------
[Driver - DEC ] Input Generated
---------------
Cipher:    78152815594937342
key: 16144636008425789881
---------------
Output Observed
---------------
Decrypt: 12964919662365805260
---------------
Result is as Expected
---------------
[ scoreboard - DEC ] Input Generated
---------------
Cipher: 13472828726326586992
key: 14643775950274165321
---------------
Output Observed
---------------
Decrypt: 12964919662365805260
---------------
```

```
---------------
[MONITOR] - DEC Input Generated
---------------
Cipher:    78152815594937342
key: 16144636008425789881
---------------
Output Observed
---------------
Decrypt: 18236230773660754005
---------------
---------------
[Driver - DEC ] Input Generated
---------------
Cipher: 17846942369046761233
key:  3253416903612027591
---------------
Output Observed
---------------
Decrypt: 18236230773660754005
---------------
Result is as Expected
---------------
[ scoreboard - DEC ] Input Generated
---------------
Cipher:    78152815594937342
key: 16144636008425789881
---------------
Output Observed
---------------
Decrypt: 18236230773660754005
---------------
```

Figure 6. Terminal Output of System Verilog verification of Decryption block

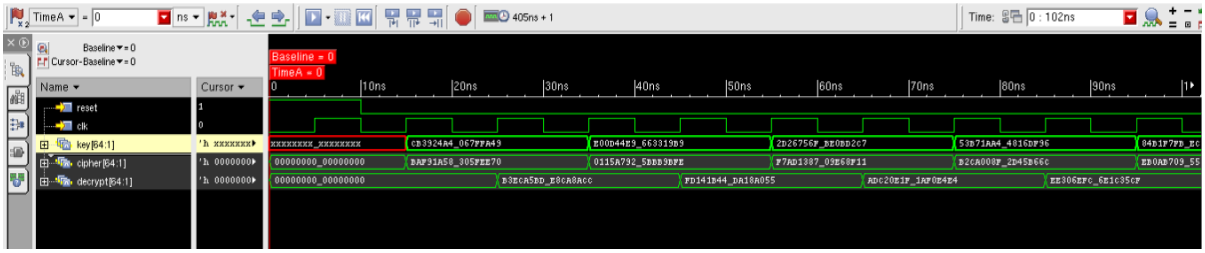

Figure 7. Simulation Output of Systemverilog verification of decryption block

11.3 Memory Block

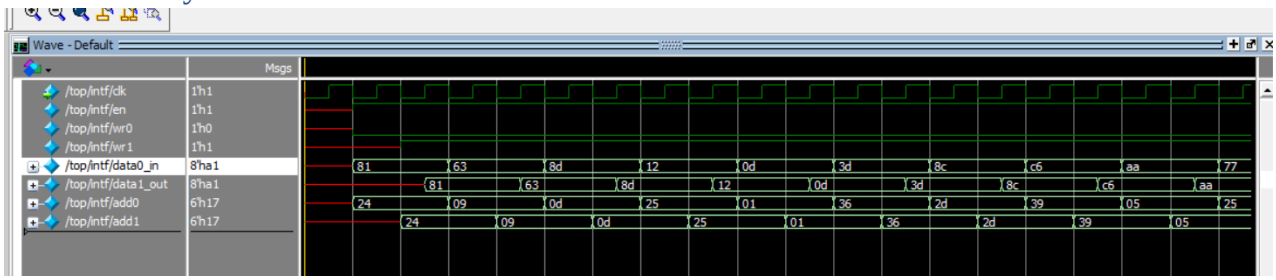

Figure 8. Simulation Output of verification of Memory Block/RAM

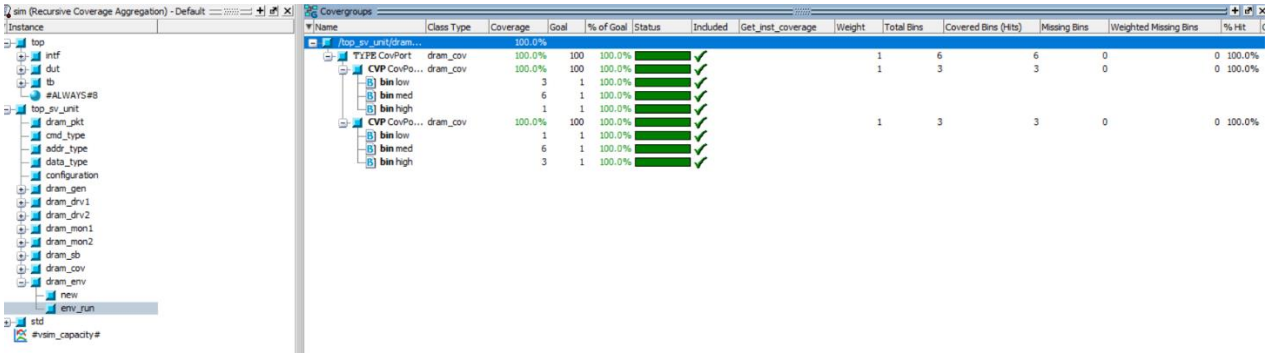

Figure 9. Percentage of Coverage analysis of memory block in Questasim

Questa Coverage Report

Number of tests run:	1
Passed:	0
Warning:	0
Error:	1
Fatal:	0

List of tests included in report...

List of global attributes included in report...

List of Design Units included in report...

Coverage Summary by Structure:

Design Scope	Hits %	Coverage %
top	62.90%	62.07%
intf	60.82%	80.20%
dut	50.00%	50.00%
tb	100.00%	100.00%
top_sv_unit	75.00%	61.30%
dram_gen/new	100.00%	100.00%
dram_gen/run	50.00%	39.58%
dram_gen/calc_addr	23.07%	22.61%
dram_gen/calc_datain	23.07%	22.61%
dram_drv1/new	100.00%	100.00%
dram_drv1/run	91.66%	75.00%
dram_drv2/new	100.00%	100.00%

Coverage Summary by Type:

Total Coverage:					70.12%	61.56%
Coverage Type	**Bins**	**Hits**	**Misses**	**Weight**	**% Hit**	**Coverage**
Covergroups	6	6	0	1	100.00%	100.00%
Statements	168	136	32	1	80.95%	80.95%
Branches	32	13	19	1	40.62%	40.62%
FEC Conditions	4	1	3	1	25.00%	25.00%
Toggles	98	60	38	1	61.22%	61.22%

Figure 10. Coverage report of Memory/RAM observed in Questasim

12 Results of verification using UVM

12.1 Encryption block

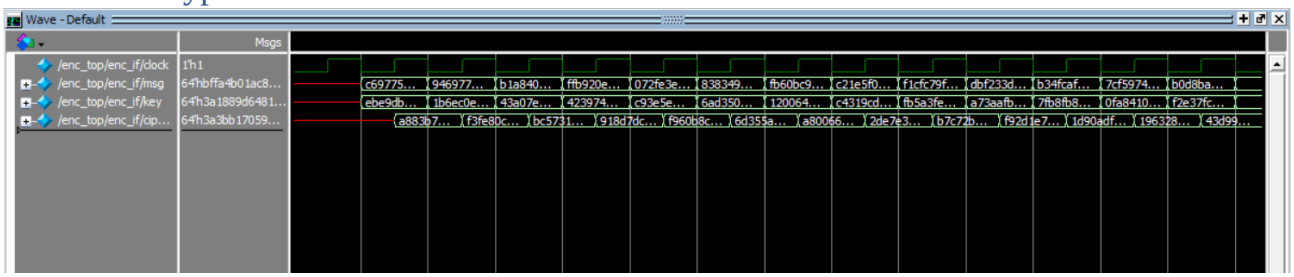

Figure 11. Simulation Output of verification of Encryption Block in UVM

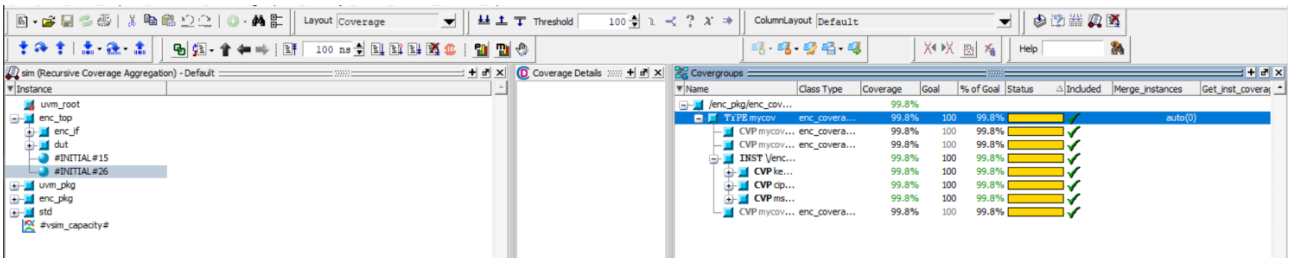

Figure 12. Percentage of Coverage Analysis of Encryption Block in UVM

Questa Coverage Report

Number of tests run:	1
Passed:	1
Warning:	0
Error:	0
Fatal:	0

List of tests included in report...

List of global attributes included in report...

List of Design Units included in report...

Coverage Summary by Structure:

Design Scope	Hits %	Coverage %
enc_top	100.00%	100.00%
enc_if	100.00%	100.00%
dut	100.00%	100.00%
enc_pkg	96.15%	93.77%
GRDESENC/encryption	100.00%	100.00%
GRDESENC/keygen	100.00%	100.00%
GRDESENC/rotate_left	100.00%	100.00%
GRDESENC/init_permute	100.00%	100.00%
GRDESENC/final_permute	100.00%	100.00%
GRDESENC/fiestal_round	100.00%	100.00%
GRDESENC/encrypt	100.00%	100.00%
GRDESENC/sbox1	99.23%	99.23%

Coverage Summary by Type:

Total Coverage:					97.20%	97.27%
Coverage Type	**Bins**	**Hits**	**Misses**	**Weight**	**% Hit**	**Coverage**
Covergroups	3006	3000	6	1	99.80%	99.80%
Statements	1267	1196	71	1	94.39%	94.39%
Branches	1136	1047	89	1	92.16%	92.16%
Toggles	518	518	0	1	100.00%	100.00%
Assertions	2	2	0	1	100.00%	100.00%

Figure 13. Complete Coverage report of Encryption block in UVM

12.2 Decryption block

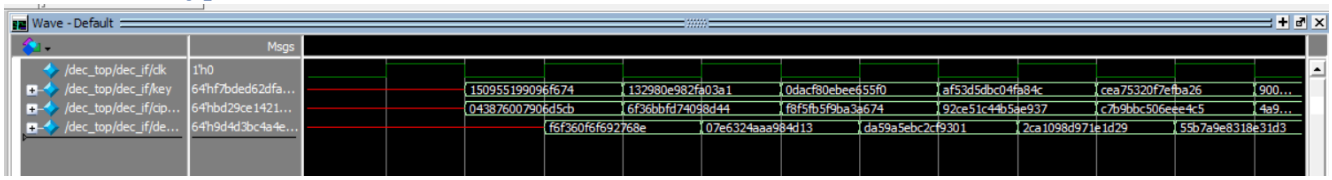

Figure 14. Simulation Output of verification of Decryption block in UVM

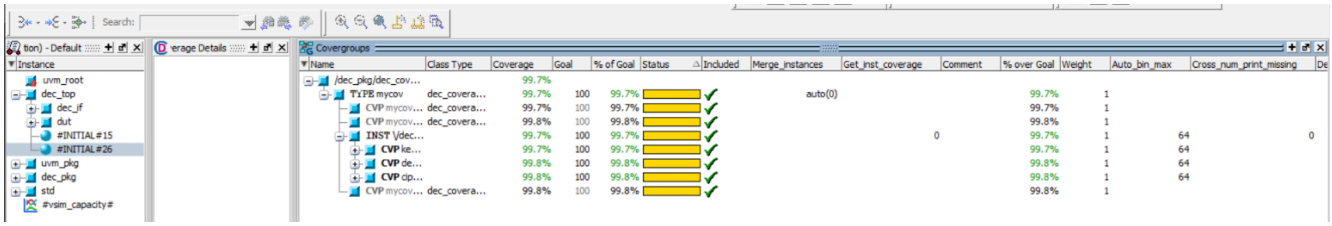

Figure 15. Percentage of Coverage analysis of Decryption block in UVM

Questa Coverage Report

Number of tests run:	1
Passed:	1
Warning:	0
Error:	0
Fatal:	0

List of tests included in report...

List of global attributes included in report...

List of Design Units included in report...

Coverage Summary by Structure:

Design Scope	Hits %	Coverage %
dec_top	92.64%	93.39%
dec_if	75.33%	87.54%
dut	100.00%	100.00%
dec_pkg	96.13%	93.76%
GRDESDEC/decryption	100.00%	100.00%
GRDESDEC/keygen	100.00%	100.00%
GRDESDEC/rotate_left	100.00%	100.00%
GRDESDEC/init_permute	100.00%	100.00%
GRDESDEC/final_permute	100.00%	100.00%
GRDESDEC/fiestal_round	100.00%	100.00%
GRDESDEC/decrypt	100.00%	100.00%
GRDESDEC/sbox1	99.23%	99.23%

Coverage Summary by Type:

Total Coverage:					95.12%	93.30%
Coverage Type	**Bins**	**Hits**	**Misses**	**Weight**	**% Hit**	**Coverage**
Covergroups	3006	2999	7	1	99.76%	**99.76%**
Statements	1266	1195	71	1	94.39%	**94.39%**
Branches	1136	1047	89	1	92.16%	**92.16%**
Toggles	646	518	128	1	80.18%	**80.18%**
Assertions	2	2	0	1	100.00%	**100.00%**

Figure 16. Complete coverage report of Decryption block in UVM

12.3 Memory Block

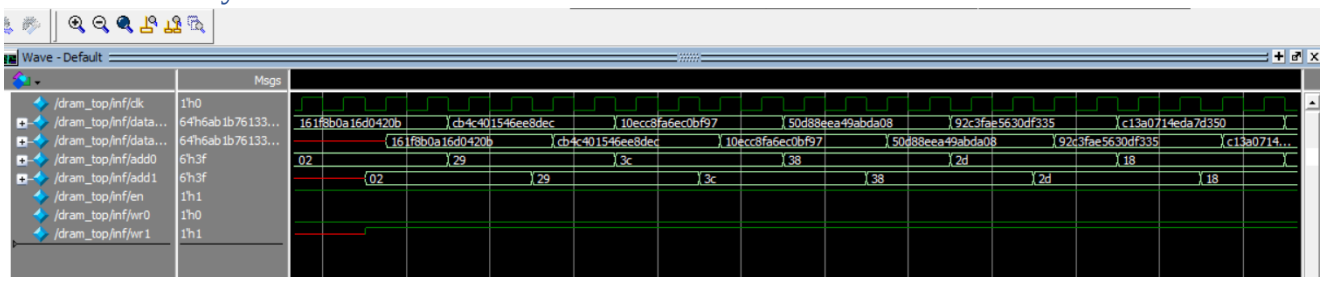

Figure 17. Simulation output of verification of Memory block/RAM in UVM

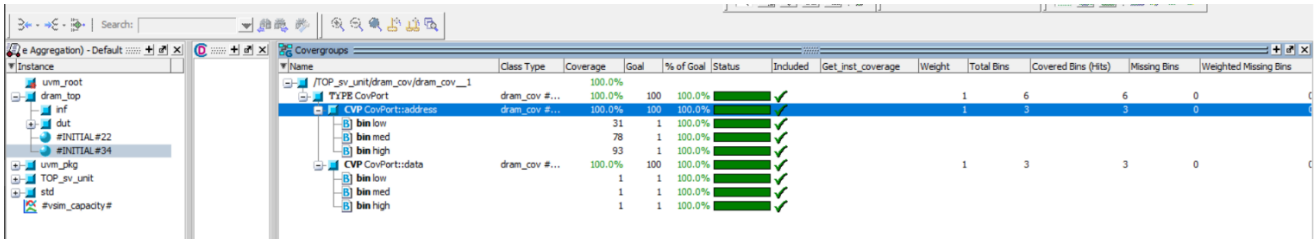

Figure 18. Percentage of coverage analysis of Memory block in UVM

Questa Coverage Report

Number of tests run:	1
Passed:	1
Warning:	0
Error:	0
Fatal:	0

List of tests included in report...

List of global attributes included in report...

List of Design Units included in report...

Coverage Summary by Structure:

Design Scope	Hits %	Coverage %
dram_top	52.46%	56.92%
inf	51.83%	51.83%
dut	50.00%	50.00%
TOP_sv_unit	64.06%	62.19%
dram_seq_item/new	100.00%	100.00%
dram_seq_item/get_type	0.00%	0.00%
dram_seq_item/get_object_type	0.00%	0.00%
dram_seq_item/create	0.00%	0.00%
dram_seq_item/get_type_name	100.00%	100.00%
dram_seq_item/__m_uvm_field_automation	25.00%	25.00%
dram_seq/new	100.00%	100.00%
dram_seq/get_type	0.00%	0.00%

Coverage Summary by Type:

Total Coverage:					55.81%	60.62%
Coverage Type	**Bins**	**Hits**	**Misses**	**Weight**	**% Hit**	**Coverage**
Covergroups	6	6	0	1	100.00%	100.00%
Statements	182	130	52	1	71.42%	71.42%
Branches	62	25	37	1	40.32%	40.32%
FEC Conditions	2	0	2	1	0.00%	0.00%
Toggles	546	284	262	1	52.01%	52.01%
Assertions	1	1	0	1	100.00%	100.00%

Figure 19. Complete coverage report of Memory block in UVM

13 Applications

1. Hardware accelerators are used extensively in AI chips to segment and expedite data-intensive tasks like computer vision and deep learning for both training and inference applications.
2. Used as external Graphical Processing Units (GPUs) for high-end gaming.
3. For performing cryptographic operations as well as in floating point calculations

14 References

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- https://verificationguide.com/systemverilog-examples/, as on 10th June 2021.
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- https://www.design-reuse.com/articles/16141/verification-planning-for-core-based-designs.html, as on 10th june 2021.
- UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology by Ray Salemi 2013.
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- https://www.chipverify.com/systemverilog/systemverilog-tutorial, as on 10th June 2021
- https://www.chipverify.com/uvm/uvm-tutorial, as on 10th June 2021.
- http://www.testbench.in/UT_00_INDEX.html, as on 10th June 2021.

15 Appendix

15.1 Log and report files of System Verilog Verification Approach

15.1.1 Encryption Block Log

```
---------------
[MONITOR] - ENC Input Generated
---------------
Msg:                    x
key:                    x
---------------
Output Observed
---------------
Cipher:                     0
---------------
---------------
[Driver - ENC ] Input Generated
---------------
Msg: 14643775950274165321
key: 13472828726326586992
---------------
Output Observed
---------------
Cipher:                     0
---------------
Wrong Result. ENC:
        Expected :                    x Actual:                     0

---------------
[ scoreboard - ENC ] Input Generated
---------------
Msg:                    x
key:                    x
---------------
Output Observed
---------------
Cipher:                     0
---------------
---------------
[MONITOR] - ENC Input Generated
---------------
Msg: 14643775950274165321
key: 13472828726326586992
---------------
Output Observed
---------------
Cipher: 10756936861419804621
---------------
---------------
[Driver - ENC ] Input Generated
---------------
Msg: 16144636008425789881
key:    78152815594937342
---------------
Output Observed
---------------
Cipher: 10756936861419804621
---------------
Result is as Expected
---------------
[ scoreboard - ENC ] Input Generated
---------------
Msg: 14643775950274165321
key: 13472828726326586992
---------------
Output Observed
---------------
Cipher: 10756936861419804621
```

```
---------------
---------------
[MONITOR] - ENC Input Generated
---------------
Msg: 16144636008425789881
key:    78152815594937342
---------------
Output Observed
---------------
Cipher: 15818365332459960971
---------------
---------------
[Driver - ENC ] Input Generated
---------------
Msg:  3253416903612027591
key: 17846942369046761233
---------------
Output Observed
---------------
Cipher: 15818365332459960971
---------------
Result is as Expected
---------------
[ scoreboard - ENC ] Input Generated
---------------
Msg: 16144636008425789881
key:    78152815594937342
---------------
Output Observed
---------------
Cipher: 15818365332459960971
---------------
---------------
[MONITOR] - ENC Input Generated
---------------
Msg:  3253416903612027591
key: 17846942369046761233
---------------
Output Observed
---------------
Cipher: 16359270421751669271
---------------
---------------
[Driver - ENC ] Input Generated
---------------
Msg:  6032319518772486038
key: 12883110298986591852
---------------
Output Observed
---------------
Cipher: 16359270421751669271
---------------
Result is as Expected
---------------
[ scoreboard - ENC ] Input Generated
---------------
Msg:  3253416903612027591
key: 17846942369046761233
---------------
Output Observed
---------------
Cipher: 16359270421751669271
---------------
---------------
[MONITOR] - ENC Input Generated
---------------
Msg:  6032319518772486038
key: 12883110298986591852
```

```
---------------
Output Observed
---------------
Cipher: 12650996009217332547
---------------
---------------
[Driver - ENC ] Input Generated
---------------
Msg:  9561696145258444900
key: 16936550599396745572
---------------
Output Observed
---------------
Cipher: 12650996009217332547
---------------
Result is as Expected
---------------
[ scoreboard - ENC ] Input Generated
---------------
Msg:  6032319518772486038
key: 12883110298986591852
---------------
Output Observed
---------------
Cipher: 12650996009217332547
---------------
---------------
[MONITOR] - ENC Input Generated
---------------
Msg:  9561696145258444900
key: 16936550599396745572
---------------
Output Observed
---------------
Cipher:  6881877631432362454
---------------
---------------
[Driver - ENC ] Input Generated
---------------
Msg:  5651632178737191144
key: 17773367370097824498
---------------
Output Observed
---------------
Cipher:  6881877631432362454
---------------
Result is as Expected
---------------
[ scoreboard - ENC ] Input Generated
---------------
Msg:  9561696145258444900
key: 16936550599396745572
---------------
Output Observed
---------------
Cipher:  6881877631432362454
---------------
---------------
[MONITOR] - ENC Input Generated
---------------
Msg:  5651632178737191144
key: 17773367370097824498
---------------
Output Observed
---------------
Cipher: 13533056312562257279
---------------
---------------
```

```
[Driver - ENC ] Input Generated
---------------
Msg: 15730455434195945102
key: 10644606227120236465
---------------
Output Observed
---------------
Cipher: 13533056312562257279
---------------
Result is as Expected
---------------
[ scoreboard - ENC ] Input Generated
---------------
Msg:  5651632178737191144
key: 17773367370097824498
---------------
Output Observed
---------------
Cipher: 13533056312562257279
---------------
---------------
[MONITOR] - ENC Input Generated
---------------
Msg: 15730455434195945102
key: 10644606227120236465
---------------
Output Observed
---------------
Cipher: 15730528236370017493
---------------
---------------
[Driver - ENC ] Input Generated
---------------
Msg: 15774731430862910706
key: 13517646133809545403
---------------
Output Observed
---------------
Cipher: 15730528236370017493
---------------
Result is as Expected
---------------
[ scoreboard - ENC ] Input Generated
---------------
Msg: 15730455434195945102
key: 10644606227120236465
---------------
Output Observed
---------------
Cipher: 15730528236370017493
---------------
---------------
[MONITOR] - ENC Input Generated
---------------
Msg: 15774731430862910706
key: 13517646133809545403
---------------
Output Observed
---------------
Cipher: 14714973406279199876
---------------
---------------
[Driver - ENC ] Input Generated
---------------
Msg:  1756913157715644902
key:  5425147556136906914
---------------
Output Observed
```

```
---------------
Cipher: 14714973406279199876
---------------
Result is as Expected
---------------
[ scoreboard - ENC ] Input Generated
---------------
Msg: 15774731430862910706
key: 13517646133809545403
---------------
Output Observed
---------------
Cipher: 14714973406279199876
---------------
---------------
[MONITOR] - ENC Input Generated
---------------
Msg:  1756913157715644902
key:  5425147556136906914
---------------
Output Observed
---------------
Cipher:  6389038484097654069
---------------
---------------
[Driver - ENC ] Input Generated
---------------
Msg: 14630111108593188340
key: 17038020110271968062
---------------
Output Observed
---------------
Cipher:  8552393607365936915
---------------
Result is as Expected
---------------
[ scoreboard - ENC ] Input Generated
---------------
Msg:  7821013592900726439
key: 16676636027694377592
---------------
Output Observed
---------------
Cipher:  8552393607365936915
---------------
---------------
[MONITOR] - ENC Input Generated
---------------
Msg: 14630111108593188340
key: 17038020110271968062
---------------
Output Observed
---------------
Cipher:  3465573786210155154
---------------
---------------
[Driver - ENC ] Input Generated
---------------
Msg: 17897506148814379365
key: 14275680192859870949
---------------
Output Observed
---------------
Cipher:  3465573786210155154
---------------
Result is as Expected
---------------
[ scoreboard - ENC ] Input Generated
```

```
---------------
Msg: 14630111108593188340
key: 17038020110271968062
---------------
Output Observed
---------------
Cipher:  3465573786210155154
---------------
Simulation complete via $finish(1) at time 405 NS + 1
./environment.sv:55       $finish;
```

15.1.2 Decryption Block Log

```
---------------
[MONITOR] - DEC Input Generated
---------------
Cipher:                    0
key:                   x
---------------
Output Observed
---------------
Decrypt:                    0
---------------
---------------
[Driver - DEC ] Input Generated
---------------
Cipher: 13472828726326586992
key: 14643775950274165321
---------------
Output Observed
---------------
Decrypt:                    0
---------------
Wrong Result. DEC:
        Expected :                   x Actual:                    0

---------------
[ scoreboard - DEC ] Input Generated
---------------
Cipher:                    0
key:                   x
---------------
Output Observed
---------------
Decrypt:                    0
---------------
---------------
[MONITOR] - DEC Input Generated
---------------
Cipher: 13472828726326586992
key: 14643775950274165321
---------------
Output Observed
---------------
Decrypt: 12964919662365805260
---------------
---------------
[Driver - DEC ] Input Generated
---------------
Cipher:    78152815594937342
key: 16144636008425789881
---------------
Output Observed
---------------
Decrypt: 12964919662365805260
---------------
Result is as Expected
```

```
---------------
[ scoreboard - DEC ] Input Generated
---------------
Cipher: 13472828726326586992
key: 14643775950274165321
---------------
Output Observed
---------------
Decrypt: 12964919662365805260
---------------
---------------
[MONITOR] - DEC Input Generated
---------------
Cipher:    78152815594937342
key: 16144636008425789881
---------------
Output Observed
---------------
Decrypt: 18236230773660754005
---------------
---------------
[Driver - DEC ] Input Generated
---------------
Cipher: 178469423690467612 33
key:  3253416903612027591
---------------
Output Observed
---------------
Decrypt: 18236230773660754005
---------------
Result is as Expected
---------------
[ scoreboard - DEC ] Input Generated
---------------
Cipher:    78152815594937342
key: 16144636008425789881
---------------
Output Observed
---------------
Decrypt: 18236230773660754005
---------------
---------------
[MONITOR] - DEC Input Generated
---------------
Cipher: 178469423690467612 33
key:  3253416903612027591
---------------
Output Observed
---------------
Decrypt: 12520585440802170084
---------------
---------------
[Driver - DEC ] Input Generated
---------------
Cipher: 12883110298986591852
key:  6032319518772486038
---------------
Output Observed
---------------
Decrypt: 12520585440802170084
---------------
Result is as Expected
---------------
[ scoreboard - DEC ] Input Generated
---------------
Cipher: 178469423690467612 33
key:  3253416903612027591
---------------
```

```
Output Observed
---------------
Decrypt: 12520585440802170084
---------------
---------------
---------------
[ scoreboard - DEC ] Input Generated
---------------
Cipher:  8618482140819293235
key:  2364358994538099039
---------------
Output Observed
---------------
Decrypt:  5763753461411876001
---------------
---------------
[MONITOR] - DEC Input Generated
---------------
Cipher: 11622222891885614073
key: 16061465308326132233
---------------
Output Observed
---------------
Decrypt:  6547734564018643854
---------------
---------------
[Driver - DEC ] Input Generated
---------------
Cipher: 12972375568864080532
key: 13905086032251398467
---------------
Output Observed
---------------
Decrypt:  6547734564018643854
---------------
Result is as Expected
---------------
[ scoreboard - DEC ] Input Generated
---------------
Cipher: 11622222891885614073
key: 16061465308326132233
---------------
Output Observed
---------------
Decrypt:  6547734564018643854
---------------
---------------
[MONITOR] - DEC Input Generated
---------------
Cipher: 12972375568864080532
key: 13905086032251398467
---------------
Output Observed
---------------
Decrypt:  5473528933260726603
---------------
---------------
[Driver - DEC ] Input Generated
---------------
Cipher:  7376018977132262759
key:  1072107501481623877
---------------
Output Observed
---------------
Decrypt:  5473528933260726603
---------------
Result is as Expected
---------------
```

```
[ scoreboard - DEC ] Input Generated
---------------
Cipher: 12972375568864080532
key: 13905086032251398467
---------------
Output Observed
---------------
Decrypt:  5473528933260726603
---------------
---------------
[MONITOR] - DEC Input Generated
---------------
Cipher:  7376018977132262759
key:  1072107501481623877
---------------
Output Observed
---------------
Decrypt:  9810797851888919478
---------------
---------------
[Driver - DEC ] Input Generated
---------------
Cipher:  5435797305044568628
key: 10075920060711363075
---------------
Output Observed
---------------
Decrypt:  9810797851888919478
---------------
Result is as Expected
---------------
[ scoreboard - DEC ] Input Generated
---------------
Cipher:  7376018977132262759
key:  1072107501481623877
---------------
Output Observed
---------------
Decrypt:  9810797851888919478
---------------
---------------
[MONITOR] - DEC Input Generated
---------------
Cipher:  5435797305044568628
key: 10075920060711363075
---------------
Output Observed
---------------
Decrypt:  2372444054361381822
---------------
---------------
[Driver - DEC ] Input Generated
---------------
Cipher: 14507877660731744359
key: 15046724497961720539
---------------
Output Observed
---------------
Decrypt:  2372444054361381822
---------------
Result is as Expected
---------------
[ scoreboard - DEC ] Input Generated
---------------
Cipher:  5435797305044568628
key: 10075920060711363075
---------------
Output Observed
```

```
---------------
Decrypt:  2372444054361381822
---------------
---------------
[MONITOR] - DEC Input Generated
---------------
Cipher: 14507877660731744359
key: 15046724497961720539
---------------
Output Observed
---------------
Decrypt: 15704972676301482760
---------------
---------------
[Driver - DEC ] Input Generated
---------------
Cipher:  2210108667745784706
key:  6220908944756275614
---------------
Output Observed
---------------
Decrypt: 15704972676301482760
---------------
Result is as Expected
---------------
[ scoreboard - DEC ] Input Generated
---------------
Cipher: 14507877660731744359
key: 15046724497961720539
---------------
Output Observed
---------------
Decrypt: 15704972676301482760
---------------
---------------
[MONITOR] - DEC Input Generated
---------------
Cipher:  2210108667745784706
key:  6220908944756275614
---------------
Output Observed
---------------
Decrypt:  3238780143107699732
---------------
---------------
[Driver - DEC ] Input Generated
---------------
Cipher: 10742618028833940510
key:  1271127590112525846
---------------
Output Observed
---------------
Decrypt:  3238780143107699732
---------------
Result is as Expected
---------------
[ scoreboard - DEC ] Input Generated
---------------
Cipher:  2210108667745784706
key:  6220908944756275614
---------------
Output Observed
---------------
Decrypt:  3238780143107699732
---------------
---------------
[MONITOR] - DEC Input Generated
---------------
```

```
Cipher: 10742618028833940510
key:  1271127590112525846
---------------
Output Observed
---------------
Decrypt:  8495693232505307014
---------------
---------------
[Driver - DEC ] Input Generated
---------------
Cipher: 16676636027694377592
key:  7821013592900726439
---------------
Output Observed
---------------
Decrypt:  8495693232505307014
---------------
Result is as Expected
---------------
[ scoreboard - DEC ] Input Generated
---------------
Cipher: 10742618028833940510
key:  1271127590112525846
---------------
Output Observed
---------------
Decrypt:  8495693232505307014
---------------
---------------
[MONITOR] - DEC Input Generated
---------------
Cipher: 16676636027694377592
key:  7821013592900726439
---------------
Output Observed
---------------
Decrypt:  2605472850092683347
---------------
---------------
[Driver - DEC ] Input Generated
---------------
Cipher: 17038020110271968062
key: 14630111108593188340
---------------
Output Observed
---------------
Decrypt:  2605472850092683347
---------------
Result is as Expected
---------------
[ scoreboard - DEC ] Input Generated
---------------
Cipher: 16676636027694377592
key:  7821013592900726439
---------------
Output Observed
---------------
Decrypt:  2605472850092683347
---------------
---------------
[MONITOR] - DEC Input Generated
---------------
Cipher: 17038020110271968062
key: 14630111108593188340
---------------
Output Observed
---------------
Decrypt:  9055200035060399887
```

```
---------------
---------------
[Driver - DEC ] Input Generated
---------------
Cipher: 14275680192859870949
key: 17897506148814379365
---------------
Output Observed
---------------
Decrypt:  9055200035060399887
---------------
Result is as Expected
---------------
[ scoreboard - DEC ] Input Generated
---------------
Cipher: 17038020110271968062
key: 14630111108593188340
---------------
Output Observed
---------------
Decrypt:  9055200035060399887
---------------
Simulation complete via $finish(1) at time 405 NS + 1
./environment.sv:55        $finish;
```

15.1.3 Memory Block Log

```
#                    0, ENV::RUN PHASE
#                    0, TXGEN::RUN PHASE
#                    0, COVER::RUN PHASE
#                    0, DRV1::RUN PHASE
#                    0, DRV2::RUN PHASE
#                    0, MON1::RUN PHASE
#                    0, MON2::RUN PHASE
#                    0, SB::RUN PHASE
# expected packet='{data_in:129, addr:36, data_out:0, en:0, wr:0}
#                   10, driver1:written pkt.wr=0,pkt.addr=36,pkt.datain=129
#                   20, driver2:written pkt.wr=1,pkt.addr=36
#                   25, monitor2: read addr=36 dataout=129
# received pkt='{data_in:0, addr:36, data_out:129, en:1, wr:1}
#                   25, scoreboard---->MATCHED, pkt2.addr=36,pkt2.data_out=129
# expected packet='{data_in:99, addr:9, data_out:0, en:1, wr:0}
#                   30, driver1:written pkt.wr=0,pkt.addr= 9,pkt.datain= 99
#                   35, monitor2: read addr=36 dataout=129
# received pkt='{data_in:0, addr:36, data_out:129, en:1, wr:1}
#                   35, scoreboard---->MATCHED, pkt2.addr=36,pkt2.data_out=129
#                   40, driver2:written pkt.wr=1,pkt.addr= 9
#                   45, monitor2: read addr= 9 dataout= 99
# received pkt='{data_in:0, addr:9, data_out:99, en:1, wr:1}
#                   45, scoreboard---->MATCHED, pkt2.addr=9,pkt2.data_out=99
# expected packet='{data_in:141, addr:13, data_out:0, en:1, wr:0}
#                   50, driver1:written pkt.wr=0,pkt.addr=13,pkt.datain=141
#                   55, monitor2: read addr= 9 dataout= 99
# received pkt='{data_in:0, addr:9, data_out:99, en:1, wr:1}
#                   55, scoreboard---->MATCHED, pkt2.addr=9,pkt2.data_out=99
#                   60, driver2:written pkt.wr=1,pkt.addr=13
#                   65, monitor2: read addr=13 dataout=141
# received pkt='{data_in:0, addr:13, data_out:141, en:1, wr:1}
#                   65, scoreboard---->MATCHED, pkt2.addr=13,pkt2.data_out=141
# expected packet='{data_in:18, addr:37, data_out:0, en:1, wr:0}
#                   70, driver1:written pkt.wr=0,pkt.addr=37,pkt.datain= 18
#                   75, monitor2: read addr=13 dataout=141
# received pkt='{data_in:0, addr:13, data_out:141, en:1, wr:1}
#                   75, scoreboard---->MATCHED, pkt2.addr=13,pkt2.data_out=141
#                   80, driver2:written pkt.wr=1,pkt.addr=37
#                   85, monitor2: read addr=37 dataout= 18
# received pkt='{data_in:0, addr:37, data_out:18, en:1, wr:1}
```

```
#                   85, scoreboard---->MATCHED, pkt2.addr=37,pkt2.data_out=18
# expected packet='{data_in:13, addr:1, data_out:0, en:1, wr:0}
#                   90, driver1:written pkt.wr=0,pkt.addr= 1,pkt.datain= 13
#                   95, monitor2: read addr=37 dataout= 18
# received pkt='{data_in:0, addr:37, data_out:18, en:1, wr:1}
#                   95, scoreboard---->MATCHED, pkt2.addr=37,pkt2.data_out=18
#                  100, driver2:written pkt.wr=1,pkt.addr= 1
#                  105, monitor2: read addr= 1 dataout= 13
# received pkt='{data_in:0, addr:1, data_out:13, en:1, wr:1}
#                  105, scoreboard---->MATCHED, pkt2.addr=1,pkt2.data_out=13
# expected packet='{data_in:61, addr:54, data_out:0, en:1, wr:0}
#                  110, driver1:written pkt.wr=0,pkt.addr=54,pkt.datain= 61
#                  115, monitor2: read addr= 1 dataout= 13
# received pkt='{data_in:0, addr:1, data_out:13, en:1, wr:1}
#                  115, scoreboard---->MATCHED, pkt2.addr=1,pkt2.data_out=13
#                  120, driver2:written pkt.wr=1,pkt.addr=54
#                  125, monitor2: read addr=54 dataout= 61
# received pkt='{data_in:0, addr:54, data_out:61, en:1, wr:1}
#                  125, scoreboard---->MATCHED, pkt2.addr=54,pkt2.data_out=61
# expected packet='{data_in:140, addr:45, data_out:0, en:1, wr:0}
#                  130, driver1:written pkt.wr=0,pkt.addr=45,pkt.datain=140
#                  135, monitor2: read addr=54 dataout= 61
# received pkt='{data_in:0, addr:54, data_out:61, en:1, wr:1}
#                  135, scoreboard---->MATCHED, pkt2.addr=54,pkt2.data_out=61
#                  140, driver2:written pkt.wr=1,pkt.addr=45
#                  145, monitor2: read addr=45 dataout=140
# received pkt='{data_in:0, addr:45, data_out:140, en:1, wr:1}
#                  145, scoreboard---->MATCHED, pkt2.addr=45,pkt2.data_out=140
# expected packet='{data_in:198, addr:57, data_out:0, en:1, wr:0}
#                  150, driver1:written pkt.wr=0,pkt.addr=57,pkt.datain=198
#                  155, monitor2: read addr=45 dataout=140
# received pkt='{data_in:0, addr:45, data_out:140, en:1, wr:1}
#                  155, scoreboard---->MATCHED, pkt2.addr=45,pkt2.data_out=140
#                  160, driver2:written pkt.wr=1,pkt.addr=57
#                  165, monitor2: read addr=57 dataout=198
# received pkt='{data_in:0, addr:57, data_out:198, en:1, wr:1}
#                  165, scoreboard---->MATCHED, pkt2.addr=57,pkt2.data_out=198
# expected packet='{data_in:170, addr:5, data_out:0, en:1, wr:0}
#                  170, driver1:written pkt.wr=0,pkt.addr= 5,pkt.datain=170
#                  175, monitor2: read addr=57 dataout=198
# received pkt='{data_in:0, addr:57, data_out:198, en:1, wr:1}
#                  175, scoreboard---->MATCHED, pkt2.addr=57,pkt2.data_out=198
#                  180, driver2:written pkt.wr=1,pkt.addr= 5
#                  185, monitor2: read addr= 5 dataout=170
# received pkt='{data_in:0, addr:5, data_out:170, en:1, wr:1}
#                  185, scoreboard---->MATCHED, pkt2.addr=5,pkt2.data_out=170
# expected packet='{data_in:119, addr:37, data_out:0, en:1, wr:0}
#                  190, driver1:written pkt.wr=0,pkt.addr=37,pkt.datain=119
#                  195, monitor2: read addr= 5 dataout=170
# received pkt='{data_in:0, addr:5, data_out:170, en:1, wr:1}
#                  195, scoreboard---->MATCHED, pkt2.addr=5,pkt2.data_out=170
#                  200, COVER::RUN PHASE
#                  200, driver2:written pkt.wr=1,pkt.addr=37
#                  205, monitor2: read addr=37 dataout=119
# received pkt='{data_in:0, addr:37, data_out:119, en:1, wr:1}
#                  205, scoreboard---->MATCHED, pkt2.addr=37,pkt2.data_out=119
# expected packet='{data_in:143, addr:18, data_out:0, en:1, wr:0}
#                  210, driver1:written pkt.wr=0,pkt.addr=18,pkt.datain=143
#                  215, monitor2: read addr=37 dataout=119
# received pkt='{data_in:0, addr:37, data_out:119, en:1, wr:1}
#                  215, scoreboard---->MATCHED, pkt2.addr=37,pkt2.data_out=119
#                  220, driver2:written pkt.wr=1,pkt.addr=18
#                  225, monitor2: read addr=18 dataout=143
# received pkt='{data_in:0, addr:18, data_out:143, en:1, wr:1}
#                  225, scoreboard---->MATCHED, pkt2.addr=18,pkt2.data_out=143
# expected packet='{data_in:206, addr:50, data_out:0, en:1, wr:0}
#                  230, driver1:written pkt.wr=0,pkt.addr=50,pkt.datain=206
#                  235, monitor2: read addr=18 dataout=143
```

```
# received pkt='{data_in:0, addr:18, data_out:143, en:1, wr:1}
#                  235, scoreboard---->MATCHED, pkt2.addr=18,pkt2.data_out=143
#                  240, driver2:written pkt.wr=1,pkt.addr=50
#                  245, monitor2: read addr=50 dataout=206
# received pkt='{data_in:0, addr:50, data_out:206, en:1, wr:1}
#                  245, scoreboard---->MATCHED, pkt2.addr=50,pkt2.data_out=206
# expected packet='{data_in:197, addr:40, data_out:0, en:1, wr:0}
#                  250, driver1:written pkt.wr=0,pkt.addr=40,pkt.datain=197
#                  255, monitor2: read addr=50 dataout=206
# received pkt='{data_in:0, addr:50, data_out:206, en:1, wr:1}
#                  255, scoreboard---->MATCHED, pkt2.addr=50,pkt2.data_out=206
#                  260, driver2:written pkt.wr=1,pkt.addr=40
#                  265, monitor2: read addr=40 dataout=197
# received pkt='{data_in:0, addr:40, data_out:197, en:1, wr:1}
#                  265, scoreboard---->MATCHED, pkt2.addr=40,pkt2.data_out=197
# expected packet='{data_in:189, addr:28, data_out:0, en:1, wr:0}
#                  270, driver1:written pkt.wr=0,pkt.addr=28,pkt.datain=189
#                  275, monitor2: read addr=40 dataout=197
# received pkt='{data_in:0, addr:40, data_out:197, en:1, wr:1}
#                  275, scoreboard---->MATCHED, pkt2.addr=40,pkt2.data_out=197
#                  280, driver2:written pkt.wr=1,pkt.addr=28
#                  285, monitor2: read addr=28 dataout=189
# received pkt='{data_in:0, addr:28, data_out:189, en:1, wr:1}
#                  285, scoreboard---->MATCHED, pkt2.addr=28,pkt2.data_out=189
# expected packet='{data_in:101, addr:45, data_out:0, en:1, wr:0}
#                  290, driver1:written pkt.wr=0,pkt.addr=45,pkt.datain=101
#                  295, monitor2: read addr=28 dataout=189
# received pkt='{data_in:0, addr:28, data_out:189, en:1, wr:1}
#                  295, scoreboard---->MATCHED, pkt2.addr=28,pkt2.data_out=189
#                  300, driver2:written pkt.wr=1,pkt.addr=45
#                  305, monitor2: read addr=45 dataout=101
# received pkt='{data_in:0, addr:45, data_out:101, en:1, wr:1}
#                  305, scoreboard---->MATCHED, pkt2.addr=45,pkt2.data_out=101
# expected packet='{data_in:10, addr:35, data_out:0, en:1, wr:0}
#                  310, driver1:written pkt.wr=0,pkt.addr=35,pkt.datain= 10
#                  315, monitor2: read addr=45 dataout=101
# received pkt='{data_in:0, addr:45, data_out:101, en:1, wr:1}
#                  315, scoreboard---->MATCHED, pkt2.addr=45,pkt2.data_out=101
#                  320, driver2:written pkt.wr=1,pkt.addr=35
#                  325, monitor2: read addr=35 dataout= 10
# received pkt='{data_in:0, addr:35, data_out:10, en:1, wr:1}
#                  325, scoreboard---->MATCHED, pkt2.addr=35,pkt2.data_out=10
# expected packet='{data_in:32, addr:0, data_out:0, en:1, wr:0}
#                  330, driver1:written pkt.wr=0,pkt.addr= 0,pkt.datain= 32
#                  335, monitor2: read addr=35 dataout= 10
# received pkt='{data_in:0, addr:35, data_out:10, en:1, wr:1}
#                  335, scoreboard---->MATCHED, pkt2.addr=35,pkt2.data_out=10
#                  340, driver2:written pkt.wr=1,pkt.addr= 0
#                  345, monitor2: read addr= 0 dataout= 32
# received pkt='{data_in:0, addr:0, data_out:32, en:1, wr:1}
#                  345, scoreboard---->MATCHED, pkt2.addr=0,pkt2.data_out=32
# expected packet='{data_in:157, addr:42, data_out:0, en:1, wr:0}
#                  350, driver1:written pkt.wr=0,pkt.addr=42,pkt.datain=157
#                  355, monitor2: read addr= 0 dataout= 32
# received pkt='{data_in:0, addr:0, data_out:32, en:1, wr:1}
#                  355, scoreboard---->MATCHED, pkt2.addr=0,pkt2.data_out=32
#                  360, driver2:written pkt.wr=1,pkt.addr=42
#                  365, monitor2: read addr=42 dataout=157
# received pkt='{data_in:0, addr:42, data_out:157, en:1, wr:1}
#                  365, scoreboard---->MATCHED, pkt2.addr=42,pkt2.data_out=157
# expected packet='{data_in:19, addr:22, data_out:0, en:1, wr:0}
#                  370, driver1:written pkt.wr=0,pkt.addr=22,pkt.datain= 19
#                  375, monitor2: read addr=42 dataout=157
# received pkt='{data_in:0, addr:42, data_out:157, en:1, wr:1}
#                  375, scoreboard---->MATCHED, pkt2.addr=42,pkt2.data_out=157
#                  380, driver2:written pkt.wr=1,pkt.addr=22
#                  385, monitor2: read addr=22 dataout= 19
# received pkt='{data_in:0, addr:22, data_out:19, en:1, wr:1}
```

```
#                   385, scoreboard---->MATCHED, pkt2.addr=22,pkt2.data_out=19
# expected packet='{data_in:83, addr:13, data_out:0, en:1, wr:0}
#                   390, driver1:written pkt.wr=0,pkt.addr=13,pkt.datain= 83
#                   395, monitor2: read addr=22 dataout= 19
# received pkt='{data_in:0, addr:22, data_out:19, en:1, wr:1}
#                   395, scoreboard---->MATCHED, pkt2.addr=22,pkt2.data_out=19
#                   400, COVER::RUN PHASE
#                   400, driver2:written pkt.wr=1,pkt.addr=13
#                   405, monitor2: read addr=13 dataout= 83
# received pkt='{data_in:0, addr:13, data_out:83, en:1, wr:1}
#                   405, scoreboard---->MATCHED, pkt2.addr=13,pkt2.data_out=83
# expected packet='{data_in:213, addr:43, data_out:0, en:1, wr:0}
#                   410, driver1:written pkt.wr=0,pkt.addr=43,pkt.datain=213
#                   415, monitor2: read addr=13 dataout= 83
# received pkt='{data_in:0, addr:13, data_out:83, en:1, wr:1}
#                   415, scoreboard---->MATCHED, pkt2.addr=13,pkt2.data_out=83
#                   420, driver2:written pkt.wr=1,pkt.addr=43
#                   425, monitor2: read addr=43 dataout=213
# received pkt='{data_in:0, addr:43, data_out:213, en:1, wr:1}
#                   425, scoreboard---->MATCHED, pkt2.addr=43,pkt2.data_out=213
# expected packet='{data_in:174, addr:2, data_out:0, en:1, wr:0}
#                   430, driver1:written pkt.wr=0,pkt.addr= 2,pkt.datain=174
#                   435, monitor2: read addr=43 dataout=213
# received pkt='{data_in:0, addr:43, data_out:213, en:1, wr:1}
#                   435, scoreboard---->MATCHED, pkt2.addr=43,pkt2.data_out=213
#                   440, driver2:written pkt.wr=1,pkt.addr= 2
#                   445, monitor2: read addr= 2 dataout=174
# received pkt='{data_in:0, addr:2, data_out:174, en:1, wr:1}
#                   445, scoreboard---->MATCHED, pkt2.addr=2,pkt2.data_out=174
# expected packet='{data_in:207, addr:29, data_out:0, en:1, wr:0}
#                   450, driver1:written pkt.wr=0,pkt.addr=29,pkt.datain=207
#                   455, monitor2: read addr= 2 dataout=174
# received pkt='{data_in:0, addr:2, data_out:174, en:1, wr:1}
#                   455, scoreboard---->MATCHED, pkt2.addr=2,pkt2.data_out=174
#                   460, driver2:written pkt.wr=1,pkt.addr=29
#                   465, monitor2: read addr=29 dataout=207
# received pkt='{data_in:0, addr:29, data_out:207, en:1, wr:1}
#                   465, scoreboard---->MATCHED, pkt2.addr=29,pkt2.data_out=207
# expected packet='{data_in:10, addr:35, data_out:0, en:1, wr:0}
#                   470, driver1:written pkt.wr=0,pkt.addr=35,pkt.datain= 10
#                   475, monitor2: read addr=29 dataout=207
# received pkt='{data_in:0, addr:29, data_out:207, en:1, wr:1}
#                   475, scoreboard---->MATCHED, pkt2.addr=29,pkt2.data_out=207
#                   480, driver2:written pkt.wr=1,pkt.addr=35
#                   485, monitor2: read addr=35 dataout= 10
# received pkt='{data_in:0, addr:35, data_out:10, en:1, wr:1}
#                   485, scoreboard---->MATCHED, pkt2.addr=35,pkt2.data_out=10
# expected packet='{data_in:60, addr:10, data_out:0, en:1, wr:0}
#                   490, driver1:written pkt.wr=0,pkt.addr=10,pkt.datain= 60
#                   495, monitor2: read addr=35 dataout= 10
# received pkt='{data_in:0, addr:35, data_out:10, en:1, wr:1}
#                   495, scoreboard---->MATCHED, pkt2.addr=35,pkt2.data_out=10
#                   500, driver2:written pkt.wr=1,pkt.addr=10
#                   505, monitor2: read addr=10 dataout= 60
# received pkt='{data_in:0, addr:10, data_out:60, en:1, wr:1}
#                   505, scoreboard---->MATCHED, pkt2.addr=10,pkt2.data_out=60
# expected packet='{data_in:138, addr:50, data_out:0, en:1, wr:0}
#                   510, driver1:written pkt.wr=0,pkt.addr=50,pkt.datain=138
#                   515, monitor2: read addr=10 dataout= 60
# received pkt='{data_in:0, addr:10, data_out:60, en:1, wr:1}
#                   515, scoreboard---->MATCHED, pkt2.addr=10,pkt2.data_out=60
#                   520, driver2:written pkt.wr=1,pkt.addr=50
#                   525, monitor2: read addr=50 dataout=138
# received pkt='{data_in:0, addr:50, data_out:138, en:1, wr:1}
#                   525, scoreboard---->MATCHED, pkt2.addr=50,pkt2.data_out=138
# expected packet='{data_in:216, addr:1, data_out:0, en:1, wr:0}
#                   530, driver1:written pkt.wr=0,pkt.addr= 1,pkt.datain=216
#                   535, monitor2: read addr=50 dataout=138
```

```
# received pkt='{data_in:0, addr:50, data_out:138, en:1, wr:1}
#                  535, scoreboard---->MATCHED, pkt2.addr=50,pkt2.data_out=138
#                  540, driver2:written pkt.wr=1,pkt.addr= 1
#                  545, monitor2: read addr= 1 dataout=216
# received pkt='{data_in:0, addr:1, data_out:216, en:1, wr:1}
#                  545, scoreboard---->MATCHED, pkt2.addr=1,pkt2.data_out=216
# expected packet='{data_in:137, addr:56, data_out:0, en:1, wr:0}
#                  550, driver1:written pkt.wr=0,pkt.addr=56,pkt.datain=137
#                  555, monitor2: read addr= 1 dataout=216
# received pkt='{data_in:0, addr:1, data_out:216, en:1, wr:1}
#                  555, scoreboard---->MATCHED, pkt2.addr=1,pkt2.data_out=216
#                  560, driver2:written pkt.wr=1,pkt.addr=56
#                  565, monitor2: read addr=56 dataout=137
# received pkt='{data_in:0, addr:56, data_out:137, en:1, wr:1}
#                  565, scoreboard---->MATCHED, pkt2.addr=56,pkt2.data_out=137
# expected packet='{data_in:182, addr:43, data_out:0, en:1, wr:0}
#                  570, driver1:written pkt.wr=0,pkt.addr=43,pkt.datain=182
#                  575, monitor2: read addr=56 dataout=137
# received pkt='{data_in:0, addr:56, data_out:137, en:1, wr:1}
#                  575, scoreboard---->MATCHED, pkt2.addr=56,pkt2.data_out=137
#                  580, driver2:written pkt.wr=1,pkt.addr=43
#                  585, monitor2: read addr=43 dataout=182
# received pkt='{data_in:0, addr:43, data_out:182, en:1, wr:1}
#                  585, scoreboard---->MATCHED, pkt2.addr=43,pkt2.data_out=182
# expected packet='{data_in:174, addr:6, data_out:0, en:1, wr:0}
#                  590, driver1:written pkt.wr=0,pkt.addr= 6,pkt.datain=174
#                  595, monitor2: read addr=43 dataout=182
# received pkt='{data_in:0, addr:43, data_out:182, en:1, wr:1}
#                  595, scoreboard---->MATCHED, pkt2.addr=43,pkt2.data_out=182
#                  600, COVER::RUN PHASE
#                  600, driver2:written pkt.wr=1,pkt.addr= 6
#                  605, monitor2: read addr= 6 dataout=174
# expected packet='{data_in:81, addr:23, data_out:0, en:1, wr:0}
#                  850, driver1:written pkt.wr=0,pkt.addr=23,pkt.datain= 81
#                  855, monitor2: read addr= 9 dataout=208
# received pkt='{data_in:0, addr:9, data_out:208, en:1, wr:1}
#                  855, scoreboard---->MATCHED, pkt2.addr=9,pkt2.data_out=208
#                  860, driver2:written pkt.wr=1,pkt.addr=23
#                  865, monitor2: read addr=23 dataout= 81
# received pkt='{data_in:0, addr:23, data_out:81, en:1, wr:1}
#                  865, scoreboard---->MATCHED, pkt2.addr=23,pkt2.data_out=81
# expected packet='{data_in:12, addr:22, data_out:0, en:1, wr:0}
#                  870, driver1:written pkt.wr=0,pkt.addr=22,pkt.datain= 12
#                  875, monitor2: read addr=23 dataout= 81
# received pkt='{data_in:0, addr:23, data_out:81, en:1, wr:1}
#                  875, scoreboard---->MATCHED, pkt2.addr=23,pkt2.data_out=81
#                  880, driver2:written pkt.wr=1,pkt.addr=22
#                  885, monitor2: read addr=22 dataout= 12
# received pkt='{data_in:0, addr:22, data_out:12, en:1, wr:1}
#                  885, scoreboard---->MATCHED, pkt2.addr=22,pkt2.data_out=12
# expected packet='{data_in:200, addr:2, data_out:0, en:1, wr:0}
#                  890, driver1:written pkt.wr=0,pkt.addr= 2,pkt.datain=200
#                  895, monitor2: read addr=22 dataout= 12
# received pkt='{data_in:0, addr:22, data_out:12, en:1, wr:1}
#                  895, scoreboard---->MATCHED, pkt2.addr=22,pkt2.data_out=12
#                  900, driver2:written pkt.wr=1,pkt.addr= 2
#                  905, monitor2: read addr= 2 dataout=200
# received pkt='{data_in:0, addr:2, data_out:200, en:1, wr:1}
#                  905, scoreboard---->MATCHED, pkt2.addr=2,pkt2.data_out=200
# expected packet='{data_in:61, addr:55, data_out:0, en:1, wr:0}
#                  910, driver1:written pkt.wr=0,pkt.addr=55,pkt.datain= 61
#                  915, monitor2: read addr= 2 dataout=200
# received pkt='{data_in:0, addr:2, data_out:200, en:1, wr:1}
#                  915, scoreboard---->MATCHED, pkt2.addr=2,pkt2.data_out=200
#                  920, driver2:written pkt.wr=1,pkt.addr=55
#                  925, monitor2: read addr=55 dataout= 61
# received pkt='{data_in:0, addr:55, data_out:61, en:1, wr:1}
#                  925, scoreboard---->MATCHED, pkt2.addr=55,pkt2.data_out=61
```

```
# expected packet='{data_in:126, addr:18, data_out:0, en:1, wr:0}
#                  930, driver1:written pkt.wr=0,pkt.addr=18,pkt.datain=126
#                  935, monitor2: read addr=55 dataout= 61
# received pkt='{data_in:0, addr:55, data_out:61, en:1, wr:1}
#                  935, scoreboard---->MATCHED, pkt2.addr=55,pkt2.data_out=61
#                  940, driver2:written pkt.wr=1,pkt.addr=18
#                  945, monitor2: read addr=18 dataout=126
# received pkt='{data_in:0, addr:18, data_out:126, en:1, wr:1}
#                  945, scoreboard---->MATCHED, pkt2.addr=18,pkt2.data_out=126
# expected packet='{data_in:57, addr:45, data_out:0, en:1, wr:0}
#                  950, driver1:written pkt.wr=0,pkt.addr=45,pkt.datain= 57
#                  955, monitor2: read addr=18 dataout=126
# received pkt='{data_in:0, addr:18, data_out:126, en:1, wr:1}
#                  955, scoreboard---->MATCHED, pkt2.addr=18,pkt2.data_out=126
#                  960, driver2:written pkt.wr=1,pkt.addr=45
#                  965, monitor2: read addr=45 dataout= 57
# received pkt='{data_in:0, addr:45, data_out:57, en:1, wr:1}
#                  965, scoreboard---->MATCHED, pkt2.addr=45,pkt2.data_out=57
# expected packet='{data_in:211, addr:31, data_out:0, en:1, wr:0}
#                  970, driver1:written pkt.wr=0,pkt.addr=31,pkt.datain=211
#                  975, monitor2: read addr=45 dataout= 57
# received pkt='{data_in:0, addr:45, data_out:57, en:1, wr:1}
#                  975, scoreboard---->MATCHED, pkt2.addr=45,pkt2.data_out=57
#                  980, driver2:written pkt.wr=1,pkt.addr=31
#                  985, monitor2: read addr=31 dataout=211
# received pkt='{data_in:0, addr:31, data_out:211, en:1, wr:1}
#                  985, scoreboard---->MATCHED, pkt2.addr=31,pkt2.data_out=211
# expected packet='{data_in:120, addr:5, data_out:0, en:1, wr:0}
#                  990, driver1:written pkt.wr=0,pkt.addr= 5,pkt.datain=120
#                  995, monitor2: read addr=31 dataout=211
# received pkt='{data_in:0, addr:31, data_out:211, en:1, wr:1}
#                  995, scoreboard---->MATCHED, pkt2.addr=31,pkt2.data_out=211
#                 1000, COVER::RUN PHASE
#                 1000, driver2:written pkt.wr=1,pkt.addr= 5
```

15.1.4 Memory Block Coverage Report

```
# Coverage Report Summary Data by file
#
# ================================================================================
# === File: cov.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                            8         8         0     100.0
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: drv1.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           13        13         0     100.0
#     Branches                         2         1         1      50.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
```

```
# === File: drv2.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           12        12         0     100.0
#     Branches                         2         1         1      50.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: dut.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           10         5         5      50.0
#     Branches                         6         3         3      50.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: env.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           27        26         1      96.2
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: interface.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                            1         1         0     100.0
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                     96        58        38      60.4
#
# ================================================================================
# === File: mon1.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           12         7         5      58.3
#     Branches                         2         1         1      50.0
#     FEC Condition Terms              2         0         2       0.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
```

```
#
# ================================================================================
# === File: mon2.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           12        12         0     100.0
#     Branches                         2         2         0     100.0
#     FEC Condition Terms              2         1         1      50.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: sb.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           16        15         1      93.7
#     Branches                         2         1         1      50.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: test.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                            7         7         0     100.0
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: top.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                            2         2         0     100.0
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      2         2         0     100.0
#
# ================================================================================
# === File: txgen.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           48        27        21      56.2
#     Branches                        16         3        13      18.7
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
```

```
#         Transitions                    0         0         0     100.0
#     Toggle Bins                        0         0         0     100.0
#
#
# TOTAL COVERGROUP COVERAGE: 66.6%  COVERGROUP TYPES: 1
#
# Total Coverage By File (code coverage only, filtered view): 51.0%
```

15.2 Log file Each Modules of UVM Verification Approach

15.2.1 Encryption Block Log

```
run -all
# ----------------------------------------------------------------
# UVM-1.1d
# (C) 2007-2013 Mentor Graphics Corporation
# (C) 2007-2013 Cadence Design Systems, Inc.
# (C) 2006-2013 Synopsys, Inc.
# (C) 2011-2013 Cypress Semiconductor Corp.
# ----------------------------------------------------------------
#
#   ***********       IMPORTANT RELEASE NOTES         ************
#
#   You are using a version of the UVM library that has been compiled
#   with `UVM_NO_DEPRECATED undefined.
#   See http://www.eda.org/svdb/view.php?id=3313 for more details.
#
#   You are using a version of the UVM library that has been compiled
#   with `UVM_OBJECT_MUST_HAVE_CONSTRUCTOR undefined.
#   See http://www.eda.org/svdb/view.php?id=3770 for more details.
#
#       (Specify +UVM_NO_RELNOTES to turn off this notice)
#
# UVM_INFO @ 0: reporter [RNTST] Running test enc_test...
# UVM_INFO @ 0: reporter [UVMTOP] UVM testbench topology:
# ------------------------------------------------------------------------
# Name                              Type                      Size  Value
# ------------------------------------------------------------------------
# uvm_test_top                      enc_test                  -     @449
#   env_h                           enc_env                   -     @461
#     enc_agent_h                   enc_agent                 -     @469
#       enc_cov                     enc_coverage_subscriber   -     @647
#         analysis_imp              uvm_analysis_imp          -     @655
#         enc_item_collected_export uvm_analysis_imp          -     @664
#       enc_drvr                    enc_driver                -     @605
#         rsp_port                  uvm_analysis_port         -     @622
#         seq_item_port             uvm_seq_item_pull_port    -     @613
#       enc_mon                     enc_monitor               -     @631
#         enc_monitor_analysis_port uvm_analysis_port         -     @675
#       enc_scbd                    enc_scoreboard            -     @639
#         enc_item_collected_export uvm_analysis_imp          -     @684
#       enc_seqr                    uvm_sequencer             -     @482
#         rsp_export                uvm_analysis_export       -     @490
#         seq_item_export           uvm_seq_item_pull_imp     -     @596
#         arbitration_queue         array                     0     -
#         lock_queue                array                     0     -
#         num_last_reqs             integral                  32    'd1
#         num_last_rsps             integral                  32    'd1
# ------------------------------------------------------------------------
#
# UVM_INFO subscriber.sv(44) @ 20: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 20, Coverage = 0.10 percent
#
# UVM_INFO scoreboard.sv(19) @ 20: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 20, printing msg=14310035277244445416, key=16999359728124721280,
cipher=12142750337192573159
# UVM_INFO subscriber.sv(44) @ 30: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 30, Coverage = 0.20 percent
#
```

```
# UVM_INFO scoreboard.sv(19) @ 30: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 30, printing msg=10694209648348820869, key=1976729415530164205,
cipher=17581631574361877043
# UVM_INFO subscriber.sv(44) @ 40: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 40, Coverage = 0.30 percent
#
# UVM_INFO scoreboard.sv(19) @ 40: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 40, printing msg=12801552420224334234, key=48730340407549740 54,
cipher=13571370320103855514
# UVM_INFO subscriber.sv(44) @ 50: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 50, Coverage = 0.40 percent
#
# UVM_INFO scoreboard.sv(19) @ 50: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 50, printing msg=18426795528907150818, key=4771973521274585516,
cipher=10488177373946894180
# UVM_INFO subscriber.sv(44) @ 60: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 60, Coverage = 0.50 percent
#
# UVM_INFO scoreboard.sv(19) @ 60: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 60, printing msg=517883075019798009, key=14501131563226561037,
cipher=17969565696465901213
# UVM_INFO subscriber.sv(44) @ 70: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 70, Coverage = 0.60 percent
#
# UVM_INFO scoreboard.sv(19) @ 70: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 70, printing msg=94764990621911471 56, key=7697584164552131881,
cipher=7869295473948398164
# UVM_INFO subscriber.sv(44) @ 80: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 80, Coverage = 0.70 percent
#
# UVM_INFO scoreboard.sv(19) @ 80: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 80, printing msg=18113685055991348537, key=1297147198978071241,
cipher=12105788050767300194
# UVM_INFO subscriber.sv(44) @ 90: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 90, Coverage = 0.80 percent
#
# UVM_INFO scoreboard.sv(19) @ 90: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 90, printing msg=13987721988329036078, key=14137253176108882845,
cipher=3307862428529108425
# UVM_INFO subscriber.sv(44) @ 100: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 100, Coverage = 0.90 percent
#
# UVM_INFO scoreboard.sv(19) @ 100: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 100, printing msg=17424364973157137075, key=18111859085850284933,
cipher=13242601465072199979
# UVM_INFO subscriber.sv(44) @ 110: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 110, Coverage = 1.00 percent
#
# UVM_INFO scoreboard.sv(19) @ 110: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 110, printing msg=15848787036875907250, key=12050136951422917574,
cipher=17955040757285122883
# UVM_INFO subscriber.sv(44) @ 120: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 120, Coverage = 1.10 percent
#
# UVM_INFO scoreboard.sv(19) @ 120: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 120, printing msg=12920769019601436742, key=9203382368287887211,
cipher=21303938863840631 15
# UVM_INFO subscriber.sv(44) @ 130: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 130, Coverage = 1.20 percent
#
# UVM_INFO scoreboard.sv(19) @ 130: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 130, printing msg=9004269383181902251, key=1128223178613085515,
cipher=1829350011291069915
# UVM_INFO subscriber.sv(44) @ 140: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 140, Coverage = 1.30 percent
#
```

```
# UVM_INFO scoreboard.sv(19) @ 140: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 140, printing msg=12743140003382796216, key=17501973103843086996,
cipher=4889113132806283182
# UVM_INFO subscriber.sv(44) @ 150: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 150, Coverage = 1.40 percent
#
# UVM_INFO scoreboard.sv(19) @ 150: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 150, printing msg=11221133271317738698, key=6016314774451866666,
cipher=17244479093230285223
# UVM_INFO subscriber.sv(44) @ 160: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 160, Coverage = 1.50 percent
#
# UVM_INFO scoreboard.sv(19) @ 160: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 160, printing msg=12117049029128627673, key=5224192781181124651,
cipher=16801320523073685035
# UVM_INFO subscriber.sv(44) @ 170: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 170, Coverage = 1.60 percent
#
# UVM_INFO scoreboard.sv(19) @ 170: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 170, printing msg=21109052298202959 27, key=7717322548522352260,
cipher=5786875473342550715
# UVM_INFO subscriber.sv(44) @ 180: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 180, Coverage = 1.70 percent
#
# UVM_INFO scoreboard.sv(19) @ 180: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 180, printing msg=10597328805149921288, key=5756242677125582687,
cipher=11373134466538435164
# UVM_INFO subscriber.sv(44) @ 190: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 190, Coverage = 1.80 percent
#
# UVM_INFO scoreboard.sv(19) @ 190: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 190, printing msg=11410282261319127 05, key=16748479739351177928,
cipher=4579890567157714615
# UVM_INFO subscriber.sv(44) @ 200: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 200, Coverage = 1.90 percent
#
# UVM_INFO scoreboard.sv(19) @ 200: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 200, printing msg=87402234731270584 77, key=10866204282472781304,
cipher=11526880862525295578
# UVM_INFO subscriber.sv(44) @ 210: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 210, Coverage = 2.00 percent
#
# UVM_INFO scoreboard.sv(19) @ 210: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 210, printing msg=17214125467841909295, key=18413419733071378862,
cipher=17612729023063575705
# UVM_INFO subscriber.sv(44) @ 220: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 220, Coverage = 2.10 percent
#
# UVM_INFO scoreboard.sv(19) @ 220: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 220, printing msg=9932450640929924660, key=6815586971968426215,
cipher=8155430674992905548
# UVM_INFO subscriber.sv(44) @ 230: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 230, Coverage = 2.20 percent
#
# UVM_INFO scoreboard.sv(19) @ 230: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 230, printing msg=11340568990077289294, key=7169813362621056123,
cipher=871120306854603535
# UVM_INFO subscriber.sv(44) @ 240: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 240, Coverage = 2.30 percent
#
# UVM_INFO scoreboard.sv(19) @ 240: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 240, printing msg=13358275854570692561, key=6091332796688399153,
cipher=7713930655886910805
# UVM_INFO subscriber.sv(44) @ 250: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 250, Coverage = 2.40 percent
#
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# UVM_INFO scoreboard.sv(19) @ 250: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 250, printing msg=13160744704889580888, key=92575449456393448 61,
cipher=17508220110711120846
# UVM_INFO subscriber.sv(44) @ 260: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 260, Coverage = 2.46 percent
#
# UVM_INFO scoreboard.sv(19) @ 260: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 260, printing msg=5354420074072148793, key=7695930347175410639,
cipher=14097472338192205799
# UVM_INFO subscriber.sv(44) @ 270: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 270, Coverage = 2.56 percent
#
# UVM_INFO scoreboard.sv(19) @ 270: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 270, printing msg=57448307538035002 43, key=16467357052176955188,
cipher=16441500518104567327
# UVM_INFO subscriber.sv(44) @ 280: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 280, Coverage = 2.63 percent
#
# UVM_INFO scoreboard.sv(19) @ 280: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 280, printing msg=44196404421793058 34, key=5231484588643006784,
cipher=13325243026547295485
# UVM_INFO subscriber.sv(44) @ 290: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 290, Coverage = 2.73 percent
#
# UVM_INFO scoreboard.sv(19) @ 290: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 290, printing msg=50692962919036151 07, key=15489528967149645090,
cipher=17221712470969173804
# UVM_INFO subscriber.sv(44) @ 300: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 300, Coverage = 2.83 percent
#
# UVM_INFO scoreboard.sv(19) @ 300: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 300, printing msg=16379946784084954220, key=12997467127879432090,
cipher=11838446373385960852
# UVM_INFO subscriber.sv(44) @ 310: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 310, Coverage = 2.93 percent
#
# UVM_INFO scoreboard.sv(19) @ 310: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 310, printing msg=672059729305446569, key=7781374585819994670,
cipher=55845145117797001
# UVM_INFO subscriber.sv(44) @ 320: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 320, Coverage = 3.03 percent
#
# UVM_INFO scoreboard.sv(19) @ 320: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 320, printing msg=17863657841621700102, key=14124948787195877799,
cipher=14529576163012126519
# UVM_INFO subscriber.sv(44) @ 330: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 330, Coverage = 3.09 percent
#
# UVM_INFO scoreboard.sv(19) @ 330: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 330, printing msg=67010060543982199 44, key=92486841694832280 72,
cipher=15430864002564925423
# UVM_INFO subscriber.sv(44) @ 340: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 340, Coverage = 3.19 percent
#
# UVM_INFO scoreboard.sv(19) @ 340: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 340, printing msg=88764134768485396 10, key=10292551512885755909,
cipher=49081856310234913 90
# UVM_INFO subscriber.sv(44) @ 350: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 350, Coverage = 3.29 percent
#
# UVM_INFO scoreboard.sv(19) @ 350: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 350, printing msg=16977617532572681895, key=15218148871577875062,
cipher=4550896051290941995
# UVM_INFO subscriber.sv(44) @ 360: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 360, Coverage = 3.39 percent
#
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# UVM_INFO scoreboard.sv(19) @ 360: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 360, printing msg=17237344685952573796, key=7946475784856793339,
cipher=18030842440900707733
# UVM_INFO subscriber.sv(44) @ 370: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 370, Coverage = 3.46 percent
#
# UVM_INFO scoreboard.sv(19) @ 370: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 370, printing msg=7667596186126968040, key=40283266404604181067,
cipher=4588186241662064360
# UVM_INFO subscriber.sv(44) @ 380: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 380, Coverage = 3.56 percent
#
# UVM_INFO scoreboard.sv(19) @ 380: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 380, printing msg=777557808206661041, key=5068112847723855125,
cipher=18011382820753348374
# UVM_INFO subscriber.sv(44) @ 390: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 390, Coverage = 3.66 percent
#
# UVM_INFO scoreboard.sv(19) @ 390: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 390, printing msg=2240554397863873876, key=14820841668944793370,
cipher=17347400629647727451
# UVM_INFO subscriber.sv(44) @ 400: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 400, Coverage = 3.76 percent
#
# UVM_INFO scoreboard.sv(19) @ 400: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 400, printing msg=12431492484103476281, key=11047087903520584531,
cipher=4504498967775484816
# UVM_INFO subscriber.sv(44) @ 410: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 410, Coverage = 3.83 percent
#
# UVM_INFO scoreboard.sv(19) @ 410: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 410, printing msg=7849266502224572281, key=6090123106632946806,
cipher=12421540030514679828
# UVM_INFO subscriber.sv(44) @ 420: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 420, Coverage = 3.93 percent
#
# UVM_INFO scoreboard.sv(19) @ 420: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 420, printing msg=9947213144434699541, key=14103304602248401703,
cipher=12711498324707496475
# UVM_INFO subscriber.sv(44) @ 430: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 430, Coverage = 3.99 percent
#
# UVM_INFO scoreboard.sv(19) @ 430: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 430, printing msg=15760822235752175086, key=16004348756715927848,
cipher=13559837246571202330
# UVM_INFO subscriber.sv(44) @ 440: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 440, Coverage = 4.09 percent
#
# UVM_INFO scoreboard.sv(19) @ 440: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 440, printing msg=12721056580817306505, key=2007319063036975425,
cipher=7155657467122940923
# UVM_INFO subscriber.sv(44) @ 450: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 450, Coverage = 4.16 percent
#
# UVM_INFO scoreboard.sv(19) @ 450: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 450, printing msg=11736819451041842913, key=716497546556482955 3,
cipher=13005077684711748359
# UVM_INFO subscriber.sv(44) @ 460: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 460, Coverage = 4.26 percent
#
# UVM_INFO scoreboard.sv(19) @ 460: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 460, printing msg=8534716089613098310, key=13998639383974191247,
cipher=2803621989129073706
# UVM_INFO subscriber.sv(44) @ 470: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 470, Coverage = 4.36 percent
#
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# UVM_INFO scoreboard.sv(19) @ 470: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 470, printing msg=1503855165982231071, key=3260304431475694399,
cipher=929144619978993818
# UVM_INFO subscriber.sv(44) @ 480: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 480, Coverage = 4.46 percent
#
# UVM_INFO scoreboard.sv(19) @ 480: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 480, printing msg=7375134581433993380, key=2732586116812614488,
cipher=2294944774200292043
# UVM_INFO subscriber.sv(44) @ 490: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 490, Coverage = 4.56 percent
#
# UVM_INFO scoreboard.sv(19) @ 490: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 490, printing msg=4772128543672447236, key=3181892317856966878,
cipher=226355123304387482
# UVM_INFO subscriber.sv(44) @ 500: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 500, Coverage = 4.66 percent
#
# UVM_INFO scoreboard.sv(19) @ 500: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 500, printing msg=14644533952091329205, key=13330230136900230322,
cipher=11239783218949023426
# UVM_INFO subscriber.sv(44) @ 510: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 510, Coverage = 4.76 percent
#
# UVM_INFO scoreboard.sv(19) @ 510: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 510, printing msg=7030506616785046388, key=7905755456289608489,
cipher=17938708318619295119
# UVM_INFO subscriber.sv(44) @ 520: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 520, Coverage = 4.86 percent
#
# UVM_INFO scoreboard.sv(19) @ 520: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 520, printing msg=6427945215303272616, key=15362139415906101185,
cipher=18404399916991671298
# UVM_INFO subscriber.sv(44) @ 530: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 530, Coverage = 4.96 percent
#
# UVM_INFO scoreboard.sv(19) @ 530: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 530, printing msg=9373972214139813533, key=5339009262015406267,
cipher=10422105673494259035
# UVM_INFO subscriber.sv(44) @ 540: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 540, Coverage = 5.06 percent
#
# UVM_INFO scoreboard.sv(19) @ 540: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 540, printing msg=14586435434502762155, key=140069967948191492,
cipher=11026395459863452264
# UVM_INFO subscriber.sv(44) @ 550: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 550, Coverage = 5.16 percent
#
# UVM_INFO scoreboard.sv(19) @ 550: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 550, printing msg=559269244536538518, key=12084293400109059930,
cipher=10593586195459058133
# UVM_INFO subscriber.sv(44) @ 560: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 560, Coverage = 5.26 percent
#
# UVM_INFO scoreboard.sv(19) @ 560: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 560, printing msg=3708580728494832230, key=10759830870312460579,
cipher=2920959810174864003
# UVM_INFO subscriber.sv(44) @ 570: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 570, Coverage = 5.36 percent
#
# UVM_INFO scoreboard.sv(19) @ 570: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 570, printing msg=7654504506043504974, key=5020704475775447548,
cipher=15564371275552647526
# UVM_INFO subscriber.sv(44) @ 580: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 580, Coverage = 5.46 percent
#
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# UVM_INFO scoreboard.sv(19) @ 580: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 580, printing msg=7466642056651104048, key=15065684692770126649,
cipher=6733464148443050661
# UVM_INFO subscriber.sv(44) @ 590: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 590, Coverage = 5.56 percent
#
# UVM_INFO scoreboard.sv(19) @ 590: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 590, printing msg=9829714407424542524, key=13898477540024855261,
cipher=13352007335106267310
# UVM_INFO subscriber.sv(44) @ 600: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 600, Coverage = 5.66 percent
#
# UVM_INFO scoreboard.sv(19) @ 600: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 600, printing msg=7595890143831952278, key=5709489696522948290,
cipher=13946683006696115861
# UVM_INFO subscriber.sv(44) @ 610: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 610, Coverage = 5.76 percent
#
# UVM_INFO scoreboard.sv(19) @ 610: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 610, printing msg=6341991816447919135, key=3223415577390254787,
cipher=7482336346468483774
# UVM_INFO subscriber.sv(44) @ 620: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 620, Coverage = 5.85 percent
#
# UVM_INFO scoreboard.sv(19) @ 620: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 620, printing msg=11354552862540637362, key=18042480145319584071,
cipher=11099336539822846902
# UVM_INFO subscriber.sv(44) @ 630: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 630, Coverage = 5.95 percent
#
# UVM_INFO scoreboard.sv(19) @ 630: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 630, printing msg=12218554897422005345, key=16813494824760341625,
cipher=5640885542197095880
# UVM_INFO subscriber.sv(44) @ 640: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 640, Coverage = 6.05 percent
#
# UVM_INFO scoreboard.sv(19) @ 640: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 640, printing msg=8754839831707345016, key=4208846359212604002,
cipher=4352788900136603628
# UVM_INFO subscriber.sv(44) @ 650: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 650, Coverage = 6.15 percent
#
# UVM_INFO scoreboard.sv(19) @ 650: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 650, printing msg=7255496700952513950, key=8402781654288822787,
cipher=2973772431369902437
# UVM_INFO subscriber.sv(44) @ 660: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 660, Coverage = 6.25 percent
#
# UVM_INFO scoreboard.sv(19) @ 660: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 660, printing msg=4984914564148550920, key=13420422744522116554,
cipher=17367253896346541105
# UVM_INFO subscriber.sv(44) @ 670: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 670, Coverage = 6.35 percent
#
# UVM_INFO scoreboard.sv(19) @ 670: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 670, printing msg=13010001179203831500, key=10139651251571755211,
cipher=4098505945932761704
# UVM_INFO subscriber.sv(44) @ 680: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 680, Coverage = 6.45 percent
#
# UVM_INFO scoreboard.sv(19) @ 680: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 680, printing msg=4739451218136446349, key=5610795158615914733,
cipher=9679373273328200541
# UVM_INFO subscriber.sv(44) @ 690: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 690, Coverage = 6.55 percent
#
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# UVM_INFO scoreboard.sv(19) @ 690: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 690, printing msg=17516753475248146452, key=1192249295584899411,
cipher=15113922807623106155
# UVM_INFO subscriber.sv(44) @ 700: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 700, Coverage = 6.65 percent
#
# UVM_INFO scoreboard.sv(19) @ 700: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 700, printing msg=1875020964149604788, key=14233411313981196509,
cipher=8271859761086513743
# UVM_INFO subscriber.sv(44) @ 710: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 710, Coverage = 6.75 percent
#
# UVM_INFO scoreboard.sv(19) @ 710: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 710, printing msg=584483472540872695, key=17426468450073434451,
cipher=15893248150056386700
# UVM_INFO subscriber.sv(44) @ 720: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 720, Coverage = 6.85 percent
#
# UVM_INFO scoreboard.sv(19) @ 720: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 720, printing msg=5911743520450674217, key=10416343342132787127,
cipher=3825495421100802384
# UVM_INFO subscriber.sv(44) @ 730: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 730, Coverage = 6.95 percent
#
# UVM_INFO scoreboard.sv(19) @ 730: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 730, printing msg=6979897607105549484, key=504694519410495312,
cipher=6334178323834582935
# UVM_INFO subscriber.sv(44) @ 740: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 740, Coverage = 7.05 percent
#
# UVM_INFO scoreboard.sv(19) @ 740: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 740, printing msg=1155937842400920654, key=3461352764890621691,
cipher=10475430912533979944
# UVM_INFO subscriber.sv(44) @ 750: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 750, Coverage = 7.15 percent
#
# UVM_INFO scoreboard.sv(19) @ 750: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 750, printing msg=4498376248313556972, key=13647705041255593975,
cipher=18186975246169806669
# UVM_INFO subscriber.sv(44) @ 760: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 760, Coverage = 7.25 percent
#
# UVM_INFO scoreboard.sv(19) @ 760: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 760, printing msg=9398676742604419156, key=2819829157447072139,
cipher=12887020902404147007
# UVM_INFO subscriber.sv(44) @ 770: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 770, Coverage = 7.35 percent
#
# UVM_INFO scoreboard.sv(19) @ 770: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 770, printing msg=17943887028377410071, key=7021523316723455647,
cipher=2396192173303795951
# UVM_INFO subscriber.sv(44) @ 780: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 780, Coverage = 7.45 percent
#
# UVM_INFO scoreboard.sv(19) @ 780: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 780, printing msg=12406054648509407072, key=1625504890280418927,
cipher=6118406869103348l2
# UVM_INFO subscriber.sv(44) @ 790: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 790, Coverage = 7.55 percent
#
# UVM_INFO scoreboard.sv(19) @ 790: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 790, printing msg=7871782124328684674, key=12663582183216477661,
cipher=1626777505839564493
# UVM_INFO subscriber.sv(44) @ 800: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 800, Coverage = 7.65 percent
#
```

```
# UVM_INFO scoreboard.sv(19) @ 800: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 800, printing msg=5775103374688062447, key=5775619840937718139,
cipher=11760556453069318699
# UVM_INFO subscriber.sv(44) @ 810: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 810, Coverage = 7.75 percent
#
# UVM_INFO scoreboard.sv(19) @ 810: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 810, printing msg=16507384697058865004, key=15268300075332195832,
cipher=1548487972527265901
# UVM_INFO subscriber.sv(44) @ 820: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 820, Coverage = 7.85 percent
#
# UVM_INFO scoreboard.sv(19) @ 820: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 820, printing msg=13269642420066669710, key=11914467478380591513,
cipher=6695056286591721237
# UVM_INFO subscriber.sv(44) @ 830: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 830, Coverage = 7.95 percent
#
# UVM_INFO scoreboard.sv(19) @ 830: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 830, printing msg=11475734060551431439, key=13221294090892327514,
cipher=3162642774124757391
# UVM_INFO subscriber.sv(44) @ 840: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 840, Coverage = 8.05 percent
#
# UVM_INFO scoreboard.sv(19) @ 840: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 840, printing msg=14419256245431644103, key=153021290482923646,
cipher=1790246300974932842
# UVM_INFO subscriber.sv(44) @ 850: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 850, Coverage = 8.15 percent
#
# UVM_INFO scoreboard.sv(19) @ 850: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 850, printing msg=1788379544996768928, key=10078851231236949079,
cipher=15736209490033627492
# UVM_INFO subscriber.sv(44) @ 860: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 860, Coverage = 8.22 percent
#
# UVM_INFO scoreboard.sv(19) @ 860: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 860, printing msg=11358838515002342775, key=3429643819590490818,
cipher=41481306438888085175
# UVM_INFO subscriber.sv(44) @ 870: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 870, Coverage = 8.32 percent
#
# UVM_INFO scoreboard.sv(19) @ 870: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 870, printing msg=9573549564720810393, key=15089145154723823124,
cipher=2103622177908964929
# UVM_INFO subscriber.sv(44) @ 880: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 880, Coverage = 8.42 percent
#
# UVM_INFO scoreboard.sv(19) @ 880: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 880, printing msg=15144014897901368571, key=16280208756173197412,
cipher=822870291128313623
# UVM_INFO subscriber.sv(44) @ 890: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 890, Coverage = 8.45 percent
#
# UVM_INFO scoreboard.sv(19) @ 890: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 890, printing msg=520263483245254725, key=7227201652317309725,
cipher=2790077243691558771
# UVM_INFO subscriber.sv(44) @ 900: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 900, Coverage = 8.55 percent
#
# UVM_INFO scoreboard.sv(19) @ 900: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 900, printing msg=41535384039532071185, key=10257757664096413671,
cipher=14163343929753900453
# UVM_INFO subscriber.sv(44) @ 910: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 910, Coverage = 8.65 percent
#
```

```
# UVM_INFO scoreboard.sv(19) @ 910: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 910, printing msg=12236362822559776663, key=18282716907939742765,
cipher=1224177355830775523
# UVM_INFO subscriber.sv(44) @ 920: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 920, Coverage = 8.75 percent
#
# UVM_INFO scoreboard.sv(19) @ 920: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 920, printing msg=122564527228707901, key=15506272196495692650,
cipher=5906453394810013000
# UVM_INFO subscriber.sv(44) @ 930: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 930, Coverage = 8.85 percent
#
# UVM_INFO scoreboard.sv(19) @ 930: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 930, printing msg=40294778918063118O4, key=11705635239822894588,
cipher=12651781078258674935
# UVM_INFO subscriber.sv(44) @ 940: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 940, Coverage = 8.92 percent
#
# UVM_INFO scoreboard.sv(19) @ 940: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 940, printing msg=7797874036579260129, key=6028342272038115005,
cipher=9914996458836310290
# UVM_INFO subscriber.sv(44) @ 950: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 950, Coverage = 8.98 percent
#
# UVM_INFO scoreboard.sv(19) @ 950: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 950, printing msg=2804002637342587085, key=11010505824463980526,
cipher=10459745295066296922
# UVM_INFO subscriber.sv(44) @ 960: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 960, Coverage = 9.08 percent
#
# UVM_INFO scoreboard.sv(19) @ 960: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 960, printing msg=5765509534348810867, key=1539396178170096229,
cipher=6987157509691864455
# UVM_INFO subscriber.sv(44) @ 970: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 970, Coverage = 9.18 percent
#
# UVM_INFO scoreboard.sv(19) @ 970: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 970, printing msg=4743360775358038817, key=15331817818509317459,
cipher=5890625329325612239
# UVM_INFO subscriber.sv(44) @ 980: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 980, Coverage = 9.28 percent
#
# UVM_INFO scoreboard.sv(19) @ 980: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 980, printing msg=18077251602880583381, key=94553641614077809З5,
cipher=7882380070199162550
# UVM_INFO subscriber.sv(44) @ 990: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 990, Coverage = 9.35 percent
#
# UVM_INFO scoreboard.sv(19) @ 990: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 990, printing msg=13887728882537763003, key=863326072599545098,
cipher=4338433728109501272
# UVM_INFO subscriber.sv(44) @ 1000: uvm_test_top.env_h.enc_agent_h.enc_cov [COVSB]
@time 1000, Coverage = 9.45 percent
#
# UVM_INFO scoreboard.sv(19) @ 1000: uvm_test_top.env_h.enc_agent_h.enc_scbd [SCBD]
@time 1000, printing msg=4136430047134195291, key=6843840086110602569,
cipher=1787333810051474327
# UVM_INFO C:/questasim64_10.6c/verilog_src/uvm-
1.1d/src/base/uvm_objection.svh(1268) @ 1000: reporter [TEST_DONE] 'run' phase is
ready to proceed to the 'extract' phase
#
# --- UVM Report Summary ---
#
# ** Report counts by severity
# UVM_INFO :  201
# UVM_WARNING :    0
# UVM_ERROR :    0
# UVM_FATAL :    0
```

```
# ** Report counts by id
# [COVSB]    99
# [RNTST]     1
# [SCBD]    99
# [TEST_DONE]     1
# [UVMTOP]     1
# ** Note: $finish    : C:/questasim64_10.6c/verilog_src/uvm-
```

15.2.2 Encryption Block Coverage Report

```
# Coverage Report Summary Data by file
#
# ================================================================================
# === File: ENC_top.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                            8         8         0     100.0
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      2         2         0     100.0
#
# ================================================================================
# === File: agent.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           13        10         3      76.9
#     Branches                         8         3         5      37.5
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: driver.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           14        10         4      71.4
#     Branches                         6         2         4      33.3
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: dut.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                          559       559         0     100.0
#     Branches                       522       522         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                    130       130         0     100.0
```

```
#
# ================================================================================
# === File: environment.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                            6         4         2      66.6
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: grDesEnc.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                          558       558         0     100.0
#     Branches                       522       514         8      98.4
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: interface.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                            5         5         0     100.0
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                    386       386         0     100.0
#
# ================================================================================
# === File: monitor.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           15        11         4      73.3
#     Branches                         6         2         4      33.3
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: scoreboard.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                            8         6         2      75.0
#     Branches                         4         1         3      25.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
```

```
#         Transitions                    0         0         0     100.0
#     Toggle Bins                        0         0         0     100.0
#
# ================================================================================
# === File: sequence.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           17         7        10      41.1
#     Branches                        12         1        11       8.3
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: sequenceItem.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           43         2        41       4.6
#     Branches                        52         0        52       0.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: subscriber.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           12         9         3      75.0
#     Branches                         4         2         2      50.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: test.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                            9         7         2      77.7
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
#
# Total Coverage By File (code coverage only, filtered view): 95.5%
```

15.2.3 Decryption Block Log

```
# ----------------------------------------------------------------
# UVM-1.1d
# (C) 2007-2013 Mentor Graphics Corporation
# (C) 2007-2013 Cadence Design Systems, Inc.
```

```
# (C) 2006-2013 Synopsys, Inc.
# (C) 2011-2013 Cypress Semiconductor Corp.
# ----------------------------------------------------------------
#
#   ***********       IMPORTANT RELEASE NOTES         ************
#
#   You are using a version of the UVM library that has been compiled
#   with `UVM_NO_DEPRECATED undefined.
#   See http://www.eda.org/svdb/view.php?id=3313 for more details.
#
#   You are using a version of the UVM library that has been compiled
#   with `UVM_OBJECT_MUST_HAVE_CONSTRUCTOR undefined.
#   See http://www.eda.org/svdb/view.php?id=3770 for more details.
#
#       (Specify +UVM_NO_RELNOTES to turn off this notice)
#
# UVM_INFO @ 0: reporter [RNTST] Running test dec_test...
# UVM_INFO @ 0: reporter [UVMTOP] UVM testbench topology:
# ------------------------------------------------------------------------------
# Name                                  Type                      Size  Value
# ------------------------------------------------------------------------------
# uvm_test_top                          dec_test                  -     @449
#   env_h                               dec_env                   -     @461
#     dec_agent_h                       dec_agent                 -     @469
#       dec_cov                         dec_coverage_subscriber   -     @647
#         analysis_imp                  uvm_analysis_imp          -     @655
#         dec_item_collected_export     uvm_analysis_imp          -     @664
#       dec_drvr                        dec_driver                -     @605
#         rsp_port                      uvm_analysis_port         -     @622
#         seq_item_port                 uvm_seq_item_pull_port    -     @613
#       dec_mon                         dec_monitor               -     @631
#         Decrypt_monitor_analysis_port uvm_analysis_port         -     @675
#       dec_scbd                        dec_scoreboard            -     @639
#         dec_item_collected_export     uvm_analysis_imp          -     @684
#       dec_seqr                        uvm_sequencer             -     @482
#         rsp_export                    uvm_analysis_export       -     @490
#         seq_item_export               uvm_seq_item_pull_imp     -     @596
#         arbitration_queue             array                     0     -
#         lock_queue                    array                     0     -
#         num_last_reqs                 integral                  32    'd1
#         num_last_rsps                 integral                  32    'd1
# ------------------------------------------------------------------------------
#
# UVM_INFO dec_pkg.sv(203) @ 20: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 20, Coverage0.10 percent
#
# UVM_INFO dec_pkg.sv(136) @ 20: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 20, printing cipher=43876007906d5cb, key=150955199096f674,
decrypt=f6f360f6f692768e
# UVM_INFO dec_pkg.sv(203) @ 30: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 30, Coverage0.20 percent
#
# UVM_INFO dec_pkg.sv(136) @ 30: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 30, printing cipher=6f36bbfd74098d44, key=132980e982fa03a1,
decrypt=7e6324aaa984d13
# UVM_INFO dec_pkg.sv(203) @ 40: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 40, Coverage0.30 percent
#
# UVM_INFO dec_pkg.sv(136) @ 40: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 40, printing cipher=f8f5fb5f9ba3a674, key=dacf80ebee655f0,
decrypt=da59a5ebc2cf9301
# UVM_INFO dec_pkg.sv(203) @ 50: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 50, Coverage0.40 percent
#
# UVM_INFO dec_pkg.sv(136) @ 50: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 50, printing cipher=92ce51c44b5ae937, key=af53d5dbc04fa84c,
decrypt=2ca1098d971e1d29
```

```
# UVM_INFO dec_pkg.sv(203) @ 60: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 60, Coverage0.50 percent
#
# UVM_INFO dec_pkg.sv(136) @ 60: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 60, printing cipher=c7b9bbc506eee4c5, key=cea75320f7efba26,
decrypt=55b7a9e8318e31d3
# UVM_INFO dec_pkg.sv(203) @ 70: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 70, Coverage0.60 percent
#
# UVM_INFO dec_pkg.sv(136) @ 70: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 70, printing cipher=4a9d0725408e5199, key=900893682ea7607e,
decrypt=c33c28f31171fa6
# UVM_INFO dec_pkg.sv(203) @ 80: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 80, Coverage0.70 percent
#
# UVM_INFO dec_pkg.sv(136) @ 80: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 80, printing cipher=2b91f054c7c1a83e, key=fe6b5e3b27b57781,
decrypt=b5524fe1d0ce747f
# UVM_INFO dec_pkg.sv(203) @ 90: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 90, Coverage0.80 percent
#
# UVM_INFO dec_pkg.sv(136) @ 90: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 90, printing cipher=1e66edb57a63c53a, key=edb1aa407aefa713,
decrypt=899d11034822f691
# UVM_INFO dec_pkg.sv(203) @ 100: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 100, Coverage0.90 percent
#
# UVM_INFO dec_pkg.sv(136) @ 100: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 100, printing cipher=8dc899c5b8535f57, key=3dfb0d93f651705b,
decrypt=610b166c3688eba3
# UVM_INFO dec_pkg.sv(203) @ 110: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 110, Coverage1.00 percent
#
# UVM_INFO dec_pkg.sv(136) @ 110: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 110, printing cipher=352400338b980064, key=8ceba65fedde88d1,
decrypt=f441e853780a567
# UVM_INFO dec_pkg.sv(203) @ 120: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 120, Coverage1.10 percent
#
# UVM_INFO dec_pkg.sv(136) @ 120: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 120, printing cipher=cbf03d98a39279a8, key=22e980c8fc393e13,
decrypt=e78651010fc683e1
# UVM_INFO dec_pkg.sv(203) @ 130: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 130, Coverage1.20 percent
#
# UVM_INFO dec_pkg.sv(136) @ 130: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 130, printing cipher=bac001e76177c648, key=84ad07a21b8bd990,
decrypt=34836f56fcd5f041
# UVM_INFO dec_pkg.sv(203) @ 140: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 140, Coverage1.30 percent
#
# UVM_INFO dec_pkg.sv(136) @ 140: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 140, printing cipher=96e3930ac0a561f6, key=518d1885bd07963,
decrypt=461f49d05cb7e6fe
# UVM_INFO dec_pkg.sv(203) @ 150: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 150, Coverage1.40 percent
#
# UVM_INFO dec_pkg.sv(136) @ 150: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 150, printing cipher=2b5b6ee73af25784, key=92d7ff689d8d8bf9,
decrypt=97c0f41ed97d6164
# UVM_INFO dec_pkg.sv(203) @ 160: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 160, Coverage1.50 percent
#
# UVM_INFO dec_pkg.sv(136) @ 160: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 160, printing cipher=d40a794898cfd88b, key=7f2fb613a456346,
decrypt=22e5fffb10dccec0
# UVM_INFO dec_pkg.sv(203) @ 170: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 170, Coverage1.60 percent
```

```
#
# UVM_INFO dec_pkg.sv(136) @ 170: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 170, printing cipher=149d09c816909e0d, key=f4737d32a85018b7,
decrypt=be06781edd518493
# UVM_INFO dec_pkg.sv(203) @ 180: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 180, Coverage1.70 percent
#
# UVM_INFO dec_pkg.sv(136) @ 180: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 180, printing cipher=b1ca39bdbf4e74ea, key=1d9055a191e6395a,
decrypt=cc5f910b897e2c6c
# UVM_INFO dec_pkg.sv(203) @ 190: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 190, Coverage1.80 percent
#
# UVM_INFO dec_pkg.sv(136) @ 190: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 190, printing cipher=468b19363acf7572, key=4308e321e1075b17,
decrypt=f928a699fe6bdc68
# UVM_INFO dec_pkg.sv(203) @ 200: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 200, Coverage1.90 percent
#
# UVM_INFO dec_pkg.sv(136) @ 200: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 200, printing cipher=78118195f4ff8e63, key=4076e29eb800fd27,
decrypt=4dcce78da65a3009
# UVM_INFO dec_pkg.sv(203) @ 210: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 210, Coverage2.00 percent
#
# UVM_INFO dec_pkg.sv(136) @ 210: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 210, printing cipher=755bf14f587411b0, key=537f9e1e034b715e,
decrypt=2185945aa209c29a
# UVM_INFO dec_pkg.sv(203) @ 220: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 220, Coverage2.10 percent
#
# UVM_INFO dec_pkg.sv(136) @ 220: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 220, printing cipher=650169b44c7a1329, key=a5cc222583f0ee02,
decrypt=af8b452735f8a02f
# UVM_INFO dec_pkg.sv(203) @ 230: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 230, Coverage2.20 percent
#
# UVM_INFO dec_pkg.sv(136) @ 230: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 230, printing cipher=ed8e3db34e512630, key=a526fa195ba9bb14,
decrypt=8899f4756d66e8d6
# UVM_INFO dec_pkg.sv(203) @ 240: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 240, Coverage2.30 percent
#
# UVM_INFO dec_pkg.sv(136) @ 240: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 240, printing cipher=cdf0ce615c3ecf76, key=8c7623b15b4bdb0a,
decrypt=1728ba9b6b2d9c55
# UVM_INFO dec_pkg.sv(203) @ 250: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 250, Coverage2.40 percent
#
# UVM_INFO dec_pkg.sv(136) @ 250: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 250, printing cipher=f026ce628ce0bb41, key=3a172c0abbba5a79,
decrypt=baf94149b7b4ca9b
# UVM_INFO dec_pkg.sv(203) @ 260: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 260, Coverage2.50 percent
#
# UVM_INFO dec_pkg.sv(136) @ 260: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 260, printing cipher=ef9b4c9460bf9f78, key=d00de680fc626bf3,
decrypt=e8a6fe32cc514864
# UVM_INFO dec_pkg.sv(203) @ 270: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 270, Coverage2.56 percent
#
# UVM_INFO dec_pkg.sv(136) @ 270: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 270, printing cipher=d430ea1bdffaa1cf, key=65cbc5b6afc6899d,
decrypt=bc8122de8c967b7d
# UVM_INFO dec_pkg.sv(203) @ 280: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 280, Coverage2.66 percent
#
```

```
# UVM_INFO dec_pkg.sv(136) @ 280: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 280, printing cipher=5ea42c01b88ff9cd, key=4ace5c93b983d55d,
decrypt=69fffd3dfac999d4
# UVM_INFO dec_pkg.sv(203) @ 290: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 290, Coverage2.76 percent
#
# UVM_INFO dec_pkg.sv(136) @ 290: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 290, printing cipher=74d88df3e67f7815, key=320a1b3e3bfd5800,
decrypt=80120ada5e10ff7b
# UVM_INFO dec_pkg.sv(203) @ 300: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 300, Coverage2.86 percent
#
# UVM_INFO dec_pkg.sv(136) @ 300: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 300, printing cipher=e8bcbae7c6ef7667, key=c5d8006215b23841,
decrypt=c5270d4714c91cbd
# UVM_INFO dec_pkg.sv(203) @ 310: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 310, Coverage2.96 percent
#
# UVM_INFO dec_pkg.sv(136) @ 310: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 310, printing cipher=27be448039cc7de9, key=65e61e682b6f93b2,
decrypt=84d5ceb59f42c454
# UVM_INFO dec_pkg.sv(203) @ 320: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 320, Coverage3.06 percent
#
# UVM_INFO dec_pkg.sv(136) @ 320: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 320, printing cipher=6468ffe28c9fa160, key=29bac9c324b2130a,
decrypt=44713bceb685a37f
# UVM_INFO dec_pkg.sv(203) @ 330: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 330, Coverage3.16 percent
#
# UVM_INFO dec_pkg.sv(136) @ 330: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 330, printing cipher=7ad52d77b37d0ab5, key=7a4365a5355ee039,
decrypt=b9651565faba09bb
# UVM_INFO dec_pkg.sv(203) @ 340: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 340, Coverage3.26 percent
#
# UVM_INFO dec_pkg.sv(136) @ 340: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 340, printing cipher=8142a1f0e294ca34, key=a35ae8dbb47c65db,
decrypt=2ec6562648fd8c5a
# UVM_INFO dec_pkg.sv(203) @ 350: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 350, Coverage3.36 percent
#
# UVM_INFO dec_pkg.sv(136) @ 350: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 350, printing cipher=6f7a79201d5a73, key=6fd25de0a70fdee0,
decrypt=290c470be8fc5bbb
# UVM_INFO dec_pkg.sv(203) @ 360: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 360, Coverage3.43 percent
#
# UVM_INFO dec_pkg.sv(136) @ 360: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 360, printing cipher=45afe2218b9c9560, key=4082619d2bc775af,
decrypt=f08d2f4ee0336b1
# UVM_INFO dec_pkg.sv(203) @ 370: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 370, Coverage3.49 percent
#
# UVM_INFO dec_pkg.sv(136) @ 370: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 370, printing cipher=d412f21209aba5f7, key=bf51508e4088b9f7,
decrypt=93781251e4bf1984
# UVM_INFO dec_pkg.sv(203) @ 380: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 380, Coverage3.59 percent
#
# UVM_INFO dec_pkg.sv(136) @ 380: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 380, printing cipher=6b715caa4ec0ab8c, key=1addf6955f78b663,
decrypt=abfc7e4e5901a401
# UVM_INFO dec_pkg.sv(203) @ 390: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 390, Coverage3.69 percent
#
```

```
# UVM_INFO dec_pkg.sv(136) @ 390: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 390, printing cipher=e965e83eacf371ec, key=71688d8bc955f7a,
decrypt=640b840b6349d068
# UVM_INFO dec_pkg.sv(203) @ 400: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 400, Coverage3.79 percent
#
# UVM_INFO dec_pkg.sv(136) @ 400: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 400, printing cipher=682856f099a56969, key=7a87e8a8b7796fb5,
decrypt=ff97a9fc8c91ac55
# UVM_INFO dec_pkg.sv(203) @ 410: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 410, Coverage3.89 percent
#
# UVM_INFO dec_pkg.sv(136) @ 410: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 410, printing cipher=93dbd76f1a3131c, key=1284005cd914ed90,
decrypt=d144f2c27ed3024d
# UVM_INFO dec_pkg.sv(203) @ 420: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 420, Coverage3.99 percent
#
# UVM_INFO dec_pkg.sv(136) @ 420: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 420, printing cipher=b12dd19936b1f186, key=f03210d3d8d289c6,
decrypt=24898655d673321d
# UVM_INFO dec_pkg.sv(203) @ 430: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 430, Coverage4.09 percent
#
# UVM_INFO dec_pkg.sv(136) @ 430: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 430, printing cipher=47f63db28a94cb9b, key=a74f9174ca8e69a4,
decrypt=227b6d2a0d60095
# UVM_INFO dec_pkg.sv(203) @ 440: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 440, Coverage4.19 percent
#
# UVM_INFO dec_pkg.sv(136) @ 440: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 440, printing cipher=fb2008823c0fc888, key=4596428e7180b70b,
decrypt=2089d54e55989579
# UVM_INFO dec_pkg.sv(203) @ 450: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 450, Coverage4.29 percent
#
# UVM_INFO dec_pkg.sv(136) @ 450: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 450, printing cipher=d55d79281e6e2343, key=7b1cecd7324162b5,
decrypt=2e110deb78c479d1
# UVM_INFO dec_pkg.sv(203) @ 460: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 460, Coverage4.39 percent
#
# UVM_INFO dec_pkg.sv(136) @ 460: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 460, printing cipher=56cef7814bb9e6f4, key=d660690ecc8991e6,
decrypt=4f205ce597fe6faf
# UVM_INFO dec_pkg.sv(203) @ 470: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 470, Coverage4.49 percent
#
# UVM_INFO dec_pkg.sv(136) @ 470: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 470, printing cipher=52461080e830ca7c, key=383fa24dd42619f6,
decrypt=3b13d4db38e9f2da
# UVM_INFO dec_pkg.sv(203) @ 480: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 480, Coverage4.59 percent
#
# UVM_INFO dec_pkg.sv(136) @ 480: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 480, printing cipher=9bb766a4cf7f639b, key=f3603322c6a91f1d,
decrypt=96e662c827d2063e
# UVM_INFO dec_pkg.sv(203) @ 490: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 490, Coverage4.69 percent
#
# UVM_INFO dec_pkg.sv(136) @ 490: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 490, printing cipher=5999585bbd3e52f8, key=4c5ef07d98208e07,
decrypt=4c4dea1e9b0fcc19
# UVM_INFO dec_pkg.sv(203) @ 500: uvm_test_top.env_h.dec_agent_h.dec_cov [COVSB]
@time 500, Coverage4.79 percent
#
```

```
# UVM_INFO dec_pkg.sv(136) @ 500: uvm_test_top.env_h.dec_agent_h.dec_scbd [SCBD]
@time 500, printing cipher=c853d0c603b414b3, key=31c4892be65ef57f,
decrypt=b44c0fc97580cf0
# UVM_INFO C:/questasim64_10.6c/verilog_src/uvm-
1.1d/src/base/uvm_objection.svh(1268) @ 500: reporter [TEST_DONE] 'run' phase is
ready to proceed to the 'extract' phase
#
# --- UVM Report Summary ---
#
# ** Report counts by severity
# UVM_INFO :  101
# UVM_WARNING :    0
# UVM_ERROR :    0
# UVM_FATAL :    0
# ** Report counts by id
# [COVSB]    49
# [RNTST]     1
# [SCBD]    49
# [TEST_DONE]     1
# [UVMTOP]     1
# ** Note: $finish    : C:/questasim64_10.6c/verilog_src/uvm-
1.1d/src/base/uvm_root.svh(430)
#    Time: 500 ns  Iteration: 62  Instance: /dec_top
```

15.2.4 Decryption Block Coverage Report

```
# Coverage Report Summary Data by file
#
# ================================================================================
# === File: dec_pkg.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                          136        65        71      47.7
#     Branches                        92        11        81      11.9
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: dutdec.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                          559       559         0     100.0
#     Branches                       522       522         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                    130       130         0     100.0
#
# ================================================================================
# === File: grDesDec.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                          558       558         0     100.0
#     Branches                       522       514         8      98.4
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
```

```
#         Transitions                    0         0         0     100.0
#     Toggle Bins                        0         0         0     100.0
#
# ================================================================================
# === File: interface.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                            5         5         0     100.0
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                    514       386       128      75.0
#
# ================================================================================
# === File: top.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                            8         8         0     100.0
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      2         2         0     100.0
#
#
# TOTAL COVERGROUP COVERAGE: 99.7%  COVERGROUP TYPES: 1
#
# TOTAL ASSERTION COVERAGE: 100.0%  ASSERTIONS: 2
#
# Total Coverage By File (code coverage only, filtered view): 88.9%
```

15.2.5 Memory Block Log

```
# ----------------------------------------------------------------
# UVM-1.1d
# (C) 2007-2013 Mentor Graphics Corporation
# (C) 2007-2013 Cadence Design Systems, Inc.
# (C) 2006-2013 Synopsys, Inc.
# (C) 2011-2013 Cypress Semiconductor Corp.
# ----------------------------------------------------------------
#
#   ***********       IMPORTANT RELEASE NOTES         ************
#
#   You are using a version of the UVM library that has been compiled
#   with `UVM_NO_DEPRECATED undefined.
#   See http://www.eda.org/svdb/view.php?id=3313 for more details.
#
#   You are using a version of the UVM library that has been compiled
#   with `UVM_OBJECT_MUST_HAVE_CONSTRUCTOR undefined.
#   See http://www.eda.org/svdb/view.php?id=3770 for more details.
#
#       (Specify +UVM_NO_RELNOTES to turn off this notice)
#
# UVM_INFO @ 0: reporter [RNTST] Running test dram_test...
# UVM_INFO SB.sv(29) @ 0: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON1
# sb data_in=                    0,add= 0
# UVM_INFO SB.sv(32) @ 0: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON2
# sb data_out=                   0,add= 0
# ------------------------------------------------------------------------------
----
# Name                          Type           Size  Value
```

```
# ------------------------------------------------------------------------------
----
# pkt                            dram_seq_item  -     @849
#   begin_time                   time           64    0
#   depth                        int            32    'd2
#   parent sequence (name)       string         3     seq
#   parent sequence (full name)  string         33
uvm_test_top.env.agent1.seqr1.seq
#   sequencer                    string         29    uvm_test_top.env.agent1.seqr1
# ------------------------------------------------------------------------------
----
# UVM_INFO MON1.sv(33) @ 5: uvm_test_top.env.agent1.mon1 [MON] MON TRANSACTIONS
# UVM_INFO MON2.sv(35) @ 5: uvm_test_top.env.agent2.mon2 [MON] MON TRANSACTIONS
# UVM_INFO DRV.sv(27) @ 10: uvm_test_top.env.agent1.drv [DRV TRANSACTIONS]
inf.data0_in= 1594145668561125899,inf.add0= 2, inf.wr0=0
# UVM_INFO COV.sv(34) @ 15: uvm_test_top.env.cov [SEQ] SEQUENCE TRANSACTIONS
# UVM_INFO SB.sv(42) @ 15: uvm_test_top.env.sb [SB MATCHED] DATA pkt.data0_in=
0,pkt1.data1_out=                   0
# UVM_INFO SB.sv(29) @ 15: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON1
# sb data_in=                    0,add= 0
# UVM_INFO SB.sv(32) @ 15: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON2
# sb data_out=                   0,add= 0
# UVM_INFO DRV.sv(39) @ 20: uvm_test_top.env.agent1.drv [DRV] DRV TRANSACTION TO
DUT
# UVM_INFO MON1.sv(31) @ 25: uvm_test_top.env.agent1.mon1 [MON1] MON1 TRANSACTIONS
# UVM_INFO MON1.sv(33) @ 25: uvm_test_top.env.agent1.mon1 [MON] MON TRANSACTIONS
# UVM_INFO MON2.sv(35) @ 25: uvm_test_top.env.agent2.mon2 [MON] MON TRANSACTIONS
# ------------------------------------------------------------------------------
----
# Name                           Type           Size  Value
# ------------------------------------------------------------------------------
----
# pkt                            dram_seq_item  -     @849
#   begin_time                   time           64    25
#   end_time                     time           64    20
#   depth                        int            32    'd2
#   parent sequence (name)       string         3     seq
#   parent sequence (full name)  string         33
uvm_test_top.env.agent1.seqr1.seq
#   sequencer                    string         29    uvm_test_top.env.agent1.seqr1
# ------------------------------------------------------------------------------
----
# UVM_INFO DRV.sv(32) @ 30: uvm_test_top.env.agent1.drv [DRV TRANSACTIONS]
inf.add1= 2, inf.wr1=1
# UVM_INFO COV.sv(34) @ 35: uvm_test_top.env.cov [SEQ] SEQUENCE TRANSACTIONS
# UVM_INFO SB.sv(42) @ 35: uvm_test_top.env.sb [SB MATCHED] DATA pkt.data0_in=
0,pkt1.data1_out=                   0
# UVM_INFO SB.sv(29) @ 35: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON1
# sb data_in= 1594145668561125899,add= 2
# UVM_INFO SB.sv(32) @ 35: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON2
# sb data_out=                   0,add= 0
# UVM_INFO DRV.sv(39) @ 40: uvm_test_top.env.agent1.drv [DRV] DRV TRANSACTION TO
DUT
# UVM_INFO SEQ.sv(27) @ 40: uvm_test_top.env.agent1.seqr1@@seq [SEQ] SEQUENCE
TRANSACTIONS
# UVM_INFO MON1.sv(31) @ 45: uvm_test_top.env.agent1.mon1 [MON1] MON1 TRANSACTIONS
# UVM_INFO MON1.sv(33) @ 45: uvm_test_top.env.agent1.mon1 [MON] MON TRANSACTIONS
# UVM_INFO MON2.sv(32) @ 45: uvm_test_top.env.agent2.mon2 [MON2] MON2 TRANSACTIONS
# UVM_INFO MON2.sv(35) @ 45: uvm_test_top.env.agent2.mon2 [MON] MON TRANSACTIONS
# ------------------------------------------------------------------------------
----
# Name                           Type           Size  Value
# ------------------------------------------------------------------------------
----
# pkt                            dram_seq_item  -     @849
#   begin_time                   time           64    45
#   end_time                     time           64    40
#   depth                        int            32    'd2
```

```
#   parent sequence (name)       string         3     seq
#   parent sequence (full name)  string         33
uvm_test_top.env.agent1.seqr1.seq
#   sequencer                    string         29    uvm_test_top.env.agent1.seqr1
# ---------------------------------------------------------------------------
----
# UVM_INFO DRV.sv(27) @ 50: uvm_test_top.env.agent1.drv [DRV TRANSACTIONS]
inf.data0_in=14649154148057910764,inf.add0=41, inf.wr0=0
# UVM_INFO COV.sv(34) @ 55: uvm_test_top.env.cov [SEQ] SEQUENCE TRANSACTIONS
# UVM_INFO SB.sv(42) @ 55: uvm_test_top.env.sb [SB MATCHED] DATA pkt.data0_in=
1594145668561125899,pkt1.data1_out= 1594145668561125899
# UVM_INFO SB.sv(29) @ 55: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON1
# sb data_in= 1594145668561125899,add= 2
# UVM_INFO SB.sv(32) @ 55: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON2
# sb data_out= 1594145668561125899,add= 2
# UVM_INFO DRV.sv(39) @ 60: uvm_test_top.env.agent1.drv [DRV] DRV TRANSACTION TO
DUT
# UVM_INFO MON1.sv(31) @ 65: uvm_test_top.env.agent1.mon1 [MON1] MON1 TRANSACTIONS
# UVM_INFO MON1.sv(33) @ 65: uvm_test_top.env.agent1.mon1 [MON] MON TRANSACTIONS
# UVM_INFO MON2.sv(32) @ 65: uvm_test_top.env.agent2.mon2 [MON2] MON2 TRANSACTIONS
# UVM_INFO MON2.sv(35) @ 65: uvm_test_top.env.agent2.mon2 [MON] MON TRANSACTIONS
# ---------------------------------------------------------------------------
----
# Name                           Type           Size  Value
# ---------------------------------------------------------------------------
----
# pkt                            dram_seq_item  -     @849
#   begin_time                   time           64    65
#   end_time                     time           64    60
#   depth                        int            32    'd2
#   parent sequence (name)       string         3     seq
#   parent sequence (full name)  string         33
uvm_test_top.env.agent1.seqr1.seq
#   sequencer                    string         29    uvm_test_top.env.agent1.seqr1
# ---------------------------------------------------------------------------
----
# UVM_INFO DRV.sv(32) @ 70: uvm_test_top.env.agent1.drv [DRV TRANSACTIONS]
inf.add1=41, inf.wr1=1
# UVM_INFO COV.sv(34) @ 75: uvm_test_top.env.cov [SEQ] SEQUENCE TRANSACTIONS
# UVM_INFO SB.sv(42) @ 75: uvm_test_top.env.sb [SB MATCHED] DATA pkt.data0_in=
1594145668561125899,pkt1.data1_out= 1594145668561125899
# UVM_INFO SB.sv(29) @ 75: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON1
# sb data_in=14649154148057910764,add=41
# UVM_INFO SB.sv(32) @ 75: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON2
# sb data_out= 1594145668561125899,add= 2
# UVM_INFO DRV.sv(39) @ 80: uvm_test_top.env.agent1.drv [DRV] DRV TRANSACTION TO
DUT
# UVM_INFO SEQ.sv(27) @ 80: uvm_test_top.env.agent1.seqr1@@seq [SEQ] SEQUENCE
TRANSACTIONS
# UVM_INFO MON1.sv(31) @ 85: uvm_test_top.env.agent1.mon1 [MON1] MON1 TRANSACTIONS
# UVM_INFO MON1.sv(33) @ 85: uvm_test_top.env.agent1.mon1 [MON] MON TRANSACTIONS
# UVM_INFO MON2.sv(32) @ 85: uvm_test_top.env.agent2.mon2 [MON2] MON2 TRANSACTIONS
# UVM_INFO MON2.sv(35) @ 85: uvm_test_top.env.agent2.mon2 [MON] MON TRANSACTIONS
# ---------------------------------------------------------------------------
----
# Name                           Type           Size  Value
# ---------------------------------------------------------------------------
----
# pkt                            dram_seq_item  -     @849
#   begin_time                   time           64    85
#   end_time                     time           64    80
#   depth                        int            32    'd2
#   parent sequence (name)       string         3     seq
#   parent sequence (full name)  string         33
uvm_test_top.env.agent1.seqr1.seq
#   sequencer                    string         29    uvm_test_top.env.agent1.seqr1
# ---------------------------------------------------------------------------
----
```

```
# UVM_INFO DRV.sv(27) @ 90: uvm_test_top.env.agent1.drv [DRV TRANSACTIONS]
inf.data0_in= 1219570577036066711,inf.add0=60, inf.wr0=0
# UVM_INFO COV.sv(34) @ 95: uvm_test_top.env.cov [SEQ] SEQUENCE TRANSACTIONS
# UVM_INFO SB.sv(42) @ 95: uvm_test_top.env.sb [SB MATCHED] DATA
pkt.data0_in=14649154148057910764,pkt1.data1_out=14649154148057910764
# UVM_INFO SB.sv(29) @ 95: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON1
# sb data_in=14649154148057910764,add=41
# UVM_INFO SB.sv(32) @ 95: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON2
# sb data_out=14649154148057910764,add=41
# UVM_INFO DRV.sv(39) @ 100: uvm_test_top.env.agent1.drv [DRV] DRV TRANSACTION TO
DUT
# UVM_INFO MON1.sv(31) @ 105: uvm_test_top.env.agent1.mon1 [MON1] MON1 TRANSACTIONS
# UVM_INFO MON1.sv(33) @ 105: uvm_test_top.env.agent1.mon1 [MON] MON TRANSACTIONS
# UVM_INFO MON2.sv(32) @ 105: uvm_test_top.env.agent2.mon2 [MON2] MON2 TRANSACTIONS
# UVM_INFO MON2.sv(35) @ 105: uvm_test_top.env.agent2.mon2 [MON] MON TRANSACTIONS
# ------------------------------------------------------------------------------
----
# Name                            Type           Size  Value
# ------------------------------------------------------------------------------
----
# pkt                             dram_seq_item  -     @849
#   begin_time                    time           64    105
#   end_time                      time           64    100
#   depth                         int            32    'd2
#   parent sequence (name)        string         3     seq
#   parent sequence (full name)   string         33
uvm_test_top.env.agent1.seqr1.seq
#   sequencer                     string         29    uvm_test_top.env.agent1.seqr1
# ------------------------------------------------------------------------------
----
# UVM_INFO DRV.sv(32) @ 110: uvm_test_top.env.agent1.drv [DRV TRANSACTIONS]
inf.add1=60, inf.wr1=1
# UVM_INFO COV.sv(34) @ 115: uvm_test_top.env.cov [SEQ] SEQUENCE TRANSACTIONS
# UVM_INFO SB.sv(42) @ 115: uvm_test_top.env.sb [SB MATCHED] DATA
pkt.data0_in=14649154148057910764,pkt1.data1_out=14649154148057910764
# UVM_INFO SB.sv(29) @ 115: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON1
# sb data_in= 1219570577036066711,add=60
# UVM_INFO SB.sv(32) @ 115: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON2
# sb data_out=14649154148057910764,add=41
# UVM_INFO DRV.sv(39) @ 120: uvm_test_top.env.agent1.drv [DRV] DRV TRANSACTION TO
DUT
# UVM_INFO SEQ.sv(27) @ 120: uvm_test_top.env.agent1.seqr1@@seq [SEQ] SEQUENCE
TRANSACTIONS
# UVM_INFO MON1.sv(31) @ 125: uvm_test_top.env.agent1.mon1 [MON1] MON1 TRANSACTIONS
# UVM_INFO MON1.sv(33) @ 125: uvm_test_top.env.agent1.mon1 [MON] MON TRANSACTIONS
# UVM_INFO MON2.sv(32) @ 125: uvm_test_top.env.agent2.mon2 [MON2] MON2 TRANSACTIONS
# UVM_INFO MON2.sv(35) @ 125: uvm_test_top.env.agent2.mon2 [MON] MON TRANSACTIONS
# ------------------------------------------------------------------------------
----
# Name                            Type           Size  Value
# ------------------------------------------------------------------------------
----
# pkt                             dram_seq_item  -     @849
#   begin_time                    time           64    125
#   end_time                      time           64    120
#   depth                         int            32    'd2
#   parent sequence (name)        string         3     seq
#   parent sequence (full name)   string         33
uvm_test_top.env.agent1.seqr1.seq
#   sequencer                     string         29    uvm_test_top.env.agent1.seqr1
# ------------------------------------------------------------------------------
----
# UVM_INFO DRV.sv(27) @ 130: uvm_test_top.env.agent1.drv [DRV TRANSACTIONS]
inf.data0_in= 5825563254913227272,inf.add0=56, inf.wr0=0
# UVM_INFO COV.sv(34) @ 135: uvm_test_top.env.cov [SEQ] SEQUENCE TRANSACTIONS
# UVM_INFO SB.sv(42) @ 135: uvm_test_top.env.sb [SB MATCHED] DATA pkt.data0_in=
1219570577036066711,pkt1.data1_out= 1219570577036066711
# UVM_INFO SB.sv(29) @ 135: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON1
```

```
# sb data_in= 1219570577036066711,add=60
# UVM_INFO SB.sv(32) @ 135: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON2
# sb data_out= 1219570577036066711,add=60
# UVM_INFO DRV.sv(39) @ 140: uvm_test_top.env.agent1.drv [DRV] DRV TRANSACTION TO
DUT
# UVM_INFO MON1.sv(31) @ 145: uvm_test_top.env.agent1.mon1 [MON1] MON1 TRANSACTIONS
# UVM_INFO MON1.sv(33) @ 145: uvm_test_top.env.agent1.mon1 [MON] MON TRANSACTIONS
# UVM_INFO MON2.sv(32) @ 145: uvm_test_top.env.agent2.mon2 [MON2] MON2 TRANSACTIONS
# UVM_INFO MON2.sv(35) @ 145: uvm_test_top.env.agent2.mon2 [MON] MON TRANSACTIONS
# ------------------------------------------------------------------------------
----
# Name                            Type           Size  Value
# ------------------------------------------------------------------------------
----
# pkt                             dram_seq_item  -     @849
#   begin_time                    time           64    145
#   end_time                      time           64    140
#   depth                         int            32    'd2
#   parent sequence (name)        string         3     seq
#   parent sequence (full name)   string         33
uvm_test_top.env.agent1.seqr1.seq
#   sequencer                     string         29    uvm_test_top.env.agent1.seqr1
# ------------------------------------------------------------------------------
----
# UVM_INFO DRV.sv(32) @ 150: uvm_test_top.env.agent1.drv [DRV TRANSACTIONS]
inf.add1=56, inf.wr1=1
# UVM_INFO COV.sv(34) @ 155: uvm_test_top.env.cov [SEQ] SEQUENCE TRANSACTIONS
# UVM_INFO SB.sv(42) @ 155: uvm_test_top.env.sb [SB MATCHED] DATA pkt.data0_in=
1219570577036066711,pkt1.data1_out= 1219570577036066711
# UVM_INFO SB.sv(29) @ 155: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON1
# sb data_in= 5825563254913227272,add=56
# UVM_INFO SB.sv(32) @ 155: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON2
# sb data_out= 1219570577036066711,add=60
# UVM_INFO DRV.sv(39) @ 160: uvm_test_top.env.agent1.drv [DRV] DRV TRANSACTION TO
DUT
# UVM_INFO SEQ.sv(27) @ 160: uvm_test_top.env.agent1.seqr1@@seq [SEQ] SEQUENCE
TRANSACTIONS
# UVM_INFO MON1.sv(31) @ 165: uvm_test_top.env.agent1.mon1 [MON1] MON1 TRANSACTIONS
# UVM_INFO MON1.sv(33) @ 165: uvm_test_top.env.agent1.mon1 [MON] MON TRANSACTIONS
# UVM_INFO MON2.sv(32) @ 165: uvm_test_top.env.agent2.mon2 [MON2] MON2 TRANSACTIONS
# UVM_INFO MON2.sv(35) @ 165: uvm_test_top.env.agent2.mon2 [MON] MON TRANSACTIONS
# ------------------------------------------------------------------------------
----
# Name                            Type           Size  Value
# ------------------------------------------------------------------------------
----
# pkt                             dram_seq_item  -     @849
#   begin_time                    time           64    165
#   end_time                      time           64    160
#   depth                         int            32    'd2
#   parent sequence (name)        string         3     seq
#   parent sequence (full name)   string         33
uvm_test_top.env.agent1.seqr1.seq
#   sequencer                     string         29    uvm_test_top.env.agent1.seqr1
# ------------------------------------------------------------------------------
----
# UVM_INFO DRV.sv(27) @ 170: uvm_test_top.env.agent1.drv [DRV TRANSACTIONS]
inf.data0_in=10575572213112369973,inf.add0=45, inf.wr0=0
# UVM_INFO COV.sv(34) @ 175: uvm_test_top.env.cov [SEQ] SEQUENCE TRANSACTIONS
# UVM_INFO SB.sv(42) @ 175: uvm_test_top.env.sb [SB MATCHED] DATA pkt.data0_in=
5825563254913227272,pkt1.data1_out= 5825563254913227272
# UVM_INFO SB.sv(29) @ 175: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON1
# sb data_in= 5825563254913227272,add=56
# UVM_INFO SB.sv(32) @ 175: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON2
# sb data_out= 5825563254913227272,add=56
# UVM_INFO DRV.sv(39) @ 180: uvm_test_top.env.agent1.drv [DRV] DRV TRANSACTION TO
DUT
# UVM_INFO MON1.sv(31) @ 185: uvm_test_top.env.agent1.mon1 [MON1] MON1 TRANSACTIONS
```

```
# UVM_INFO MON1.sv(33) @ 185: uvm_test_top.env.agent1.mon1 [MON] MON TRANSACTIONS
# UVM_INFO MON2.sv(32) @ 185: uvm_test_top.env.agent2.mon2 [MON2] MON2 TRANSACTIONS
# UVM_INFO MON2.sv(35) @ 185: uvm_test_top.env.agent2.mon2 [MON] MON TRANSACTIONS
# ------------------------------------------------------------------------------
----
# Name                            Type           Size  Value
# ------------------------------------------------------------------------------
----
# pkt                             dram_seq_item  -     @849
#   begin_time                    time           64    385
#   end_time                      time           64    380
#   depth                         int            32    'd2
#   parent sequence (name)        string         3     seq
#   parent sequence (full name)   string         33
uvm_test_top.env.agent1.seqr1.seq
#   sequencer                     string         29    uvm_test_top.env.agent1.seqr1
# ------------------------------------------------------------------------------
----
# UVM_INFO DRV.sv(32) @ 390: uvm_test_top.env.agent1.drv [DRV TRANSACTIONS]
inf.add1=50, inf.wr1=1
# UVM_INFO COV.sv(34) @ 395: uvm_test_top.env.cov [SEQ] SEQUENCE TRANSACTIONS
# UVM_INFO SB.sv(42) @ 395: uvm_test_top.env.sb [SB MATCHED] DATA pkt.data0_in=
1711158093729812244,pkt1.data1_out= 1711158093729812244
# UVM_INFO SB.sv(29) @ 395: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON1
# sb data_in= 6438137669251362200,add=50
# UVM_INFO SB.sv(32) @ 395: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON2
# sb data_out= 1711158093729812244,add=62
# UVM_INFO DRV.sv(39) @ 400: uvm_test_top.env.agent1.drv [DRV] DRV TRANSACTION TO
DUT
# UVM_INFO SEQ.sv(27) @ 400: uvm_test_top.env.agent1.seqr1@@seq [SEQ] SEQUENCE
TRANSACTIONS
# UVM_INFO MON1.sv(31) @ 405: uvm_test_top.env.agent1.mon1 [MON1] MON1 TRANSACTIONS
# UVM_INFO MON1.sv(33) @ 405: uvm_test_top.env.agent1.mon1 [MON] MON TRANSACTIONS
# UVM_INFO MON2.sv(32) @ 405: uvm_test_top.env.agent2.mon2 [MON2] MON2 TRANSACTIONS
# UVM_INFO MON2.sv(35) @ 405: uvm_test_top.env.agent2.mon2 [MON] MON TRANSACTIONS
# UVM_INFO COV.sv(34) @ 415: uvm_test_top.env.cov [SEQ] SEQUENCE TRANSACTIONS
# UVM_INFO SB.sv(42) @ 415: uvm_test_top.env.sb [SB MATCHED] DATA pkt.data0_in=
6438137669251362200,pkt1.data1_out= 6438137669251362200
# UVM_INFO SB.sv(29) @ 415: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON1
# sb data_in= 6438137669251362200,add=50
# UVM_INFO SB.sv(32) @ 415: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON2
# sb data_out= 6438137669251362200,add=50
# UVM_INFO MON1.sv(31) @ 425: uvm_test_top.env.agent1.mon1 [MON1] MON1 TRANSACTIONS
# UVM_INFO MON1.sv(33) @ 425: uvm_test_top.env.agent1.mon1 [MON] MON TRANSACTIONS
# UVM_INFO MON2.sv(32) @ 425: uvm_test_top.env.agent2.mon2 [MON2] MON2 TRANSACTIONS
# UVM_INFO MON2.sv(35) @ 425: uvm_test_top.env.agent2.mon2 [MON] MON TRANSACTIONS
# UVM_INFO COV.sv(34) @ 435: uvm_test_top.env.cov [SEQ] SEQUENCE TRANSACTIONS
# UVM_INFO SB.sv(42) @ 435: uvm_test_top.env.sb [SB MATCHED] DATA pkt.data0_in=
6438137669251362200,pkt1.data1_out= 6438137669251362200
# UVM_INFO SB.sv(29) @ 435: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON1
# sb data_in= 6438137669251362200,add=50
# UVM_INFO SB.sv(32) @ 435: uvm_test_top.env.sb [SB] TRANSACTIONS FROM MON2
# sb data_out= 6438137669251362200,add=50
# UVM_INFO MON1.sv(31) @ 445: uvm_test_top.env.agent1.mon1 [MON1] MON1 TRANSACTIONS
# UVM_INFO MON1.sv(33) @ 445: uvm_test_top.env.agent1.mon1 [MON] MON TRANSACTIONS
# UVM_INFO MON2.sv(32) @ 445: uvm_test_top.env.agent2.mon2 [MON2] MON2 TRANSACTIONS
# UVM_INFO MON2.sv(35) @ 445: uvm_test_top.env.agent2.mon2 [MON] MON TRANSACTIONS
# UVM_INFO C:/questasim64_10.6c/verilog_src/uvm-
1.1d/src/base/uvm_objection.svh(1268) @ 450: reporter [TEST_DONE] 'run' phase is
ready to proceed to the 'extract' phase
#
# --- UVM Report Summary ---
#
# ** Report counts by severity
# UVM_INFO :  231
# UVM_WARNING :    0
# UVM_ERROR :    0
# UVM_FATAL :    0
```

```
# ** Report counts by id
# [DRV]    20
# [DRV TRANSACTIONS]    20
# [MON]    46
# [MON1]    22
# [MON2]    21
# [RNTST]     1
# [SB]    46
# [SB MATCHED]    22
# [SEQ]    32
# [TEST_DONE]     1
# ** Note: $finish    : C:/questasim64_10.6c/verilog_src/uvm-
1.1d/src/base/uvm_root.svh(430)
#    Time: 450 ns  Iteration: 54  Instance: /dram_top
```

15.2.6 Memory Block Coverage Report

```
# Coverage Report Summary Data by file
#
# ================================================================================
# === File: AGENT1.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           10         7         3      70.0
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: AGENT2.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                            6         3         3      50.0
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: COV.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                            9         6         3      66.6
#     Branches                         2         1         1      50.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: DRV.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           23        20         3      86.9
```

```
#     Branches                          8         5         3      62.5
#     FEC Condition Terms               0         0         0     100.0
#     FEC Expression Terms              0         0         0     100.0
#     FSMs                                                      100.0
#         States                        0         0         0     100.0
#         Transitions                   0         0         0     100.0
#     Toggle Bins                       0         0         0     100.0
#
# ================================================================================
# === File: DUT.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           10         5         5      50.0
#     Branches                         6         3         3      50.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                      100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: ENV.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           13        10         3      76.9
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                      100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: INTERFACE.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                            0         0         0     100.0
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                      100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                    544       282       262      51.8
#
# ================================================================================
# === File: MON1.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           21        18         3      85.7
#     Branches                         6         4         2      66.6
#     FEC Condition Terms              2         0         2       0.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                      100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: MON2.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
```

```
#     ----------------            ------      ----    ------ ---------
#     Stmts                           17        14         3      82.3
#     Branches                         6         4         2      66.6
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: SB.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           19        15         4      78.9
#     Branches                        12         5         7      41.6
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: SEQ.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           22        13         9      59.0
#     Branches                        12         1        11       8.3
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: SEQR.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                            4         1         3      25.0
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: SEQ_ITEM.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           11         3         8      27.2
#     Branches                        10         2         8      20.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: TEST.sv
```

```
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                           11         9         2      81.8
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      0         0         0     100.0
#
# ================================================================================
# === File: TOP.sv
# ================================================================================
#     Enabled Coverage            Active      Hits    Misses % Covered
#     ----------------            ------      ----    ------ ---------
#     Stmts                            6         6         0     100.0
#     Branches                         0         0         0     100.0
#     FEC Condition Terms              0         0         0     100.0
#     FEC Expression Terms             0         0         0     100.0
#     FSMs                                                     100.0
#         States                       0         0         0     100.0
#         Transitions                  0         0         0     100.0
#     Toggle Bins                      2         2         0     100.0
#
#
# TOTAL COVERGROUP COVERAGE: 100.0%  COVERGROUP TYPES: 1
#
# TOTAL ASSERTION COVERAGE: 100.0%  ASSERTIONS: 1
#
# Total Coverage By File (code coverage only, filtered view): 40.9%
```