Physical Design (PD)

Day 29
Design for Testability (DFT-2)

Delivered by

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Session Topics

- Controllability
- Sequential testing
- Ad-Hoc DFT
- Scan DFT
- DFT DRC rules

Objective of DFT

- The main objective of Design for testability where in extra circuitry is inserted is to achieve the two goals of
- Controllability
  - The ability to establish a specific signal value at each node in a circuit by setting values on the circuit's inputs
- Observability
  - The ability to determine the signal value at any node in a circuit by controlling the circuit's inputs and observing its outputs

Design for Testability

- DFT is defined as changing a given circuit to decrease the overall difficulty of testing
  - Changing refers to addition of new logic or modification of existing circuit
- As a result the new circuit will have two modes of operation
  - Test mode in which circuit is configured only for testing purpose
  - Normal Mode in which circuit behaviour is same as that of original design
- DFT though may not always be used as it introduces overhead such as timing, power, area, package cost, design time, yield, manufacturing cost

Need for DFT

- Key objective is to reduce the difficulty of testing
- Difficulty arises from the fact that state inputs and state outputs can not be directly controlled and observed
- Modification of circuit leads to creation of certain modes where controlling and observing the internal flip-flops is possible
  - Leads to reduction of test development cost
- DFT not only reduces Test Development and Application cost but makes high test quality achievable

Relevance of DFT

- Consider a typical board manufacturing scenario where pre-tested chips are assembled onto a printed circuit board
  - One possible way to test the interconnects is via application of test at primary inputs and observation of responses at outputs of the board
  - In this method CUT is the aggregate of the circuitry in each chip on the board and all inter chip interconnections
  - In such scenario
    - Test development is expensive
    - Test development is impossible due to unavailability of details of the circuit within each chip

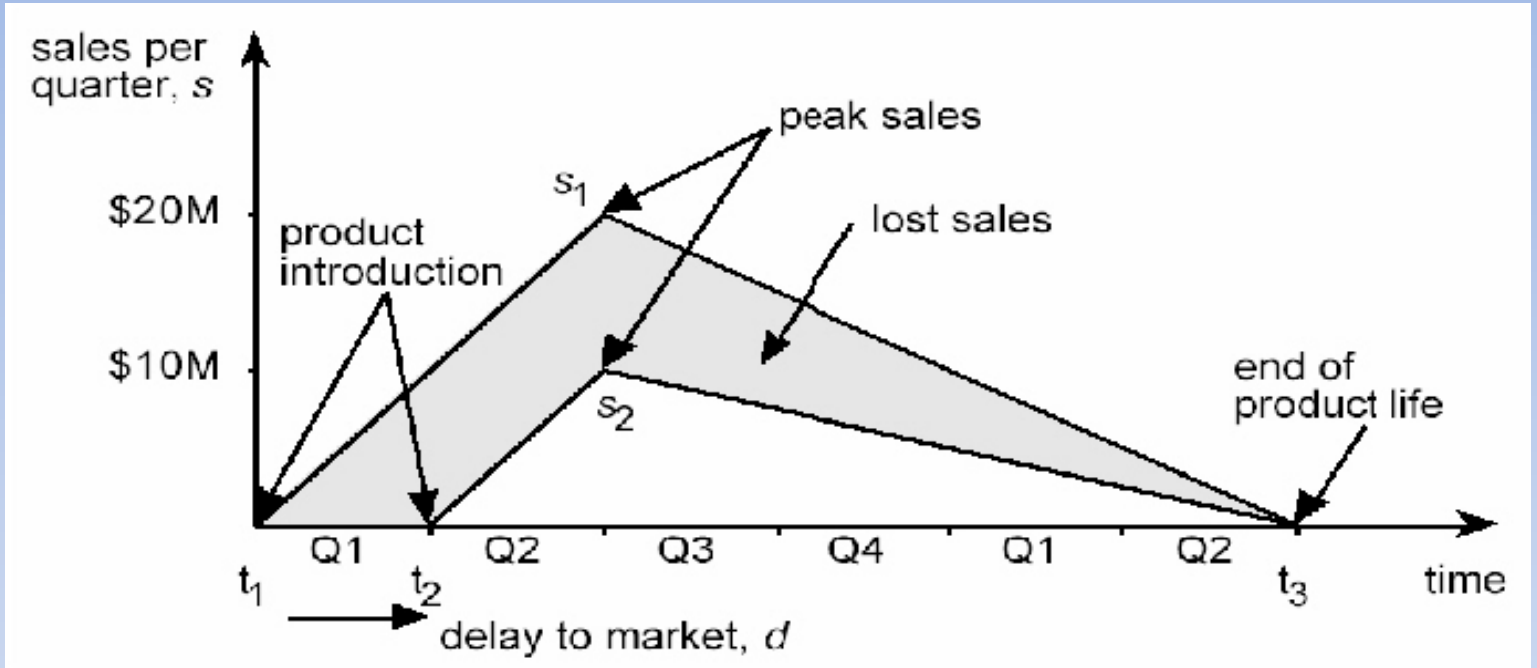
Relevance of DFT

- Alternative is to use physical probes to connect chip I/O *pins* to check for interconnect
  - First difficulty is that a value must be applied to a pin via probe
  - Second, cost of such physical probing can be very high
  - Finally in BGA packaging technology many of the pins are located across bottom surface of the chip and can't be probed
- Best alternative is DFT
  - Reduces test cost
  - Reduces test pattern generation effort
  - Improves test quality
  - Achieve higher fault coverage
  - Reduces chip re-spins

DFT Techniques

- Many DFT techniques available such as
- Ad-Hoc DFT
  - DFT technique for a particular design
  - Not applicable to all designs
  - Relies on ‘good’ design practice learned from experience
  - Testability Measures can be used to identify circuit areas that are difficult to test
  - Once identified circuit is modified or test points are inserted

Ad-Hoc DFT



- Shortcomings
  - This type of strategy is difficult to use in large circuits
  - Testability measures are **approximations** and don't always work
  - Good fault coverage is not **guaranteed** from ATPG even after circuit modifications and test point insertion is performed

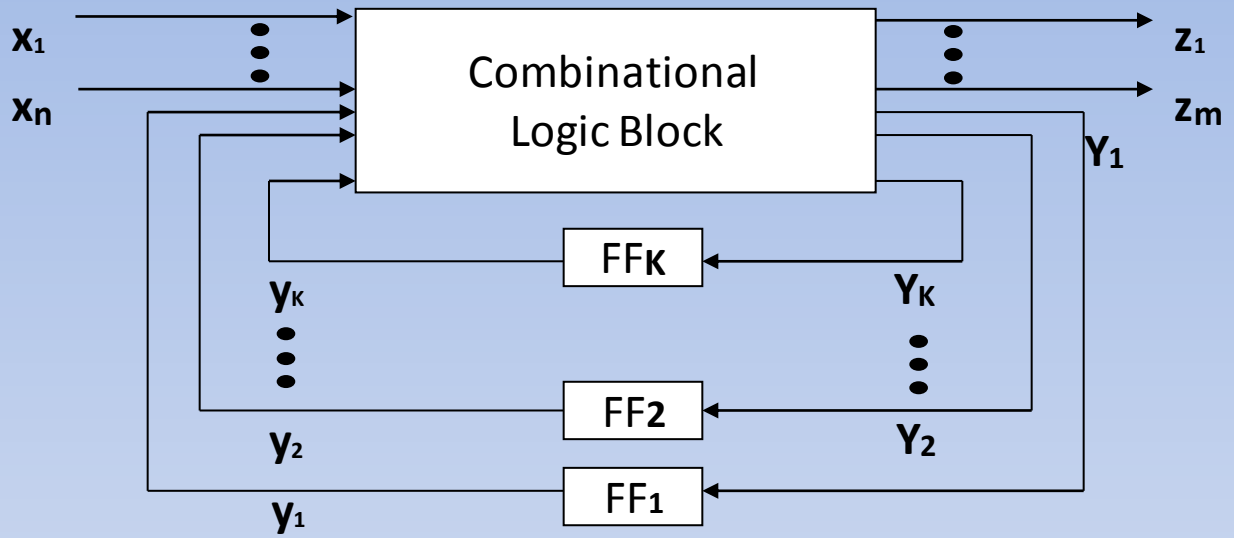
Guidelines for DFT

- For Ad-Hoc DFT to be successful the basic requirements of a circuit are
- Avoid use of redundant logic
- Minimize asynchronous logic
- Isolate clock from the logic
- Partition large circuits to smaller sub-blocks
- Circuit should be easily initializable
- Separate analog and digital circuits physically
- Ensure that internal oscillators, PLL, memory can be disabled during testing

Structured DFT

- Structured DFT involves adding extra logic and signals dedicated for test according to some procedure
- Most common Structured DFT techniques are
  - Scan based DFT
    - Mux based Scan
      - Full
      - Partial
    - LSSD Based Scan
  - Built in Self Test
    - Logic BIST
    - Memory BIST

Sequential Circuit



- Sequential circuit comprises of a block of combinational circuit and a set of ‘k’ flip-flops.
- Primary inputs of the sequential circuit are x1,x2,……xn

Sequential Circuit

- Primary outputs of the sequential circuit are z1,z2,……zm
- Present state variables y1,y2,……yk form the state inputs of the combinational circuits
- Next state variables Y1,Y2,……Yk form the state outputs of the combinational circuits

Scan Based DFT

- Test development for sequential circuit is difficult due to the inability to control and observe the state inputs and outputs.
- For many sequential circuits cost of test development is so high that fault coverage attained is low
- Scan DFT Methodology helps in
  - Reducing test development cost
  - Enabling high fault coverage

Scan Methodology

- In this Methodology flip-flops are designed and connected in a manner that enables two modes of operation
  - Normal Mode
  - Test Mode
- In test mode, flip-flops are configured as one or more shift registers called Scan Registers or Scan Chain
- In normal mode, response at the state outputs is captured in the flip-flops

Scan Methodology

- The obtained values are observed by switching the circuit back to test mode and observing the output of the last flip-flop in each chain
- For the purpose of Test development, the state inputs and state outputs can be treated as similar to primary inputs and primary outputs

Scan Methodology

- The combinational logic block with inputs x1, x2, ….. xn **and** y1,y2,……yk and outputs z1,z2,……zm **and** Y1,Y2,……Yk need to be considered for the purpose of test development

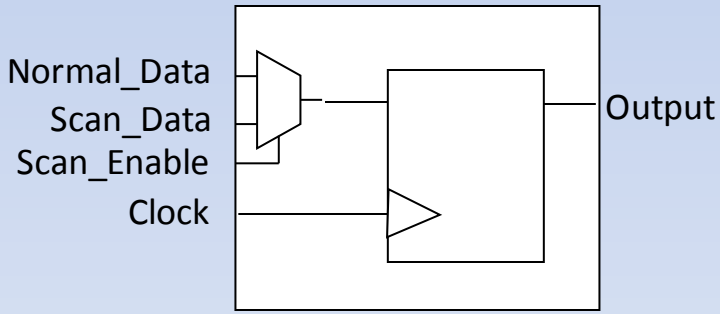
- By reducing the problem of generating tests for a sequential circuit to one of generating tests for a combinational circuit, scan DFT methodology reduces the test development cost.

- In many cases it enables the attainment of acceptable fault coverage

Scan Techniques

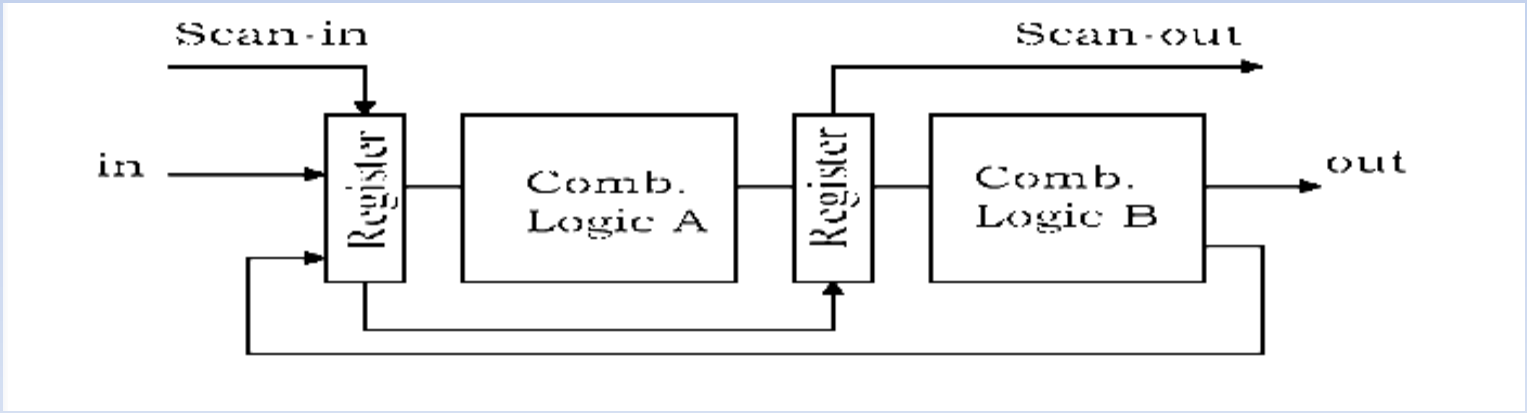
Scan based DFT can be achieved through 2 techniques

- Mux Based Scan – Multiplexer Based
  - Replaces every flip-flop with a mux-based flip-flop
- LSSD based Scan – Level Sensitive Scan Device



Mux Based Scan

- The flops have two modes of operation
  - Test Mode in which flops are connected in a serial shift register like structure
  - Normal Mode in which flops are connected to their respective combo blocks



Mux Based Scan

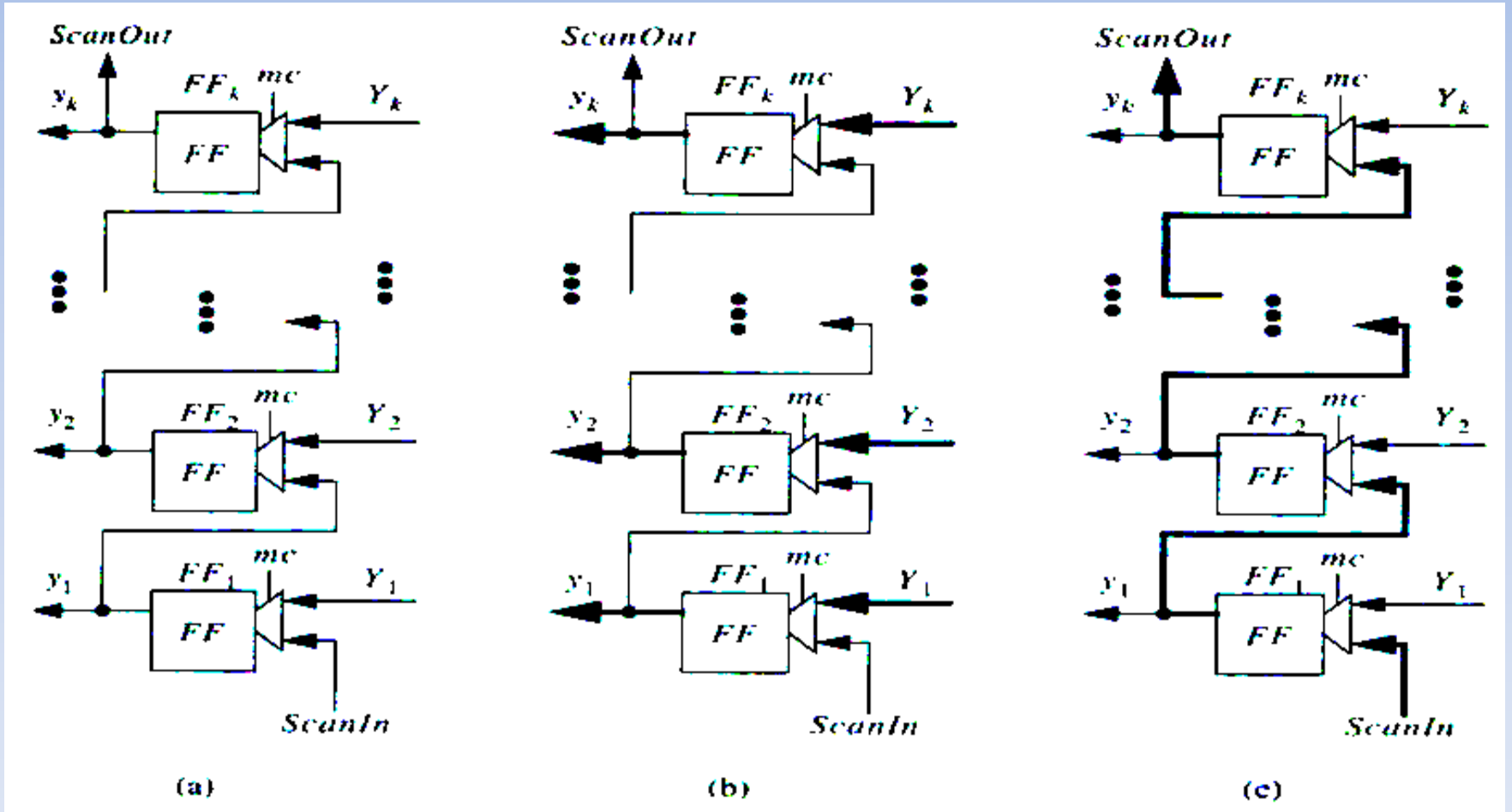
- Penalties include
  - Scan hardware occupies between 5-20% of silicon area
  - Performance impact
  - Additional Pins , e.g scan_in , scan_out

Muxed Scan Methodology

- Test control is added as primary Input
- All flops are replaced with scan flip-flops and connected serially through multiplexers
- Each flip-flop is controllable and observable from the primary input/ primary output
- Combinational ATPG methodology is used to test all the combinational logic in between the flops

Scan Chain

- Figure of Generic Scan Chain in various modes is as shown below
  - (a) Structure (b) Configuration in Normal Mode (c) Configuration in Test Mode

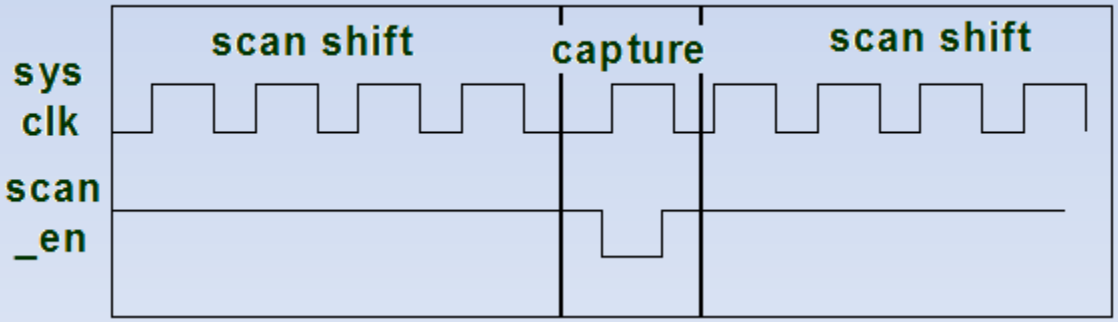


Scan Based Testing

- Design works in two modes
  - Scan Mode when SE = 1
  - Normal Mode when SE = 0
- The following steps are carried out for system with N flops
  - SE =1, now all flip-flops are connected in serial fashion
  - Apply the scan clock
  - Apply test patterns at the input serially through scan_in
    - one bit of the test pattern per clock cycle
  - Clock the system N times, called shift cycle
  - Now every flop is filled with the test patterns

Scan Based Testing

- SE = 0, now all flops are connected in normal mode
- Clock applied to circuit which works in normal mode
- Called Capture Cycle
- Combinational output is evaluated and stored in flops
- SE = 1, flops again rigged up in serial fashion
- System again clocked for N clock cycles, again shift cycle



Scan Based Testing

- Output is shifted out serially and observed through scan_out pin
- Total procedure takes 2N + 1 clock cycles

Scan Design Approach

There are two approaches to scan design

- Full Scan
  - The most predictable DFT methodology
  - All the flip-flops in the design become controllable and observable
  - Most widely adopted methodology in industry
    - Extensively researched and used for over 25 years
  - Enable faster ATPG (combinational ATPG)
    - Compatible with, and supported by all commercial ATPG/fault simulation tools
  - Achieve the highest fault coverage

Scan Design Approach

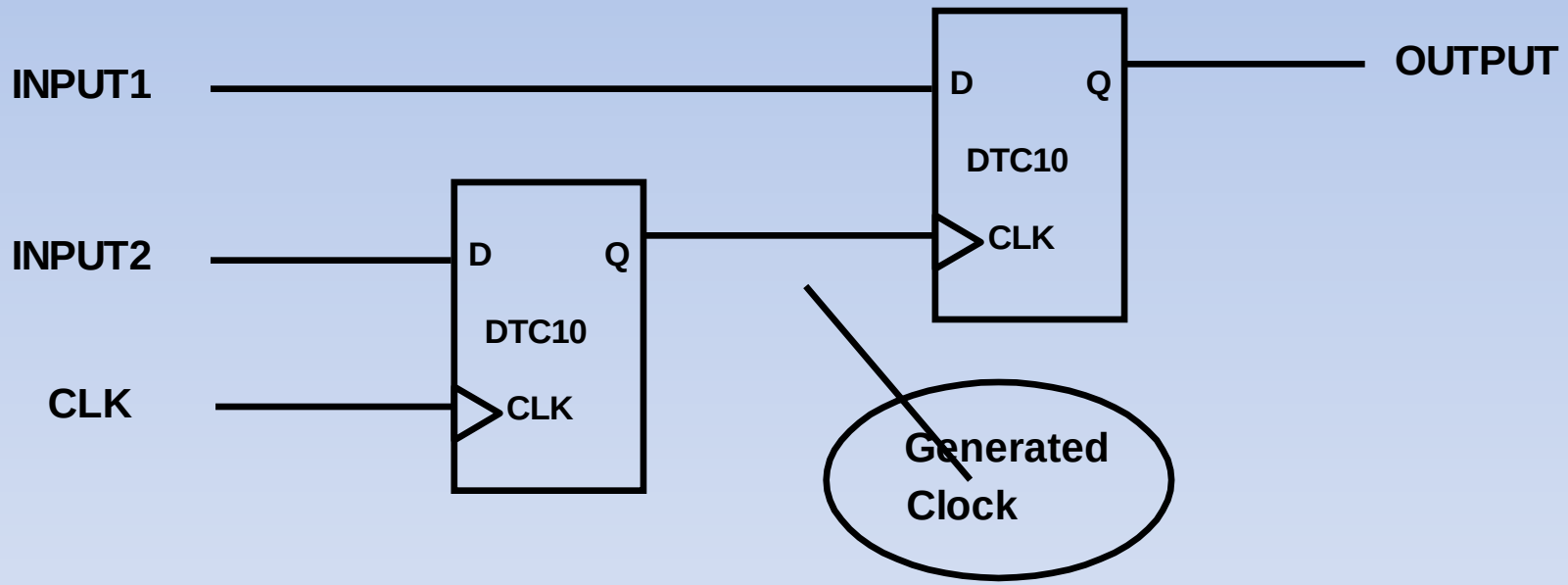
- Full Scan Drawbacks
  - Extra Pins
  - Extra Mux
  - Extra Routing
  - Mux Delay
  - Flop Delay due to extra load
- Partial Scan
  - Not all flip-flops are converted to be scannable
  - Not all flip-flops are controllable and observable
  - Partial Scan may be required for performance and area sensitive designs
  - Requires expensive computations (sequential ATPG)
  - Fault coverage is not predictable

Scan Design Rules

- For efficient scan design the circuit should follow certain rules, such as
  - Use only clocked D-type of flip-flops for all state variables
  - At least one PI pin must be available for test; more pins, if available, can be used
  - All clocks must be controlled from PIs
  - Clocks must not feed data inputs of flip-flops
- A set of design rules need to be satisfied for scan insertion to take place generally known as DFT DRC rules

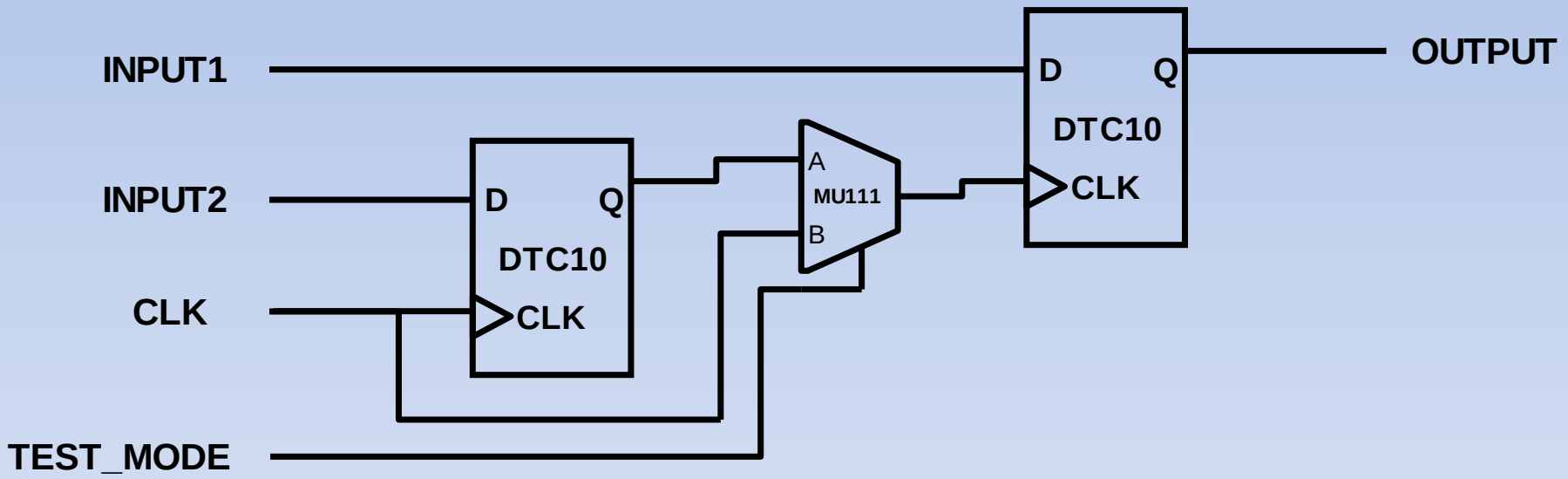
No Generated Clocks

- All internal clocks must be controlled by port level CLK signal (primary input) in scan test mode



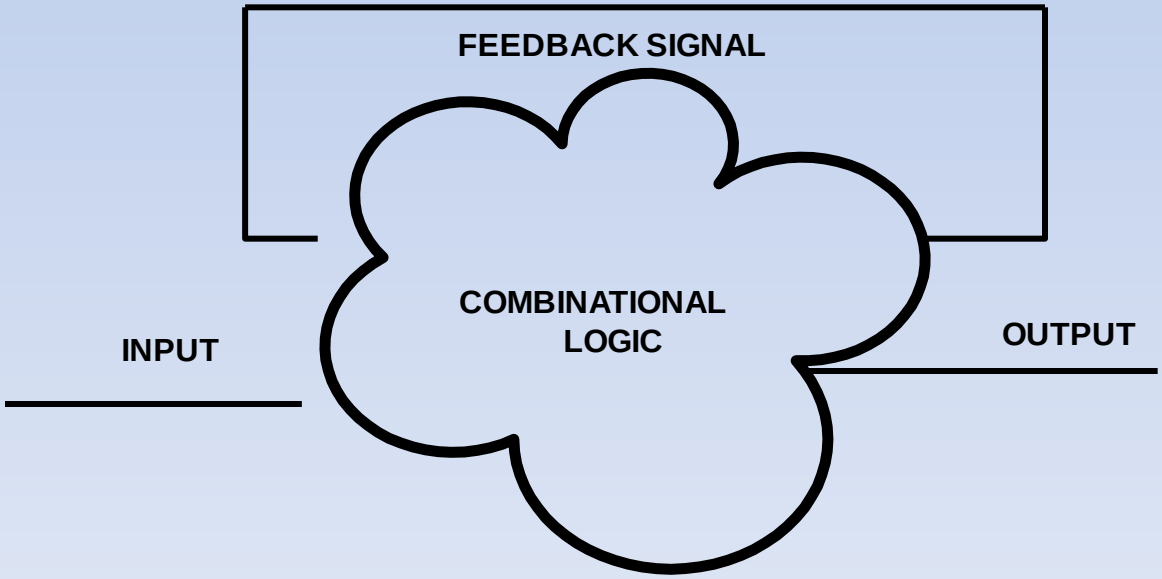
No Generated Clocks

- Rectification
  - Mux the generated clock with the primary clock input



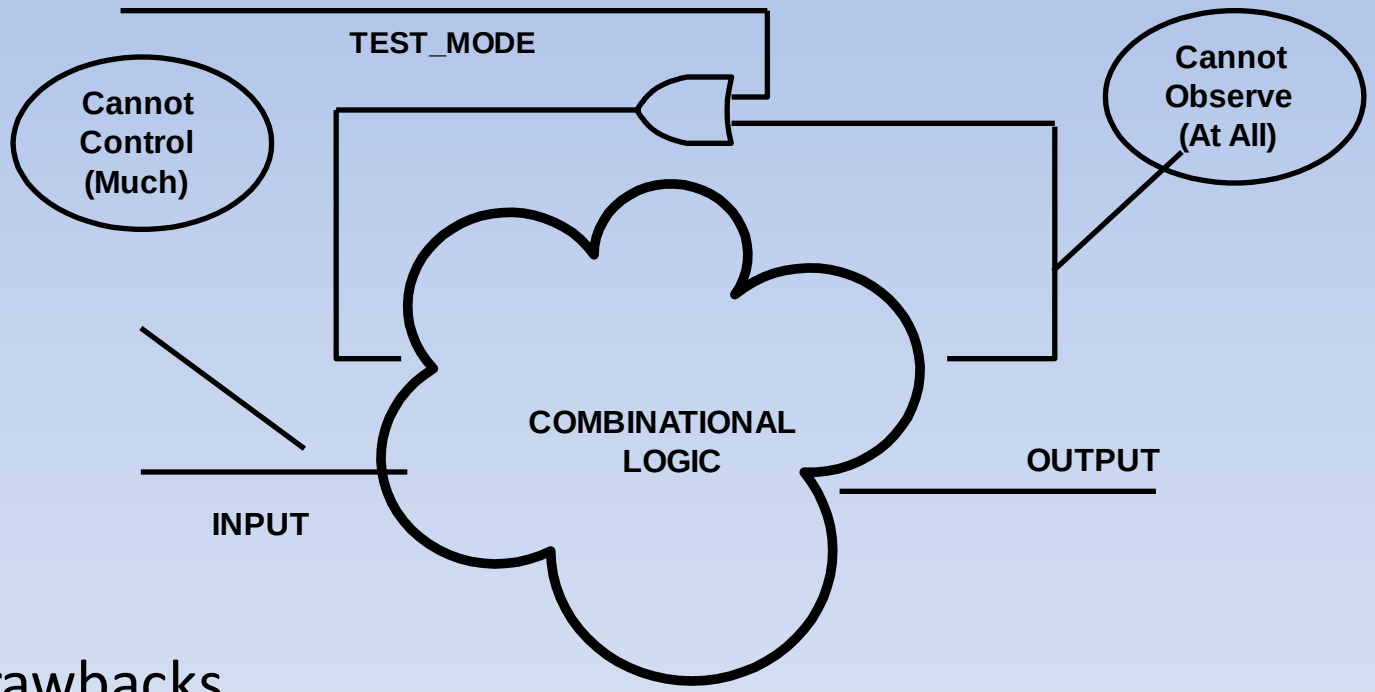
No Combinational Feedback

- Implementation of combination feedback circuit makes the combinational system to mimic sequential logic
  - Output depends on input and previous value



No Combinational Feedback

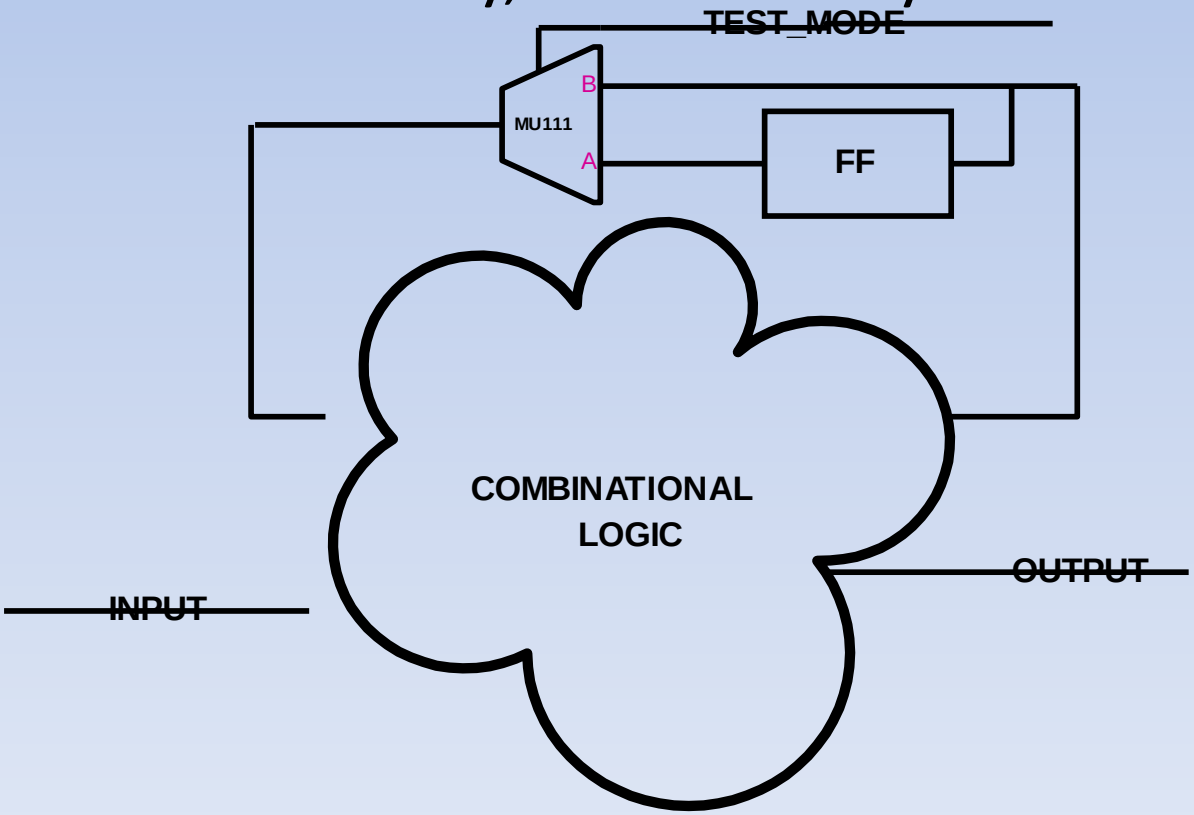
- Rectification
  - Break the feedback loop by means of and/or gate



  - Drawbacks
    - Feedback signal is not testable
    - Gate output is not testable

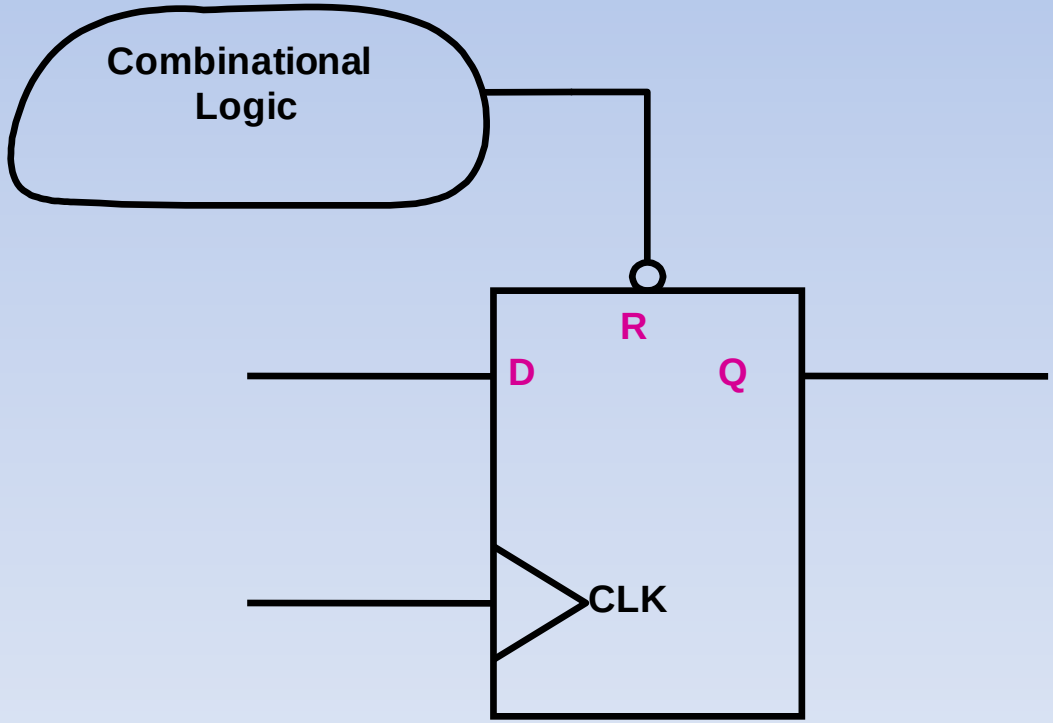
No Combinational Feedback

- Rectification
  - Break feedback loop by means of flop and mux
  - Increases controllability, observability and complexity



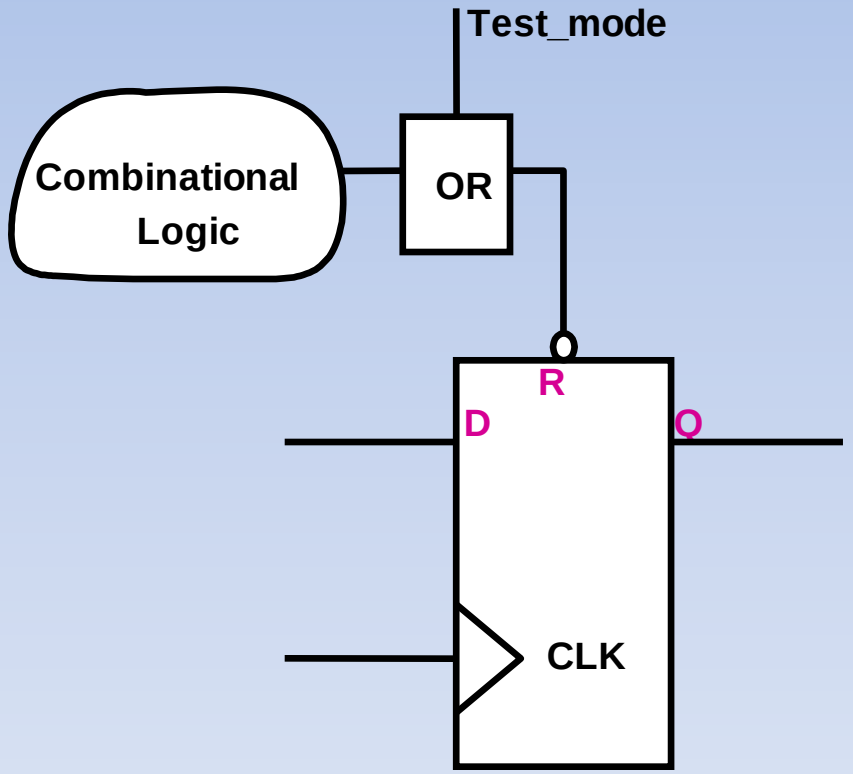
Avoid Asynchronous Reset

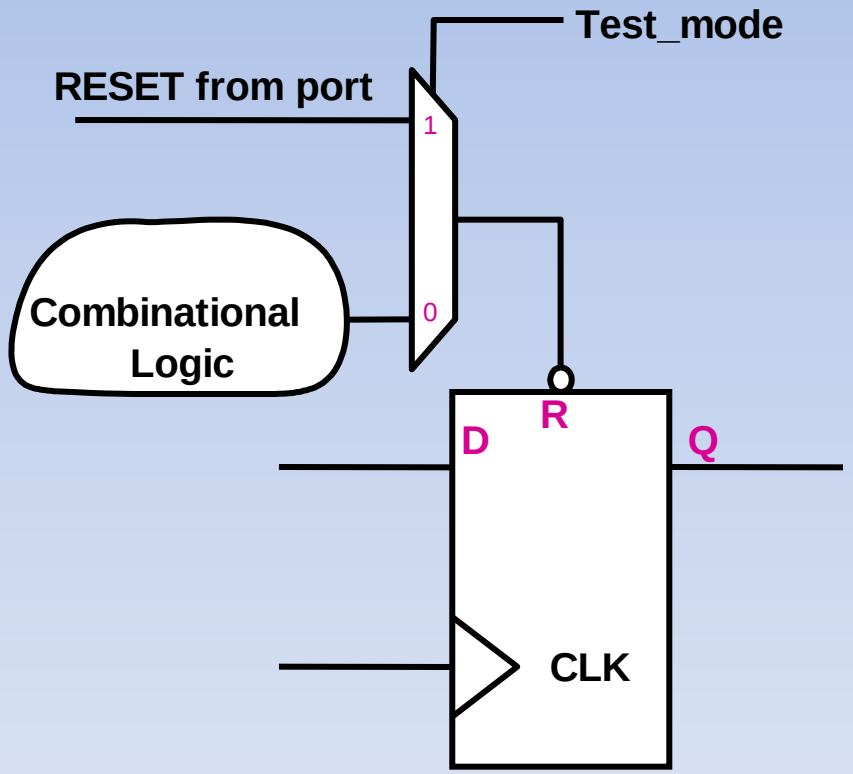
- No Internally generated asynchronous reset
  - Asynchronous controls if required should not be internally generated



Avoid Asynchronous Reset

- Rectification
  - Make asynchronous control signal controllable from input port

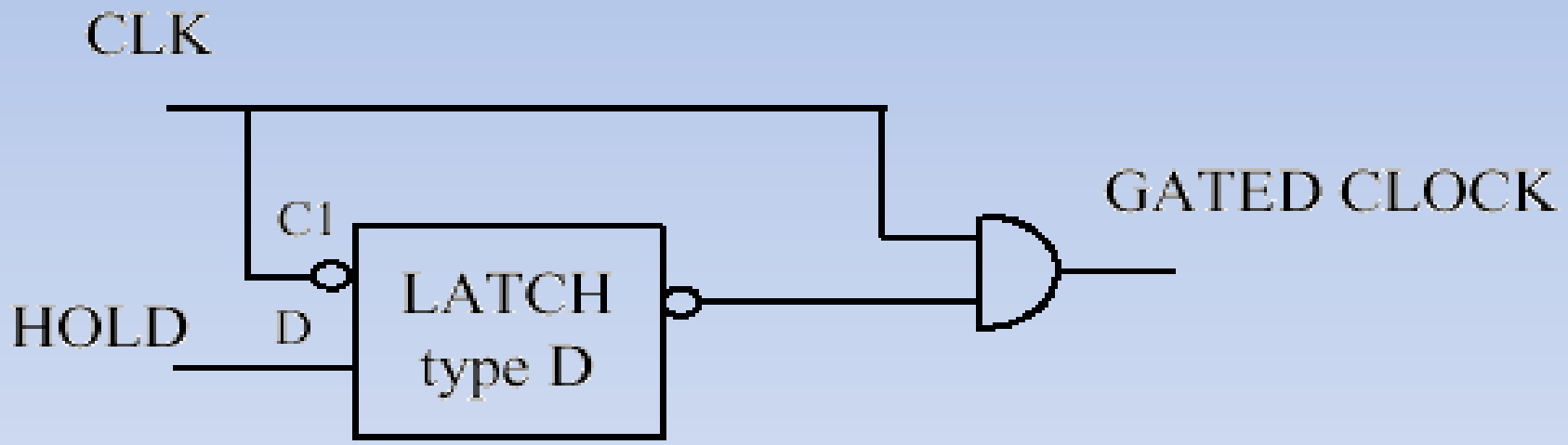




- Solution 1
- Solution 2

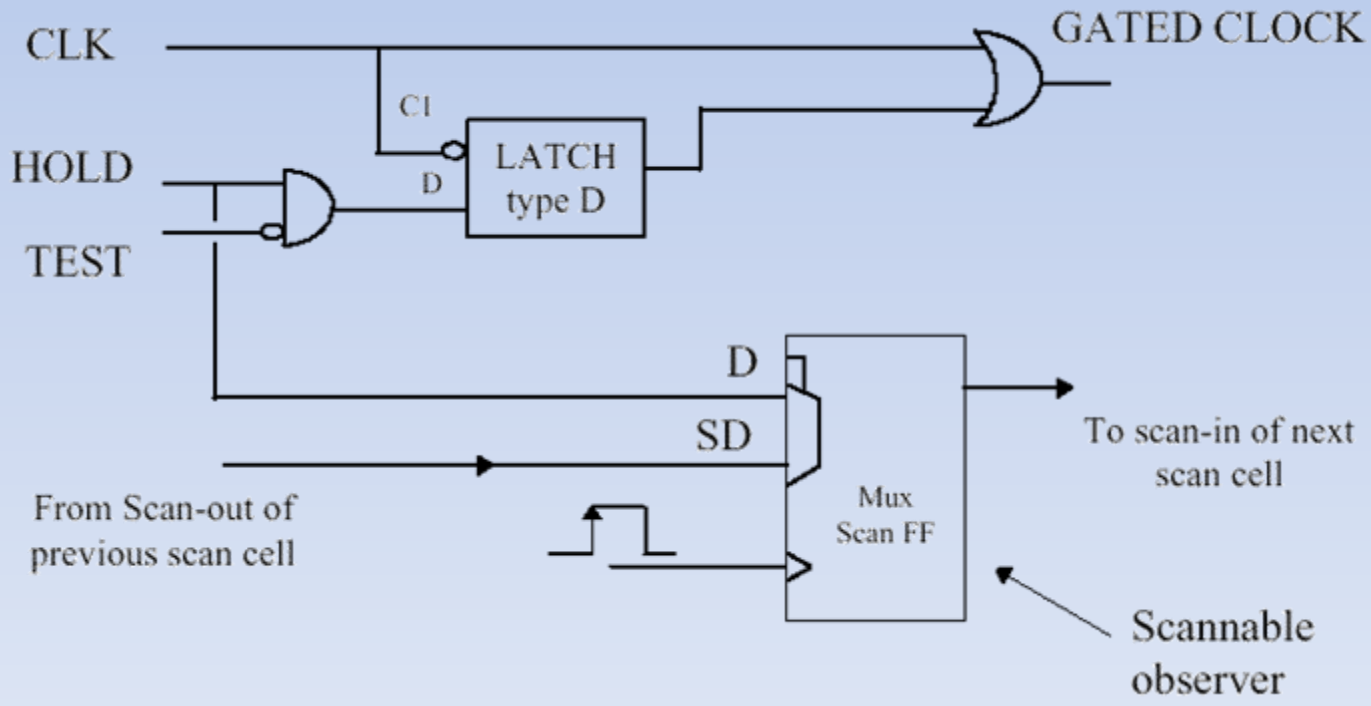
No Gated Clocks

- Gated Clocks may not be enabled during the scan shift cycle
  - No controllability on the gated clock



No Gated Clocks

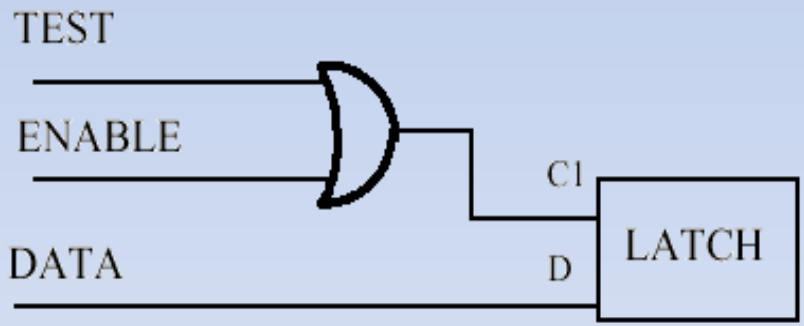
- Rectification
  - Gated clock should be enabled in the scan mode
  - Mux the gated clock with the master clock



No Latches

- NO Latches
  - Latches have to be avoided
  - In an edge triggered design, it is difficult to replace latches while stitching scan chain
  - There exists no edge triggered scan equivalent to latch

```
always @ (data, enable, test)
if(enable || test)
latch_signal = data
```



- Rectification
  - Latches have to be enabled for test to be successful

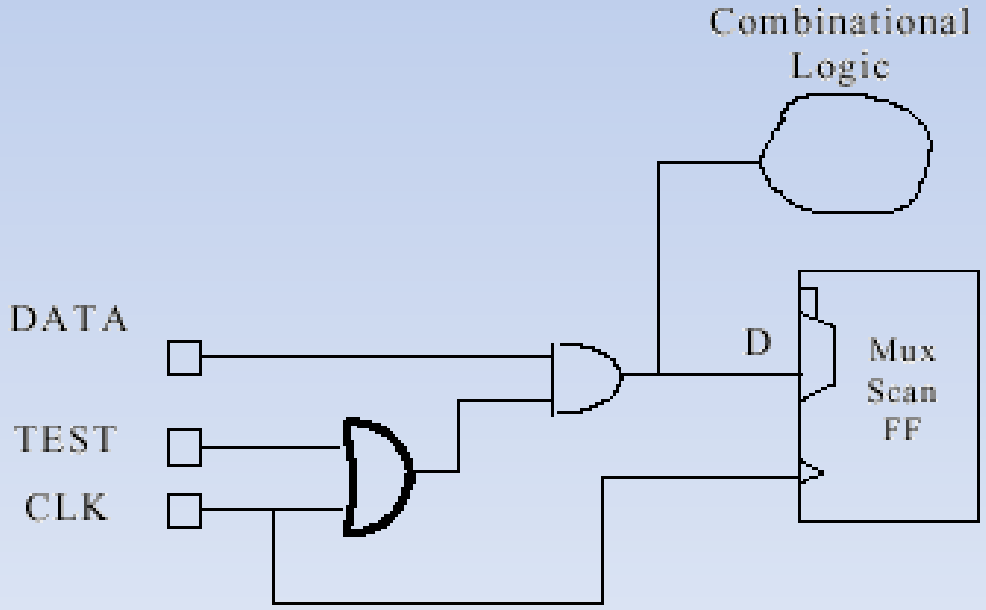
Shift Registers

- DO NOT replace shift registers
  - Shift registers are already connected serially
  - Need not be replaced by scan equivalents
  - Add Scan_Enable signal in the code

```
always@(posedge clock)
    if (RESET  && !SCAN_EN )
        shifter_bus <= 0;
    else
        if (ACTIVE_SHIFT || SCAN_EN)
            begin
                shifter_bus[16:1] <= shifter_bus[15:0];
                shifter_bus[0] <= DATA_IN;
            end
```

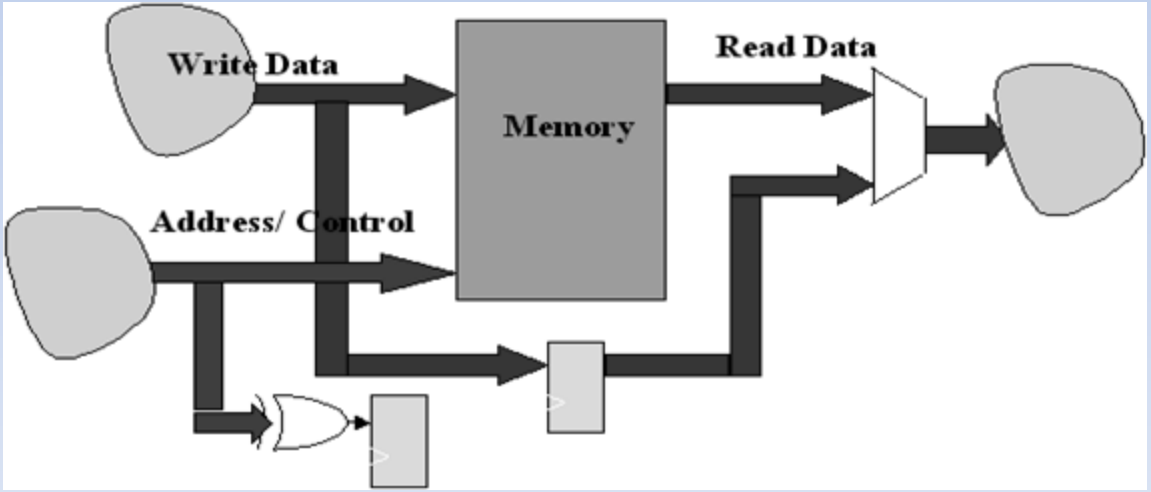
Clock Used as Data

- Clock should not be used in the data path
  - For ATPG to be successful there should be minimal mixing of clock and data
  - Clock shared by data leads to lesser fault coverage



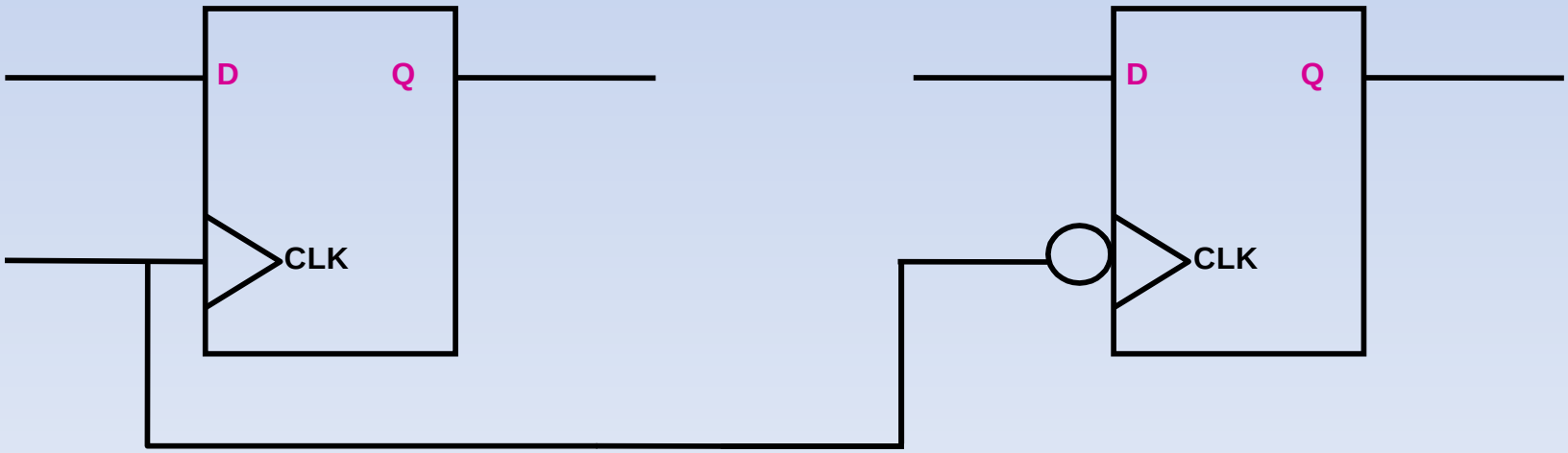
Bypass Memory

- Paths ending at memories are not observable
- Paths starting from Memory are not controllable
- Rectification
  - Bypass memory
  - Build a shadow logic around memory



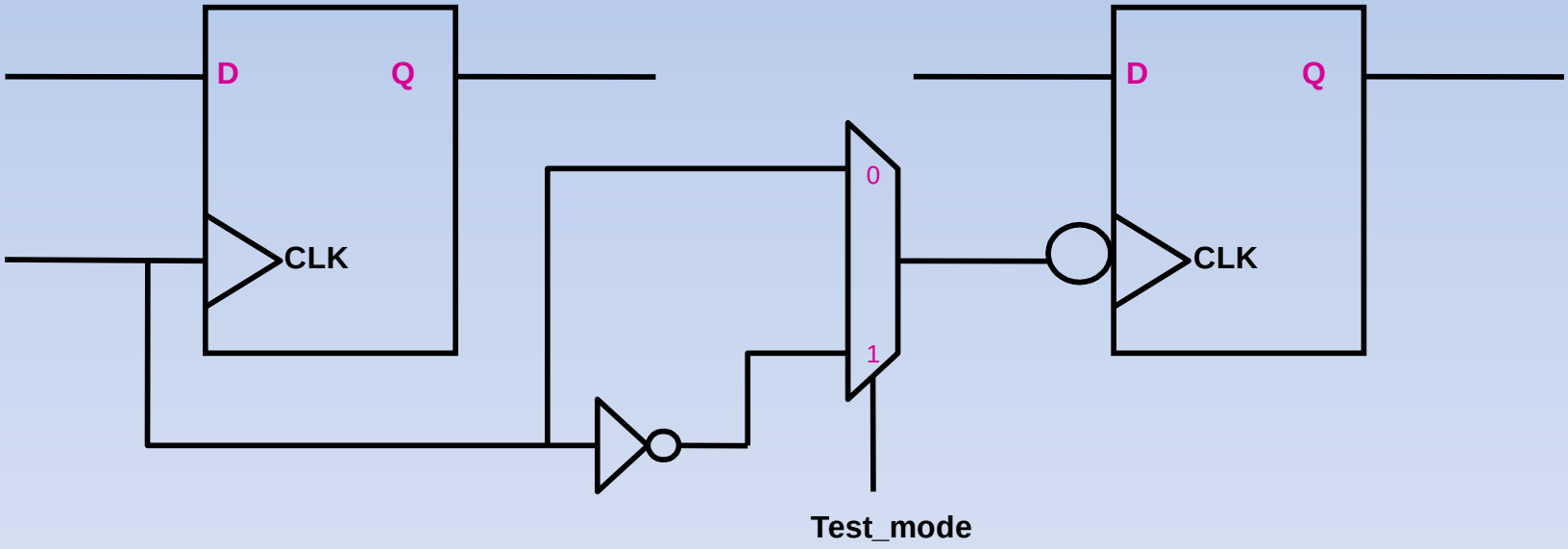
Mixed Edge Triggering

- Do not mix +ve edge triggered flops with –ve edge triggered flops in same scan chain
  - For ATPG to work in a clock cycle only one capture / shift should happen
  - Hence -ve edge flops should be triggered at the same time as +ve edge flops



Mixed Edge Triggering

- Rectification
  - Invert the clock of –ve edge triggered flops in the test mode

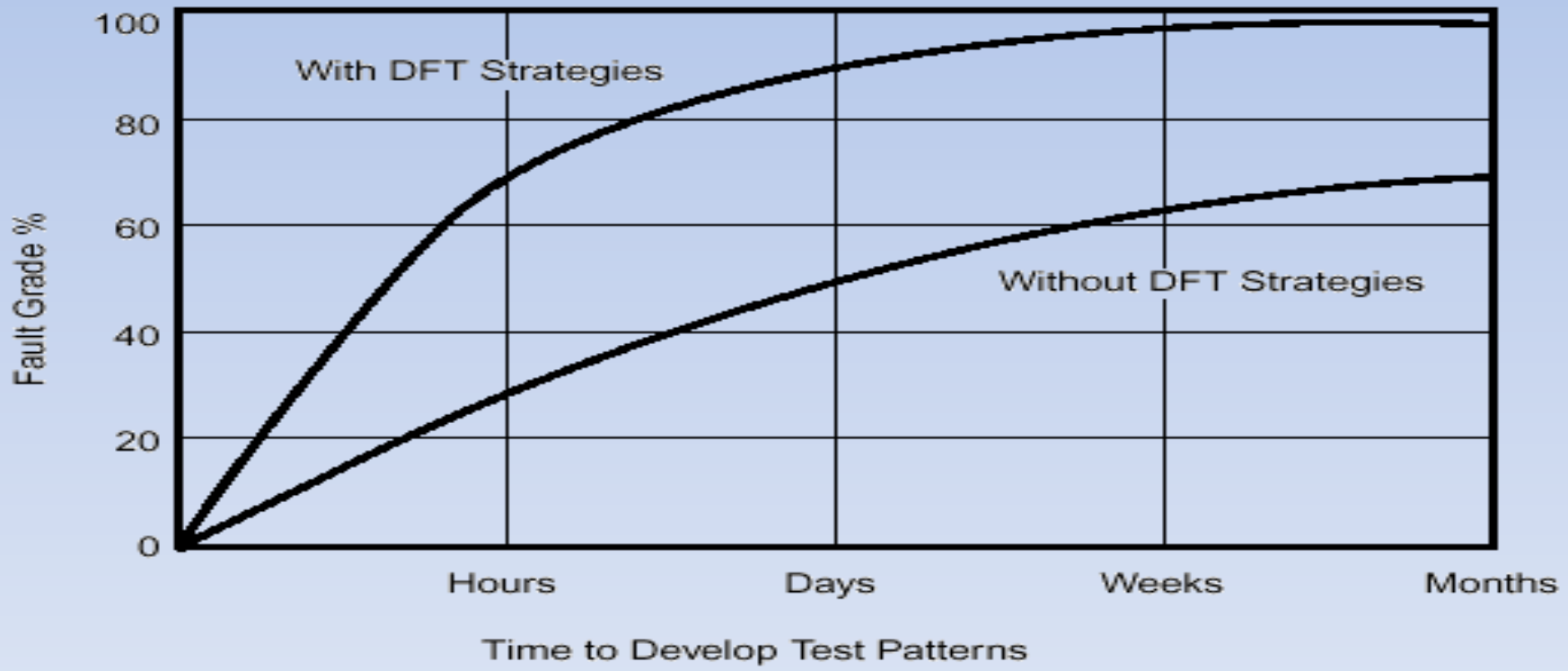


Scan Enable Buffering

- The Scan enable signal should be adequately buffered
- The scan enable signal feeds all the flip-flops in the design
  - Which makes the signal heavily loaded
- Scan enable can be considered equivalent to clock but without the same kind of switching activity
- The drive strength of the scan_enable port should be sufficiently high
  - Which needs to be taken care of during synthesis

Affect of DFT

- DFT increases Time to market as well as fault coverage
- Balance has to be stricken



Cons of Scan

- Disadvantages
  - Additional Pins
    - Scan Input, Scan Output, Scan Enable, Test Enable
    - Packaging cost increases
  - Performance Penalty
    - Longer setup Time
  - Area Overhead
    - FF without mux – 4/5 nand gates
    - FF with mux – 7/8 nand gates
      - But proven to increase area by about 7%
    - Area increases yield decreases
    - Silicon Cost increases
  - More Design Effort
    - Scan stitching, scan routing
  - High power when scan shifting

Pros of Scan

- Improves Confidence in the design
- Reliability and quality Increases
- Test application time and fault coverage increases
- Controllability and Observability of internal nodes increases
- Makes possible use of simpler ATPG algorithms
- Reduces failure rate and hence COST !!

Summary

- Test development cost has been understood
- Scan based DFT has been found suitable for sequential designs
- Objective of DFT has been identified
- Various DFT DRC rules have been studied
- Methods to overcome DFT DRC violations have been understood