Full Custom IC design flow

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Full Custom IC Design Flow using Cadence Tool

1. Custom Library Creation

- **Right-click** on the desktop and select **Create New Folder**.
- **Right-click** inside the folder and choose **Open in Terminal**.
- In the terminal, enter the following commands:
    - *csh*
    - *source /home/install/cshrc*
- Open the Virtuoso tool using the command:
    - *virtuoso*
- A **Command Interpreter Window (CIW)** will open — **do not close this window** until the entire procedure is complete.
- In the CIW, navigate to **File → New → Library**.
- Enter a **New Library Name** for your custom library.
- Select **Attach to an existing technology file** and click **OK**.
- In the **Technology Selection** window, select **gpdk045** (or your preferred technology) and click **OK**.
- The CIW will display a confirmation message indicating that the technology file is attached.
- To open your newly created library, go to **Tools → Library Manager**.
- In the Library Manager, select the **Library Name** you created.

2. Schematic Design

- In the Library Manager, click on **File → New → Cellview**.
- Enter a name for your schematic and click **OK**.
- A new **Schematic Editor** will open.
- In the schematic editor, go to **Create → Instance** to insert new components.
- In the **Instance Window**, select the **gpdk045** library from the dropdown menu.
- For the **Cell**, select **pmos1v**.
- Ensure the PMOS symbol appears, then click **Hide**.
- Place the PMOS in an appropriate position in the schematic workspace.

- Use the shortcut **'i'** to create new instances and place other required components, such as **nmos1v**.
- To create input and output ports, go to **Create → Pins**.
- In the **Pins Window**, select the direction as **Input** or **Output** as required.
- Type all input pin names (e.g., **vin vdd vss**) separated by spaces. **Pin names are case-sensitive**.
- The input pins will appear in order — place them appropriately in the schematic.
- Use the shortcut **'r'** to rotate components for proper alignment.
- Use the shortcut **'f'** to fit all components to the window.
- To add new pins quickly, use the shortcut **p**.
- Add the output pin **vout** and place it in the desired position.
- To connect all components, go to **Create → Narrow Wire**, or use the shortcut **w**.
- Click on the starting point of the wire, then click on the ending point (do not drag the mouse).
- After completing all connections, click on **Check and Save** in the **File Menu** or the toolbar.
- Check for any errors in the **CIW** and resolve them if required.

3. Symbol Design

- In the schematic window, go to **Create → Cellview → From Cellview**.
- In the **New Cellview** window, no changes are required — just click **OK**.
- In the **Symbol Generation Options**, adjust the position(top, bottom, left and right) of each pin as required. **Pin names are case-sensitive**.
- Click **OK**.
- A **Symbol Editor** window will open displaying a generic symbol.
- The **red box** indicates the **Place and Route (PR) boundary**, inside which no other components or connections should be placed.
- The **green box** represents the symbol itself.
- Pins are represented by **red squares**.
- You may delete the **red box** and **green box**, but **do not delete the pins**.
- Delete the **green box** and draw your own custom symbol if needed.

- Assign a **Part Name** to your symbol and ensure all pins are properly connected to the drawn symbol.
- Click on **Check and Save**.
- Check the **CIW** for any errors and confirm that both the **schematic** and **symbol** are saved in the Library Manager.

4. Testbench Creation

- In the Library Manager, click on **File → New → Cellview**.
- Give the cell a name ending with **_tb** for identification.
- A new **Schematic Editor** window opens.
- Add a new instance by selecting **your custom library** from the dropdown.
- In the **Cell** dropdown, select the **Schematic** cell.
- Ensure your symbol appears, then click **Hide**.
- Place your symbol in the workspace.
- For input and supply components, add instances from the **analogLib** library.
- Select **vpulse** for input and set the following values:
    - **DC voltage:** 1
    - **Voltage1:** 0 (low voltage)
    - **Voltage2:** 1 (high voltage)
    - **Period:** 20n
    - **Delay time:** 2n
    - **Rise time:** 1n
    - **Fall time:** 1n
    - **Pulse width:** 10n (half of period for 50% duty cycle)
- Place the **vpulse** near the **vin** pin, but **do not connect it directly**.
- Add an instance of **vdc** for supply voltage and set **DC voltage** to **1**.
- Place it near **vdd**, ensuring the **+** terminal is near the **vdd** pin. Again, **do not connect directly**.
- Add an instance of **gnd** and place it where necessary.

- Create a new pin named **vout** with direction as **Output**, and place it near the **vout** of your symbol. **Do not connect directly**.
- Use wires to connect all components correctly.
- Click **Check and Save**, and verify for errors in the **CIW**.

5. Simulation (Pre-layout)

- In the testbench schematic window, click on **Launch → ADE L** to run the **Spectre** tool.
- In the tool window, select **Analyses → Choose**.
- In the analysis window, select **tran** for transient analysis.
- Set the **Stop Time** to **100n**.
- Tick the **Moderate** checkbox and click **OK**.
- Next, go to **Outputs → To Be Plotted → Select on Design**.
- The testbench schematic window will reappear — select the wire connecting the **output** to the symbol, and then the wire connecting the **input** to the symbol. **Do not click on the component itself; only click the wire once**.
- Return to the **ADE L** window, click on **Simulation → Netlist and Run** to start the simulation.
- Verify the logic by checking and comparing the **input** and **output** graphs.
- If the results do not match your expected logic, go back to the original schematic, correct the design, recreate the symbol, create a new testbench, and run the simulation again.
- To separate the waveform plots for clarity, click on the **Split All Strips** option located next to **Family**.

6. Delay Calculation

- Right-click on the **input plot** and select **Send To → Calculator**.
- In the **Calculator** window, under the **Functions Panel**, select **Special Functions → Delay**.
- Copy the generated expression and paste it in **Signal1**.
- Go back to the graph, right-click on the **output plot** and select **Send To → Calculator**.
- Copy the new expression to **Signal2**.
- Change the **Threshold Value 1** and **Threshold Value 2** to **0.5**.

- Set **Edge Type 1** to **Falling** and **Edge Type 2** to **Rising**.
- Click **OK**.
- Click the **Evaluate Buffer** button next to **Append**.
- A new window will open displaying the delay — **note down the delay value**.
- Close the **Calculator** and **Waveform** windows once complete.
- In the ADE L window, click on **Session → Save State**, select the **Cellview** option, and click OK.

7. Layout Design

- Open the Library Manager and open your original schematic file by selecting your library, schematic cellview, and double-click on **Schematic**.
- In the schematic window, click on **Launch → Layout XL**.
- In the new layout window, select **Create New and Automatic**, then click **OK**.
- The schematic will appear on the left and the layout on the right.
- In the layout window, go to **Connectivity → Generate → All from Source** (use **Selected from Source** if there are many transistors).
- In the **Generate Layout** window, set **Minimum Separation** to **0.12** and tick the **In Boundary** checkbox.
- The layout will appear — press **Shift + F** to view MOS terminals.
- Use shortcut **S** to stretch boundaries as needed.
- Zoom into the **VDD** pin, then:
    - **Left-click** the VDD pin, then **Right-click** and select **Pin Placement**.
    - Select **VDD** from the list. Under **Attributes**, change the **Edge** to **Top**, click **Apply**, and then click **Hrail**.
    - Repeat for the **VSS** pin. Set **Edge** to **Bottom**, click **Apply**, and select **Hrail**. Close the window.
- Select the MOS transistor, then **Right-click** and select **Properties**.
- In the **Parameters** tab, change the **Bodytie Type** to **Integrated** and click **Close**.
- Use shortcut **P** to join the metal terminals:
    - Connect **Drain to Drain**, then extend it to the **VOUT** pin.
    - Connect **VDD** to the **PMOS Source** and **VSS** to the **NMOS Source**.

- For the **Poly Layer** connections:
    - From the **Vin** pin, start drawing the **Metal Layer** until it reaches the minimum required distance.
    - **Right-click** on the endpoint, select **Via Down To → Poly**.
    - Place the via connection, then continue to connect the **Poly Layer** to the **Gate Terminal**.
- On the left side under **Layers**, click on **Nwell**.
- Use shortcut **R** to draw a rectangle around the PMOS region.
- Ensure all connections are well-spaced and correct before saving.

8. DRC and LVS Check

- In the **Layout Window**, click on **Assura → Technology**.
- Click on the **three dots** next to the text bar.
- In the window, double-click on the **two dots** repeatedly until the **install** folder appears.
- Then select the following path:
    - **install → foundry → analog → 45nm_rev**.
- On the right side, select **assura_tech.lib** and click **OK**.
- Back in the layout window, go to **Assura → Run DRC**.
- In the **Run DRC** window:
    - Enter **Run Name** as **drc**.
    - Select **gpdk045** from the **Technology** dropdown.
    - Click **OK** and confirm by selecting **Yes** when prompted.
- Check the results for any design errors and correct them as needed, until no errors occur.
- Next, go to **Assura → Run LVS**.
- In the **Run LVS** window:
    - Enter **Run Name** as **lvs**.
    - Select **gpdk045** from the **Technology** dropdown.
    - Click **OK** and ensure there are **zero DRC and LVS violations** before proceeding.

9. RC Extraction

- In the **Layout Window**, click on **Assura → Run Quantus**.
- Under the **Setup** tab:
    - Select **Technology** as **gpdk045(whichever you chose)**.
    - Select **Ruleset** as **Typical** (only for 45nm technology).
    - Change the **Output** to **Extracted View**,
    - Enter a dot (.) as the **Library Prefix**.
- Under the **Extraction** tab:
    - Select **RC** as the **Extraction Type**.
    - Enter **vss** (case-sensitive) as the **Reference Node**.
- Under the **Netlisting** tab:
    - Select **Include as Comment** for the **Parasitic Capacitor Model** (only for 45nm technology).
- Click **OK**.
- In the **Library Manager**, look for "**av_extracted" file** and double-click to open it.
- If you zoom in, you can see the parasitic resistance and capacitances.

10. Post-Layout Simulation

- **In the Library Manager, select the Testbench Cellview, and then select the Testbench Schematic.**
- **Click on File → New → Cellview.**
- **Change the Type to Config and click OK.**
- **In the new configuration window:**
    - **Click on Use Template, select Spectre from the dropdown, and click OK.**
    - **Change the View to Schematic and click OK.**
- **In the Hierarchy Editor window:**
    - **Select Tree View.**
    - **Select I0, then Right-click → Set Instance View → av_extracted.**
    - **Click the + before I0 to expand the folder and confirm that parasitic R and C are imported.**

    - **In Table View, locate the View Found column.**
    - **Right-click on the 3rd column (NONE) and select Set Cellview → av_extracted. Click Save.**

- **Now the Post Layout Schematic is available.**
- **Click on Launch → ADEL.**
- **In the ADEL window, click Session → Load State → Cellview.**
- **Click on Simulation → Netlist and Run.**
- **Note down the Post Layout Simulation Delay from the output plot.**

11. GDSII File Extraction

- **Open the CIW window and navigate to File → Export → Stream → Xtream Out.**
- **In the new window:**
    - **Under Library, select the respective library.**
    - **Select the correct Cell and View (Layout), then click OK.**
- **In the Technology Library field, enter gpdk045.**
- **Click on Translate, then select Yes when prompted.**
- **After the process completes, a strmOut.log file will appear. Close it.**
- **Go back to your working folder and look for a .gds file.**
- **Open the .gds file with a text editor for verification.**