Semi-Custom IC Design Flow

1. **Folder Setup**
    - Create a new folder with the name of the experiment.
    - Inside this folder, create another folder named simulation.
    - Right-click in the simulation folder and select Open in Terminal.
2. **Create Source Code File**
    - Type the command: *gedit source_counter.v*
    - This opens the text editor.
    - Write the Verilog program in this file, save and close it.
3. **Create Testbench Code File**
    - Type the command: *gedit testbench_counter.v*
    - Write the testbench code in this file, save and close it.
4. **Setup Environment**
    - Execute the following commands to set up the environment:
        - *csh*
        - *source /home/install/cshrc*
5. **Choose One of the Following Procedures**
    - After setting up the environment, proceed with either the **Single-Step Procedure** or the **Multi-Step Procedure**.

5.1 Single-Step Procedure

- In the terminal, run the following command:

  xrun source_counter.v testbench_counter.v -access +rwc -gui

- In the **Design Browser 1** window, select **counter_test.v** file and click on the **Waveform icon** on the right top (Send to Waveform).
- In the **Waveform 1** window, click on **Run**.

5.2 Multi-Step Procedure

- Execute the command: *nclaunch -new*
- In the Incisive tool, perform the following steps:
    - **Click on Multiple Step.**
    - In the "Open Design Directory" window, select **Create cds.lib file**.
    - Click **Save**. In the "New cds.lib File" dialog box, select **Don't include default library (Verilog design)** (3rd option) and click **OK**.
    - In the NClaunch window (left side), select the source code file and click the **second icon (Verilog Compiler)** in tools.
    - Repeat the above step for the **testbench code file**.
    - On the right side, click on **+** next to the **worklib folder**, select the **counter file**, and click the **third icon (Launch Elaborator)** in tools.
    - Repeat the above step with the **counter_test file**.
    - Click **+** next to the **snapshots folder**.
    - Select **worklib counter_test:module**, and click the **fourth icon (Launch Simulator)** in tools.
    - In the **Design Browser 1** window, select **counter_test**, click on the **Waveform icon** on the right top (Send to Waveform).
    - In the **Waveform 1** window, click on **Run**.

6. **Synthesis Process**
    - Navigate to the **experiment folder** and create a new folder named synthesis.
    - Copy the **source code file** into the synthesis folder.
    - Open the terminal in the synthesis folder and execute the following command: *gedit input_constraints.sdc*
    - Type the **constraints code** in the editor, save, and close the file.
    - Execute the following command: *gedit script.tcl*
    - Type the **script code**, save, and close the file.

7. **Cadence Genus Flow**
    - Open **Cadence Design Suite** and enter the command: *genus*
    - In the terminal, execute the command: *source script.tcl*
    - In the **Genus** window:
        - Click on **+** next to **Layout** and select **Schematic** to view the gate-level diagram.
        - Select **Timing**, then **Debug Timing**, and click **OK**.
        - Check the **Slack** column — all values should be positive. Review **Total Paths** and **Failing Paths** (if any slack is negative, it indicates failing paths).
        - To adjust slack, modify the **Period** in the **timing_contraints** file.
        - Under the **Path List**, right-click on any path and select **Show Timing Path Analyzer**.
        - Go to the **Synthesis** folder and review the **Area Report File**, **Gate Report File**, and **Netlist Report File**.