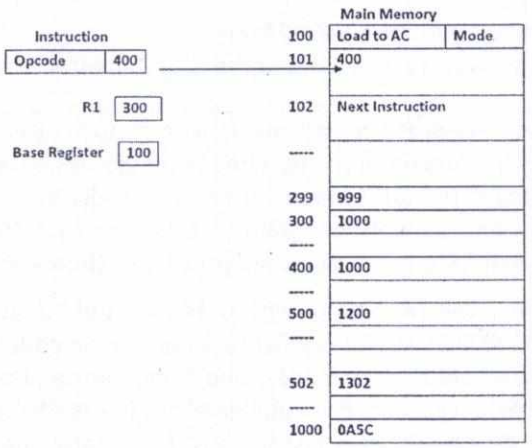
Roll Number: _____

Thapar Institute of Engineering & Technology, Patiala
Department of Computer Science &Engineering

B. E.(COE/CSE) : EST	Course Code: UCS510 Course Name: Computer Architecture and Organization
14 Dec'2022	9:00 AM – 12:00AM
Time: 3 Hours, M. Marks: 45	Faculty: SHI/SOL/ALK/YAS/SHR

Note: All questions carry equal marks and compulsory to attempt. Attempt all questions in order and assume missing data if any.

Q.1.A	The content of program counter in the basic computer is 3AC (all number are in hexadecimals), the content of AC is 7EC3. The content of memory at address 3AC is 935E. The content at memory address 35E is 08AC and content at memory address 8AC is 7A9F. The opcode bits of ADD and AND instructions are 001 and 010 respectively. What is the instruction that will be fetched and executed next? Show the binary operation that will be performed in AC when the instruction is executed.	**(3+6)**
Q.1.B	What is DMA? Explain its working with neat and clean diagram (Consider following points: Diagram, Registers included, step by step working, modes of transfer).	
Q.2.A	Consider a 16-bit processor in which the main memory appears as:  Determine the effective address and operand to be loaded for the Indirect, PC relative, Base, Register Indirect, and Auto decrement using R1 addressing modes.	**(5+4)**
Q.2.B	a) Differentiate between memory references instructions and register reference instructions with one example of both. b) Differentiate between Interrupted I/O and Programmed I/O. (4 differences only)	

Q.3. A	Consider the execution of the following sequence of instructions on a five-stage pipeline consisting of IF (instruction fetch), ID (instruction decode), OF (operand fetch), EX (execute), and WB (write-back) without operand forwarding. I1 -> LOAD -1, R1 //R1<- -1 I2 -> LOAD 5, R2 //R2 <- 5 I3 -> SUB R2, 1, R2 //R2 <- R2 – 1 I4 ->ADD R1, R2, R3 //R3 <- R1 + R2 I5 -> ADD R4, R5, R6 //R6 <- R4 + R5 I6 -> SHL R //R3 <- Shift Left(R3) I7 -> ADD R6, R4, R7 //R7 <- R4 + R6 I8 -> JMP 0A00H //Jump to 0A00H a). Find the number of clock cycles by showing the pipeline timing diagram required to complete the sequence of instructions. b). Write the various hazards observed in the given sequence of instructions.	(6+3)
Q.3.B	Consider the two 8-bit numbers A= 01000001 and B= 10000100. a) Give decimal equivalent of each number assuming that (i) they are unsigned and (ii) they are signed. b) Add the two binary numbers and interpret the sum assuming that the numbers are (i) unsigned and (ii) signed. c) Determines the values of the C, S, Z and V status bits after the addition.	
Q.4.A	Consider a non-pipelined processor with a clock rate of 3.6 gigahertz and average cycles per instruction of 5. The same processor is upgraded to a pipelined processor with six stages, but due to the internal pipeline delay, the clock speed is reduced to 2.5 gigahertz. Assume there are stalls of 1 ns after each stage in the pipeline. Find the speed up achieved in this pipelined processor. Show each step clearly.	(5+4)
Q.4.B	The memory unit of a computer has 4K words of 32 bits each. The computer has an instruction format with three fields: an operation code field, a mode field to specify one of three addressing modes, and a memory address. An instruction takes one memory word, calculate the number of bits in each fields of the instruction format. If there are 60 two-address instructions, how many one-address instructions can be formulated?	
Q.5.A	A digital computer has a memory unit of 64K x 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. How many bits are there in the tag, index, block, and word fields of the address format? How many bits are there in each word of cache and how are they divided into functions? Include a valid bit. How many blocks can the cache accommodate?	(5+4)
Q.5.B	The access time of cache memory is 35 nsec and that of main memory is 500 nsec. It is found that 80% of memory requests are for read and remaining for write. If the hit access for read is 0.9 and hit ratio for write is 1 and write through protocol is used (directly write to memory), then what is the average memory access time.	