Roll Number:_____

Thapar Institute of Engineering & Technology, Patiala

Department of Computer Science &Engineering

Course Code: UCS510 Course Name: Computer Architecture and Organization	B. E.(COE/CSE) : MST
28/9/2022	1:00 PM - 3:00 PM
Time: 2 Hours, M. Marks: 30	Faculty: SHI/SOL/ALK/YAS/SHR

Note: All questions carry equal marks. Attempt all questions.

Q.1.	A. A circuit outputs a digit in the form of 4 bits. 0 is represented by 0000, 1 by 0001..., 9 by 1001. A combinational circuit is to be designed which takes these 4 bits as input and outputs 1 if the digit ≥5, and 0 otherwise. If only AND, OR and NOT gates may be used, Draw the circuit and Find the minimum number of gates required? B. A computer uses a memory of 65536 words with 8 bit in each word. Determine the size of PC, IR, DR, AC?	**(4+2)**
Q.2	A. Let R1 and R2 be two 4-bit registers that store numbers in 2's complement form. If the value to be stored in R1 is 1100 and R2 is 1010 what will be the value of Vs (overflow bit) after performing operation R1+R2? B. Minimize the given Boolean Expression by using the four-variable K-Map. F (A, B, C, D) = Σ m (1, 5, 6, 12, 13, 14) + d (2, 4).	**(2+4)**
Q.3	A. A processor has 64 registers and uses 16-bit instruction format. It has two types of instructions: I-type and R-type. Each I-type instruction contains an opcode, a register name, and a 4-bit immediate value. Each R-type instruction contains an opcode and two register names. If there are 8 distinct I-type opcodes, then how many maximum number of distinct R-type opcodes will be possible? B. Convert following numbers in IEEE-754 floating point 32 bit short precision format. **A. $(14.25)_{10}$** **B. $(C164)_{16}$**	**(3+3)**
Q.4	Perform the signed multiplication of following number using Booth's Algorithm with clear steps **[12*5]** using 5 bits to represent both multiplier and multiplicands.	**(6)**
Q.5	Design an arithmetic circuit with one selection variable S_0 and two 4-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram for C_{in}=0 / C_{in}=1 S_0=0: A+B / Transfer A S_0=1: A+1 / A-B	**(6)**