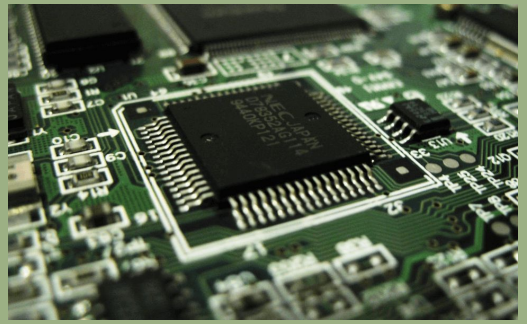

8085 Microprocessor

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Instruction Cycle

·An instruction is a command given to the microprocessor to perform a specific operation on the given data.

·Sequence of instructions written for a processor to perform a particular task is called a program.

·Program & data are stored in the memory.

· The microprocessor fetches one instruction from the memory at a time & executes it. It executes all the instructions of the program one by one to produce the final result.

· The necessary steps that a microprocessor carries out to fetch an instruction & necessary data from the memory & to execute it constitute an instruction cycle.

·In other words, an instruction cycle is defined as the time required completing the execution of an instruction.

·An instruction cycle consists of a fetch cycle and an execute cycle. The time required to fetch an opcode (fetch cycle) is a fixed slot of time while the time required to execute an instruction (execute cycle) is variable which depends on the type of instruction to be executed.

Instruction Cycle (IC) = Fetch Cycle (FC) + Execute Cycle (EC)

Fetch Operation

- The first byte of an instruction is its op-code. An instruction may be more than one byte long.
- The other bytes are data or operand address. The program counter (PC) keeps the memory address of the next instruction to be executed. In the beginning of a fetch cycle the content of the program counter, which is the address of the memory location where op-code is available, is sent to the memory.
- The memory places the op-code on the data bus so as to transfer it to the microprocessor.
- The entire operation of fetching an op-code takes three clock cycles.

- A slow memory may take more time. In case of a slow memory the CPU has to wait till the memory sends the opcode. The clock cycle for which the CPU waits is called wait cycle.

Execute Operation

-The opcode fetched from the memory goes to the data register, DR (data/address buffer in Intel 8085) and then to Instruction Register, IR.
- From the Instruction Register it goes to the decoder circuitry which decodes the instruction.
- The decoder circuitry is within the microprocessor.
- After the Instruction is decoded, execution begins.
- If the operand is in the general purpose registers, execution is immediately performed.
- The time taken in decoding and execution is one clock cycle.
- If an instruction contains data or operand address which are still in the memory, the CPU has to perform some read operations to get the desired data.
- After receiving the data it performs execute operation.
- A read cycle is similar to a fetch cycle .

Machine Cycle and State

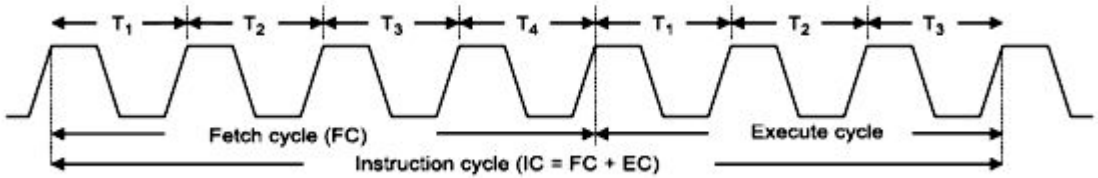
·Machine cycle is defined as the time required for completing the operation of accessing either memory or I/O device. In the 8085, the machine cycle may consist of three to six T states.

·The T-state is defined as one sub-division of the operation performed in one clock period.

· These sub-divisions are internal states synchronized with the system clock.

·In every machine cycle the first operation is op-code fetch and the remaining will be read or write from memory or IO devices.

- So one clock cycle of the system clock is referred to as a state.



Timing Diagram

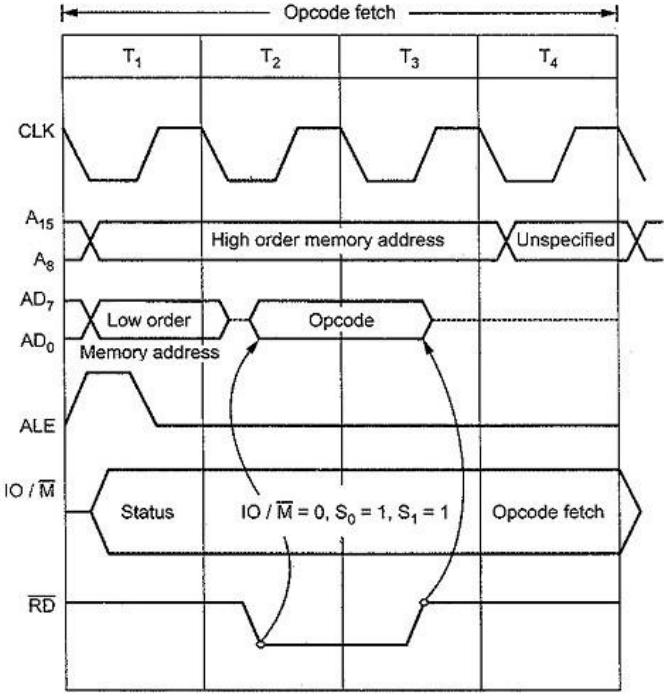
- The necessary steps which are carried out in a machine cycle can be represented graphically. Such a graphical representation is called timing diagram. The timing diagram for opcode fetch, memory read, memory write, I/O read and I/O write will be discussed further:

Opcode fetch machine cycle

- The opcode fetch machine cycle (OFMC) involves the fetching of the opcode of the instruction to be executed and the decoding process of that opcode. Usually, it consists of four T states. The timing diagram of a typical OFMC is explained below:

1st T state

- During the first T state, the address of the location where the opcode is stored is loaded on the address bus. In 8085, this address is stored in a 16-bit register called the program counter. Higher eight bits of the address are loaded on A_8-A_{15}, and the lower eight bits of the address are loaded into AD_0-AD_7 for demultiplexing.
- Also, the ALE signal becomes active in the first T state to indicate that the data on AD_0-AD_7 pins are the lower address bits.
- IO/$\overline{M}$ signal becomes low at the beginning of the first T state to indicate that the opcode will be fetched from memory (reading from memory).
- At the beginning of the first T state, signals S_1 and S_0 take the value 1 and 1 respectively to indicate that it is an opcode fetch machine cycle.



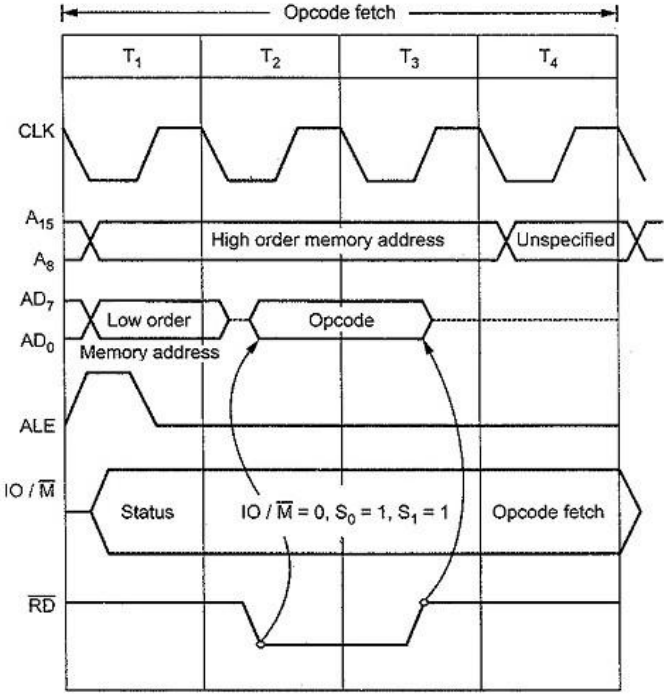
Opcode fetch machine cycle contd..

2nd T state

- By the beginning of the 2nd T state or the end of 1st T state, the ALE signal goes low. By this time, 8085 expects that the lower address bits are latched, and AD_0-AD_7 is free to be used as a data bus.
- At the beginning of the second T state, $\overline{RD}$ goes low, indicating that the read process has started. Meanwhile, higher address bits are present in A_8-A_{15}, and lower address bits are expected to be latched.
- As $\overline{RD}$ goes low, the opcode (eight bits) is loaded into the data bus AD_0-AD_7.

3rd T state

- The opcode loaded on the data bus is present there until the middle of the third T state.
- During the third T state, $\overline{RD}$ goes up, indicating that the read operation is completed and 'the opcode is fetched' and placed in the instruction register.
- The data on the data bus and the higher address bits on A_8-A_{15} exist until the middle of this T state.



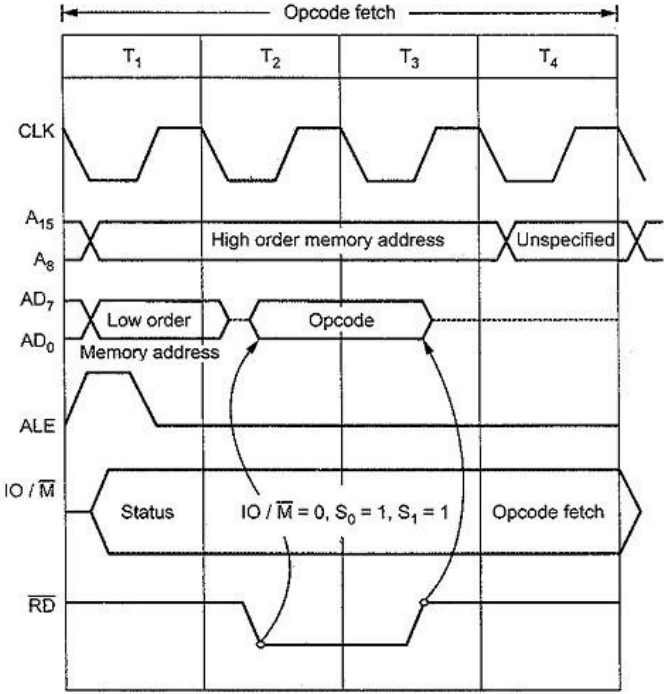
Opcode fetch machine cycle contd..

4th T state

- During the fourth T state, the fetched opcode is decoded. There is nothing much to observe in the timing diagram during this process.
- In case of some simple one-byte instructions like STC (set carry flag), execution is also completed during the fourth T state. One such instruction is MOV A, D.
- During the fourth T state, after decoding the opcode, the microprocessor decides if it needs fifth and sixth T states, or should proceed to the next machine cycle.

5th and 6th T state

- In case of one-byte instructions that operate on 16-bit data and some other instructions, OFMC may extend up to six T states. During the fifth and sixth T states, execution of these instructions takes place. Since these instructions are simple, they get executed in the OFMC itself. Examples of such instructions are DCX, INX, PCHL, SPHL, CALL, RSTN and conditional RET.

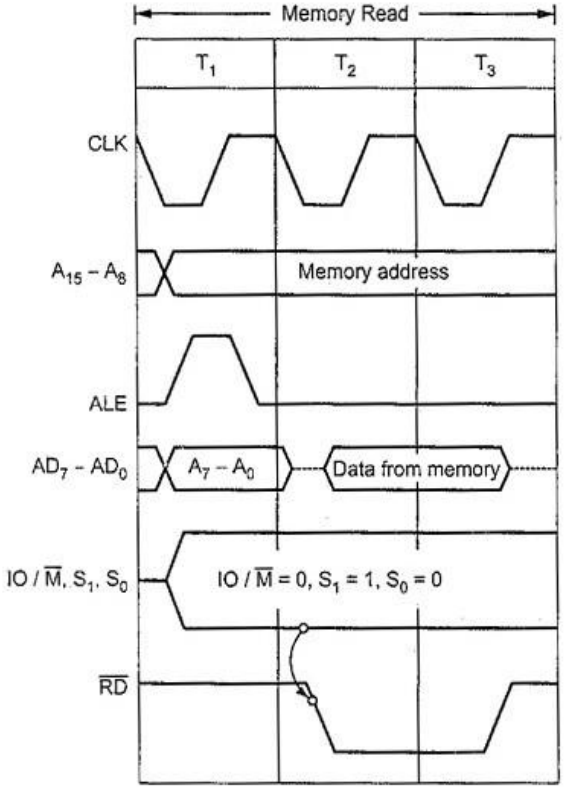


Memory read machine cycle

- Contents from a memory location are read during the memory read machine cycle (MRMC). This cycle is also known as the operand fetch machine cycle. But there are cases when MRMC is not used for operand fetch but for reading data at given memory location. This machine cycle spans over three T states. Each of these T states is explained here along with a timing diagram. The first three T states are almost the same as the first three T states of Opcode Fetch Machine Cycle.

1st T state

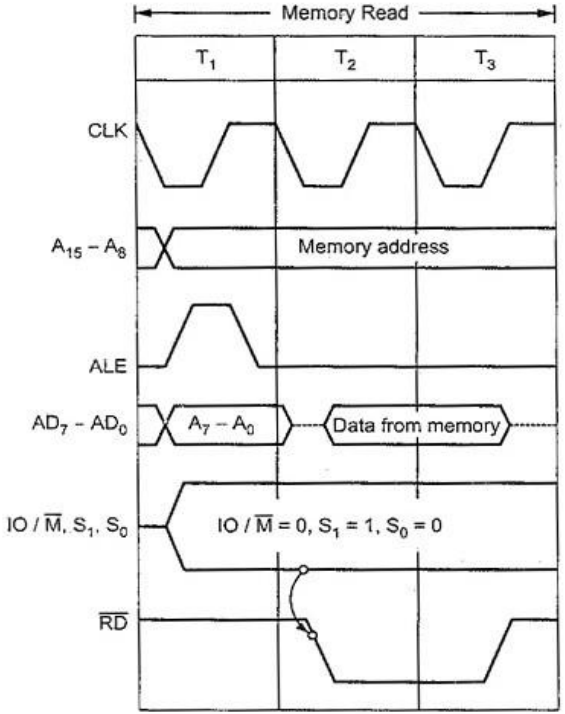
- Higher address bits loaded into A_8-A_{15}.
- Lower address bits loaded into AD_0-AD_7.
- ALE signal goes high in the beginning to indicate that AD_0-AD_7 contains lower address bits.
- IO/$\overline{M}$ goes low since it is a memory operation.
- S_1 and S_0 become 1 and 0 respectively, indicating Memory Read Machine Cycle.
- ALE goes low by the end of the first T state. Lower address bits are expected to be latched by this time.



Memory read machine cycle contd.

2nd and 3rd T states

- $\overline{RD}$ goes low, indicating the initiation of the read operation.
- Data is read from the memory location and is loaded into the data bus AD_0-AD_7. The data is loaded into the data bus at the beginning of the 2nd T state and exists until the end of the third T state.
- By the end of the third T state, $\overline{RD}$ goes high, indicating the end of the read operation.

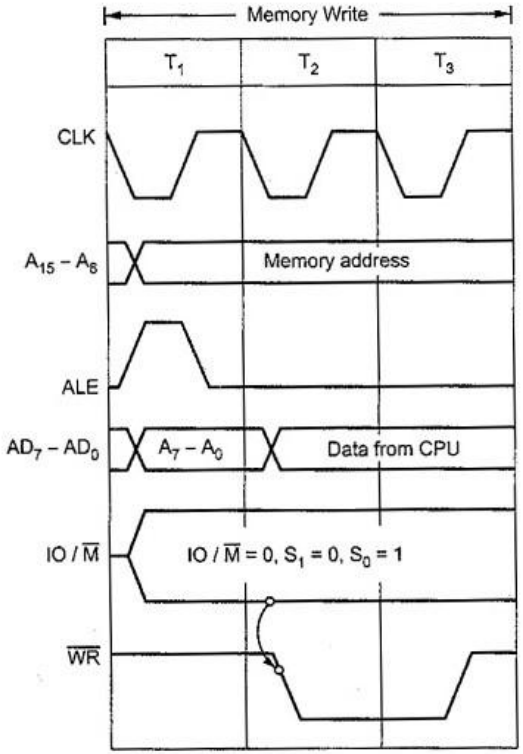


Memory write machine cycle

- Contents are written to a memory location/stack during a memory write machine cycle (MWMC). This machine cycle spans over three T states. Each of these T states are explained here along with the timing diagram.

1st T state

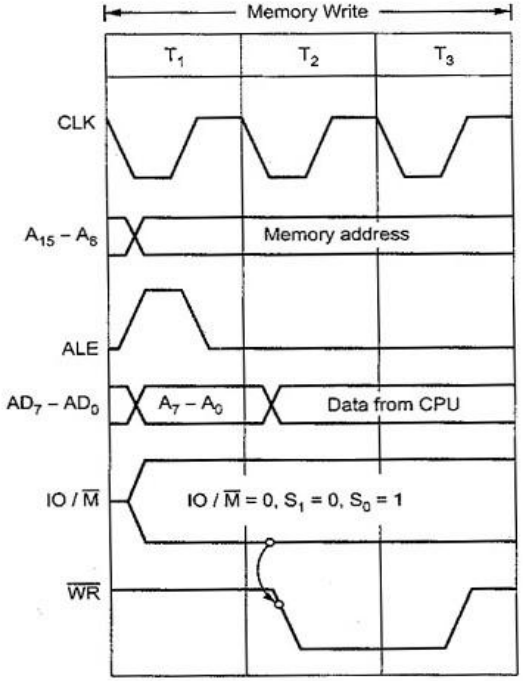
- Higher address bits loaded into A_8-A_{15}.
- Lower address bits loaded into AD_0-AD_7.
- ALE signal goes high in the beginning to indicate that AD_0-AD_7 contains lower address bits.
- IO/$\overline{M}$ goes low since it is a memory operation.
- S_1 and S_0 become 0 and 1 respectively, indicating MWMC.
- ALE goes low by the end of the first T state. Lower address bits are expected to be latched by this time.



Memory write machine cycle contd.

2nd and 3rd T states

- $\overline{WR}$ goes low, indicating the initiation of the write operation.
- Data to be written is loaded on the data bus at the beginning of the second T state and exists until the end of the third T state when the data is transferred from the data bus to the memory location.
- By the end of the third T state, $\overline{WR}$ goes high, indicating the end of the write operation. Thus, MWMC comes to an end.

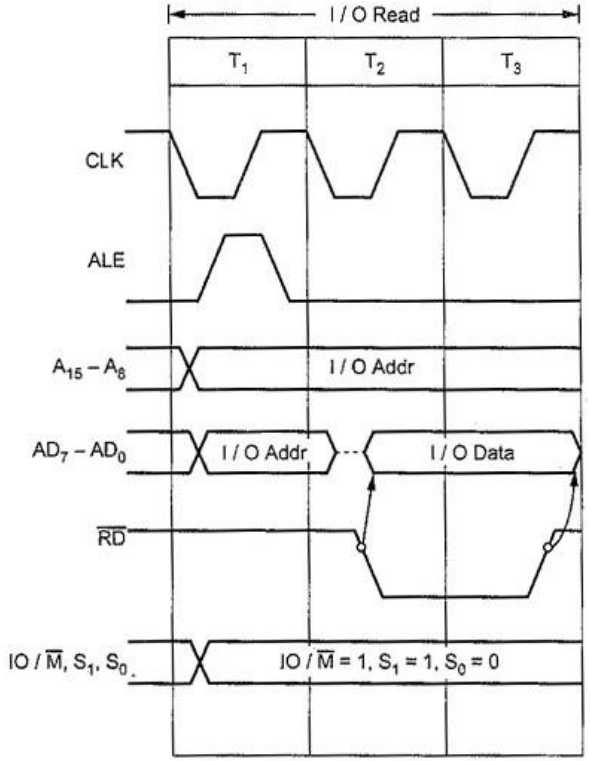


I/O read machine cycle

- Contents from an IO device are read during IO read machine cycle (IORMC). This machine cycle spans three T states and is similar to MRMC except for the IO/ $\overline{M}$ signal. The destination of this read operation is the accumulator. The Program Counter is not incremented here. IO/$\overline{M}$ goes high instead of going low, indicating that the microprocessor is talking to an IO device. Each of these T states are explained here along with a timing diagram.

1st T state

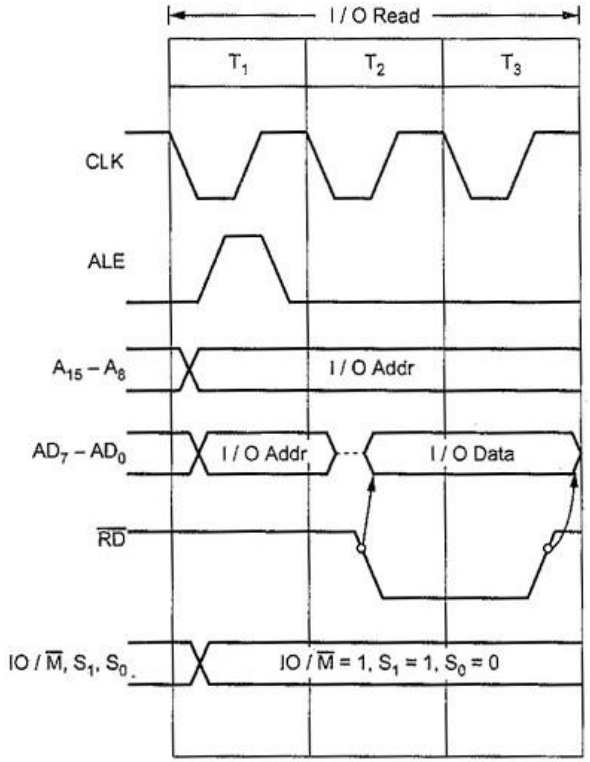
- 8-bit address is loaded into A_8-A_{15}.
- The same 8-bit address is loaded into AD_0-AD_7.
- ALE signal goes high in the beginning to indicate that AD_0-AD_7 contains address bits and not data bits.
- IO/$\overline{M}$ goes high since the microprocessor is dealing with an IO device.
- S_1 and S_0 become 1 and 0 respectively, indicating a 'read' machine cycle.
- ALE goes low by the end of the first T state. Address bits in AD_0-AD_7 are expected to be latched by this time.



I/O read machine cycle contd.

2nd and 3rd T states

- $\overline{RD}$ goes low, indicating the initiation of the read operation.
- Data is read and is loaded on the data bus (AD_0-AD_7) at the beginning of the second T state and exists until the end of the third T state.
- In the third T state, the data is transferred from the data bus to the accumulator.
- By the end of the third T state, $\overline{RD}$ goes high, indicating the end of the read operation.

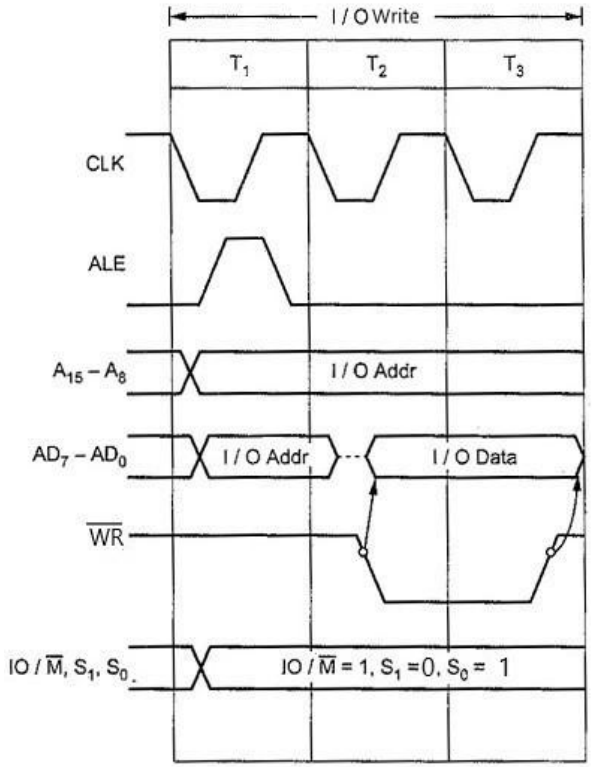


I/O write machine cycle

- Contents are written to an IO device during IO write machine cycle (IOWMC). This machine cycle spans three T states and is similar to MWMC except for the IO/$\overline{M}$ signal. IO/$\overline{M}$ goes high instead of going low, indicating that the microprocessor is talking to an IO device. The contents of the accumulator are transferred to the data bus and written to an output device in this cycle. The T states are explained here along with a timing diagram for your reference.

1st T state

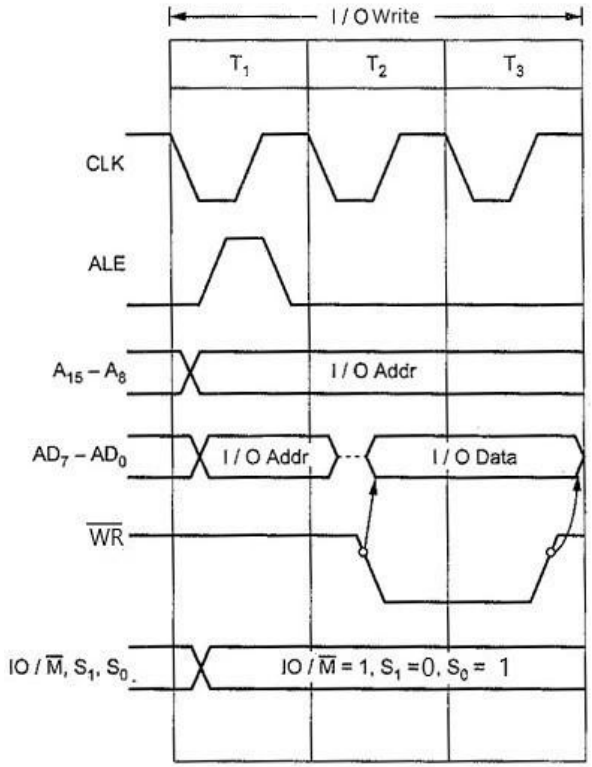
- 8-bit address is loaded into A_8-A_{15}.
- The same 8-bit address is loaded into AD_0-AD_7.
- ALE signal goes high in the beginning to indicate that AD_0-AD_7 contains address bits.
- IO/$\overline{M}$ goes high since the microprocessor is dealing with an IO device.
- S_1 and S_0 become 0 and 1 respectively, indicating a write machine cycle.
- ALE goes low by the end of the first T state. Address bits in AD_0-AD_7 are expected to be latched by this time.



I/O write machine cycle contd.

2nd and 3rd T states

- $\overline{WR}$ goes low, indicating the initiation of the write operation.
- Data to be written is loaded on the data bus at the beginning of the second T state and exists until the end of the third T state.
- In the third T state, the data is transferred from the data bus to the IO device.
- By the end of the third T state, $\overline{WR}$ goes high, indicating the end of the write operation.




Thank you!