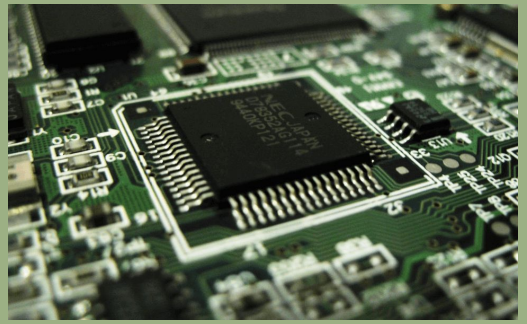


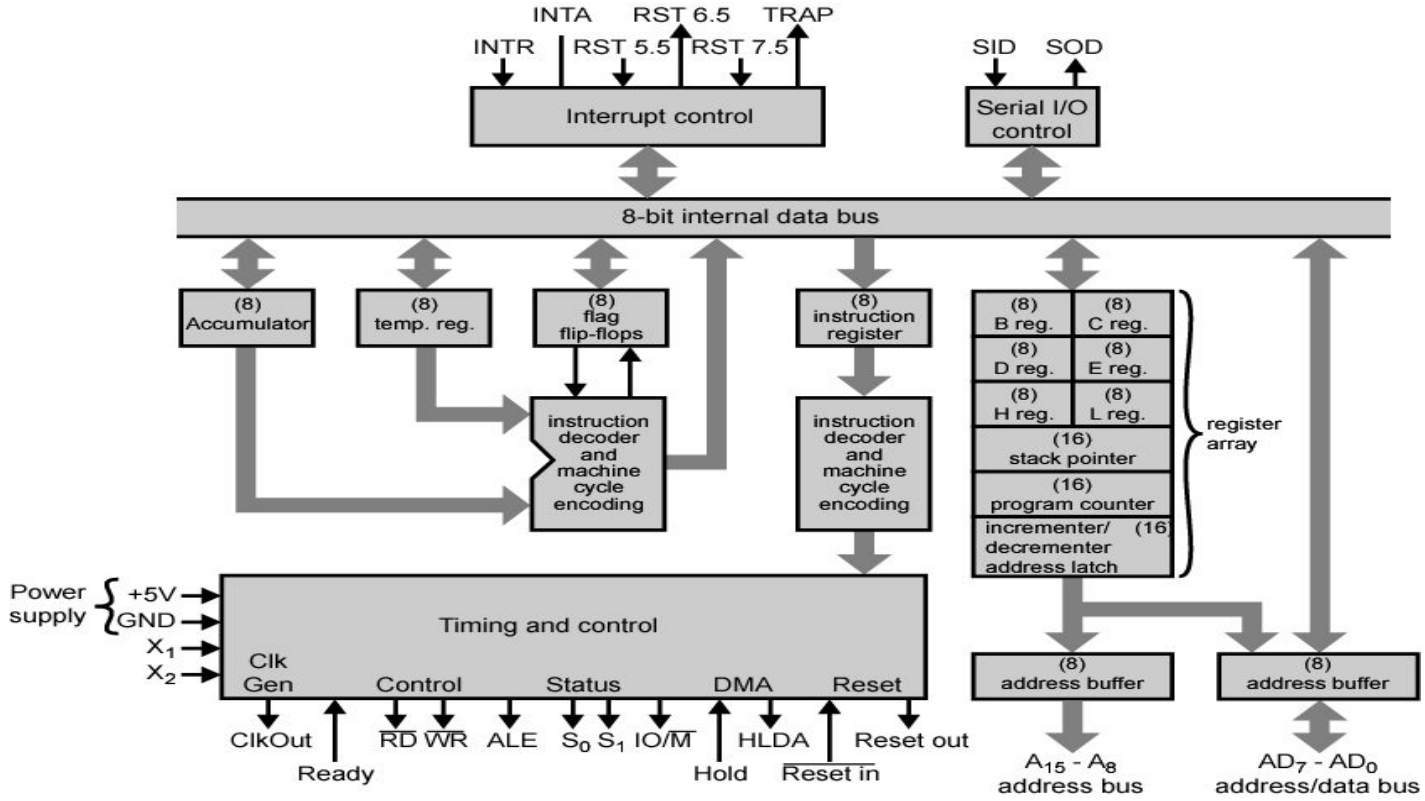
8085 Microprocessor

Dr. Manju Khurana
Assistant Professor, CSED
TIET, Patiala
manju.khurana@thapar.edu

Features of Microprocessor- 8085

- 8085 is developed by INTEL.
- 8 bit microprocessor: can accept 8 bit data simultaneously.
- Operates on single +5V D.C. supply.
- Designed using NMOS technology.
- 6200 transistor on a single chip.
- It provides on chip clock generator, hence it does not require external clock generator.
- Operates on 3MHz clock frequency.
- 8bit multiplexed address/data bus, which reduce the number of pins.
- 16address lines, hence it can address 2^16 = 64 K bytes of memory
- It generates 8 bit I/O addresses, hence it can access 2^8 = 256 I/O ports.
- 5 hardware interrupts i.e. TRAP/RST4.5, RST 7.5, RST 6.5, RST 5.5, and INTR
- It provides DMA (Direct memory access).
- 40-pin I.C. package fabricated on a single LSI chip.
- Clock cycle is 320ns.
- 80 basic instructions and 246 opcodes.

Block Diagram of Intel 8085



Intel 8085 Architecture

8085 architecture consists of following blocks:

1. Register Array
2. ALU & Logical Group
3. Instruction decoder and machine cycle encoder, Timing and control circuitry
4. Interrupt control Group
5. Serial I/O control Group

Intel 8085 Architecture contd.

1. Registers Array :

(a) General purpose register : (user accessible)

- B, C, D, E, H, L are 8 bit register. (can be used singly)
- Can also be used for 16-bit register pairs- BC, DE & HL.
- Used to store the intermediate data and result
- **H & L** can be used as a data pointer (holds memory address)

(b) Special Purpose Register [A, Instruction Register and Flag]

(b.1) Accumulator (A) : (user accessible)

- 8 bit register
- All the ALU operations are performed with reference to the contents of Accumulator.
- Result of an operation is stored in A.
- Store 8 bit data during I/O transfer

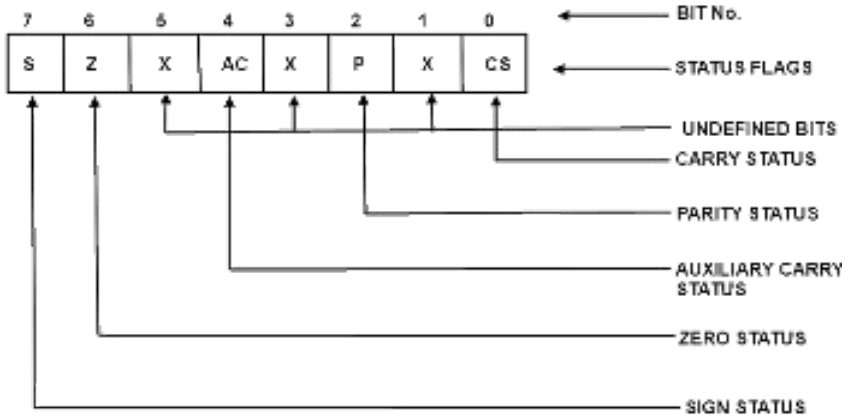
(b.2) Instruction Register: (user not accessible)

- When an instruction is fetched from memory, it is loaded in IR. Then transferred to the decoder for decoding.
- It is not programmable and can not be accessed through any instruction.

Intel 8085 Architecture contd.

(b.3) Flag Register (F) : (user accessible)

- 8 bit Register
- Indicates the status of the ALU operation.
- ALU includes 5 flip flop, which are set or reset after an operation according to data conditions of the result in the accumulator.



Intel 8085 Architecture contd.

Flag	Significance
C or CY (Carry)	CY is set when an arithmetic operation generates a carry out, otherwise it is 0 (reset)
P (Parity)	P= 1; if the result of an ALU operation has an even number of 1's in A; P= 0; if number of 1 is odd.
AC (Auxiliary carry)	Similar to CY, AC= 1 if there is a carry from D_3 to D_4 Bit AC= 0 if there is a no carry from D_3 to D_4 Bit (not available for user)
Z(zero)	Z = 1; if result in A is 00H 0 otherwise
S(Sign)	S=1 if D_7 bit of the A is 1(indicate the result is -ive) S= 0 if D_7 bit of the A is 0(indicate the result is +ive)

Intel 8085 Architecture contd.

(c) Temporary Register [W, Z, Temporary data register]

- Internally used by the MP(user not accessible)

(c.1) W and Z register:

- 8 bit capacity
- Used to hold temporary addresses during the execution of some instructions

(c.2) Temporary data register:

- 8 bit capacity
- Used to hold temporary data during ALU operations.

Intel 8085 Architecture contd.

(d) Pointer Register or special purpose [SP, PC]

(d.1) Stack Pointer (SP)

- 16 bit address which holds the address of the data present at the top of the stack memory
- It is a reserved area of the memory in the RAM to store and retrieve the temporary information.
- Also hold the content of PC when subroutines are used.
- When there is a subroutine call or on an interrupt i.e. pushing the return address on a jump, and retrieving it after the operation is complete to come back to its original location.

(d.2) Program Counter (PC)

- 16 bit address used for the execution of program
- Contain the address of the next instruction to be executed after fetching the instruction
- it is automatically incremented by 1.
- Not much use in programming, but as an indicator to user only.

Intel 8085 Architecture contd.

In addition to register MP contains some latches and buffer

- **Increment and decrement address latch**
  - 16 bit register
  - Used to increment or decrement the content of PC and SP
- **Address buffer**
  - 8 bit unidirectional buffer
  - Used to drive high order address bus(A_8 to A_{15})
  - When it is not used under such as reset, hold and halt etc this buffer is used tri-state high order address bus.
- **Data/Address buffer**
  - 8 bit bi-Directional buffer
  - Used to drive the low order address (A_0 to A_7) and data (D_0 to D_7) bus.
  - Under certain conditions such as reset, hold and halt etc this buffer is used tri-state low order address bus.

Intel 8085 Architecture contd.

(2) ALU & Logical Group: it consists of ALU, Accumulator, Temporary register and Flag Register

(a) ALU

- Performs arithmetic and logical operations
- Stores result of arithmetic and logical operations in accumulator

(b) Accumulator

- General purpose register
- Stores one of the operand before any arithmetic and logical operations and result of operation is again stored back in Accumulator
- Store 8 bit data during I/O transfer

(c) Temporary Register

- 8 bit register
- During the arithmetic and logical operations one operand is available in A and other operand is always transferred to temporary register

For Eg.: ADD B – content of B is transferred into temporary register before actual addition

(d) Flag Register

- Five flags are connected to ALU
- After the ALU operation is performed the status of result will be stored in five flags.

Intel 8085 Architecture contd.

(3) Instruction decoder and machine cycle encoder, Timing and control circuitry

(a) Instruction decoder and machine cycle encoder :

- Decodes the op-code stored in the Instruction Register (IR) and establishes the sequence of events to follow.
- Encodes it and transfer to the timing & control unit to perform the execution of the instruction.

(b) Timing and control circuitry

- works as the brain of the CPU
- For proper sequence and synchronization of all the operations of MP, this unit generates all the timing and control signals necessary for communication between microprocessor and peripherals.

Intel 8085 Architecture contd.

(4) Interrupt Control group

Interrupt:- Occurrence of an external disturbance

- After servicing the interrupt, 8085 resumes its normal working sequence
- Transfer the control to special routines
- Five interrupts: - TRAP, RST7.5, RST6.5, RST5.5, INTR
- In response to INTR, it generates INTA signal

(5) Serial I/O control Group

- Data transfer D_0- D_7 lines is parallel data
- But under some conditions it is used serial data transfer
- Serial data is entered through SID (serial input data) input (received)
- Serial data is outputted on SOD (serial output data) input (send)


Thank you!