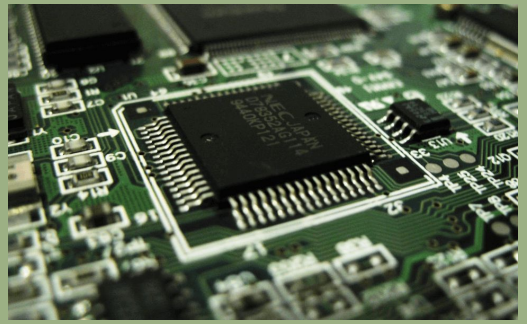
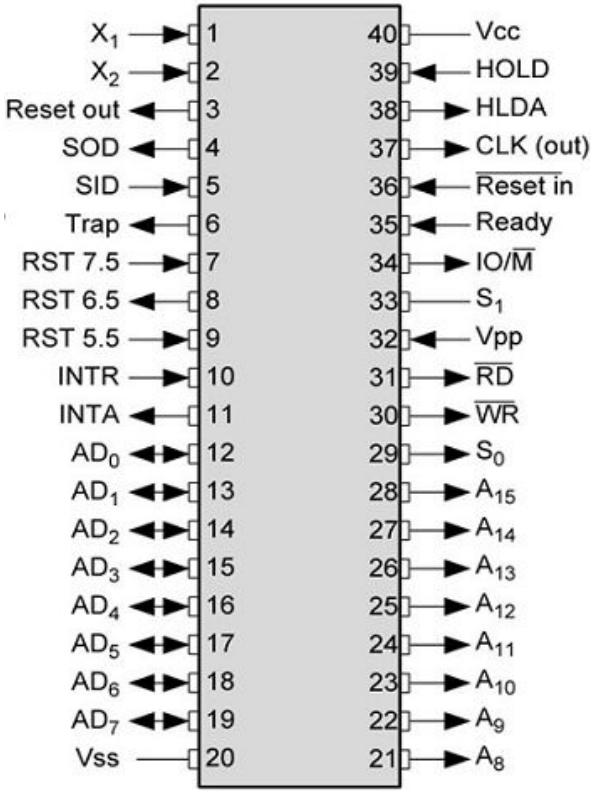


8085 Microprocessor

Dr. Manju Khurana
Assistant Professor, CSED
TIET, Patiala
manju.khurana@thapar.edu

Pin Diagram of Intel 8085

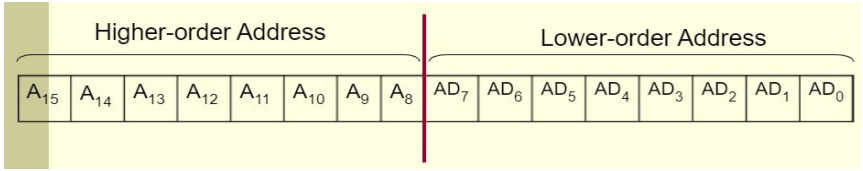


8085 Pin Description

- The 8085 is an 8-bit general purpose microprocessor that can address 64K Byte of memory.
- It has 40 pins and uses +5V for power. It can run at a maximum frequency of 3 MHz.
- The pins on the chip can be grouped into 9 groups:
  - Address Bus and Data Bus
  - Status Signals
  - Control signal
  - Interrupt signal
  - Power supply and Clock signal
  - Reset Signal
  - DMA request Signal
  - Serial I/O signal
  - Externally Initiated Signals.

The Address and Data Busses

- **Address Bus (Pin 21-28)**
  - 16 bit address lines A_0 to A_{15}
  - The address bus has 8 signal lines A_8 – A_{15} which are unidirectional.
  - The other 8 address lines A_0 to A_7 are multiplexed (time shared) with the 8 data bits.



- **Data Bus (Pin 19-12)**
  - To save the number of pins lower order address pin are multiplexed with 8 bit data bus (bidirectional)
  - So, the bits AD_0 – AD_7 are bi-directional and serve as A_0 – A_7 and D_0 – D_7 at the same time.
  - During the execution of the instruction, these lines carry the address bits during the early part (T_1 state), then during the late parts (T_2 state) of the execution, they carry the 8 data bits.

Status Signals

Status Pins – ALE, S_1, S_0

1. **ALE(Address Latch Enable) : (Pin 30)**
   - Used to demultiplexed the address and data bus
   - +ve going pulse generated when a new operation is started by microprocessor.
   - ALE = 1 when the AD_0 – AD_7 lines have an address
   - ALE = 0 When it is low it indicates that the contents are data.
   - This signal can be used to enable a latch to save the address bits from the AD lines.
2. **S_1 and S_0 (Status Signal) : (Pin 33 and 29)**
   - Status signals to specify the kind of operation being performed .
   - Usually un-used in small systems.

S_1	S_0	Operation
0	0	HALT
0	1	WRITE
1	0	READ
1	1	FETCH

Control Signals

Control Pins – RD, WR, IO/M (active low)

1. **RD: Read (Active low) (Pin 32)**
   - Read Memory or I/O device
   - Indicated that data is to be read either from memory or I/P device and data bus is ready for accepting data from the memory or I/O device.
2. **WR: Write (Active low) (Pin 31)**
   - Write Memory or I/O device
   - Indicated that data on the data bus are to be written into selected memory or I/P device.
3. **IO/M: (Input Output/Memory-Active low) (Pin 34)**
   - Signal specifies that the read/write operation relates to whether memory or I/O device.
   - When (IO/M=1) the address on the address bus is for I/O device
   - When (IO/M=0) the address on the address bus is for memory

IO/M(active low)	RD	WR	Control Signal	Operation
0	0	1	MEMR	M/M Read
0	1	0	MEMW	M/M write
1	0	1	IOR	I/O Read
1	1	0	IOW	I/O Write

Control and status Signals

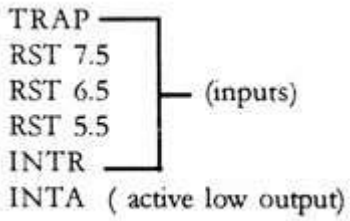
- When S_0, S_1 is combined with IO/M (active low), we get status of machine cycle

IO/M	S1	So	OPERATION	Control Signal
0	1	1	Opcode fetch	$\overline{RD}$ = 0
0	1	0	Memory read	$\overline{RD}$= 0
0	0	1	Memory write	$\overline{WR}$ = 0
1	1	0	I/O read	$\overline{RD}$ = 0
1	0	1	I/O write	$\overline{WR}$ = 0
1	1	0	Interrupt Acknowledge	$\overline{INTA}$ = 0
Z	0	0	Halt	$\overline{RD}$, $\overline{WR}$ = Z and $\overline{INTA}$ =1
Z	x	x	Hold	
Z	x	x	Reset	

Z= Tristate, X = don't care condition

Interrupts

- They are the signals initiated by an external device to request the microprocessor to do a particular task or work.
- There are five hardware interrupts called, **(Pin 6-11)**
- On receipt of an interrupt, the microprocessor acknowledges the interrupt by the active low INTA (Interrupt Acknowledge) signal.



Power supply and Clock Signal

- Vcc **(Pin 40) : single +5 volt power supply**
- Vss **(Pin 20) : Ground**

- ✔ **X_0 and X_1 : (Pin 1-2)**
  - Crystal or R/C network or LC network connections to set the frequency of internal clock generator.
  - The frequency is internally divided by two.
  - Since the basic operating timing frequency is 3 MHz, a 6 MHz crystal is connected to the X_0 and X_1 pins.
- ✔ **CLK (output) : (Pin 37)**
  - Clock Output is used as the system clock for peripheral and devices interfaced with the microprocessor.

Reset Signals

- **Reset In (input, active low) (Pin 36)**
  - This signal is used to reset the microprocessor.
  - The program counter inside the microprocessor is set to zero (0000H)
  - The buses are tri-stated.

- **Reset Out (Output, Active High) (Pin 3)**
  - It indicates microprocessor is being reset.
  - Used to reset all the connected devices when the microprocessor is reset.

DMA Request Signals

- **DMA:**
  - When 2 or more devices are connected to a common bus, to prevent the devices from interfering with each other, the tristate gates are used to disconnect all devices except the one that is communicating at a given instant .
  - The CPU controls the data transfer operation between memory and I/O device.
  - DMA operation is used for large volume data transfer between memory and an I/O device directly.
  - The CPU is disabled by tri-stating its buses and the transfer is effected directly by external control circuits.
- **HOLD (Pin 38)**
  - This signal indicates that another device is requesting the use of address and data bus.
  - So it relinquish the use of buses as soon as the current machine cycle is completed.
  - Microprocessor regains the bus after the removal of a HOLD signal
- **HLDA (Pin 39)**
  - On receipt of HOLD signal, the MP acknowledges the request by sending out HLDA signal and leaves out the control of the buses.
  - After the HLDA signal the DMA controller starts the direct transfer of data.
  - After the removal of HOLD request HLDA goes low.

Serial I/O Signals

These pins are used for serial data communication

- **SID (input) Serial input data (Pin 4)**
  - It is a data line for serial input
  - Used to accept serial data bit by bit from external device
  - The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

- **SOD (output) Serial output data (Pin 5)**
  - It is a data line for serial output
  - Used to transmit serial data bit by bit to the external device
  - The 7th bit of the accumulator is outputted on SOD line when SIM instruction is executed.

Externally Initiated signal

- **Ready (input) (Pin 35)**
  - Memory and I/O devices will have slower response compared to microprocessors.
  - Before completing the present job such a slow peripheral may not be able to handle further data or control signals from CPU.
  - The processor sets the READY signal after completing the present job to access the data.
  - It synchronize slower peripheral to the processor.
  - The microprocessor enters into WAIT state while the READY pin is disabled.


Thank you!