8259 PIC

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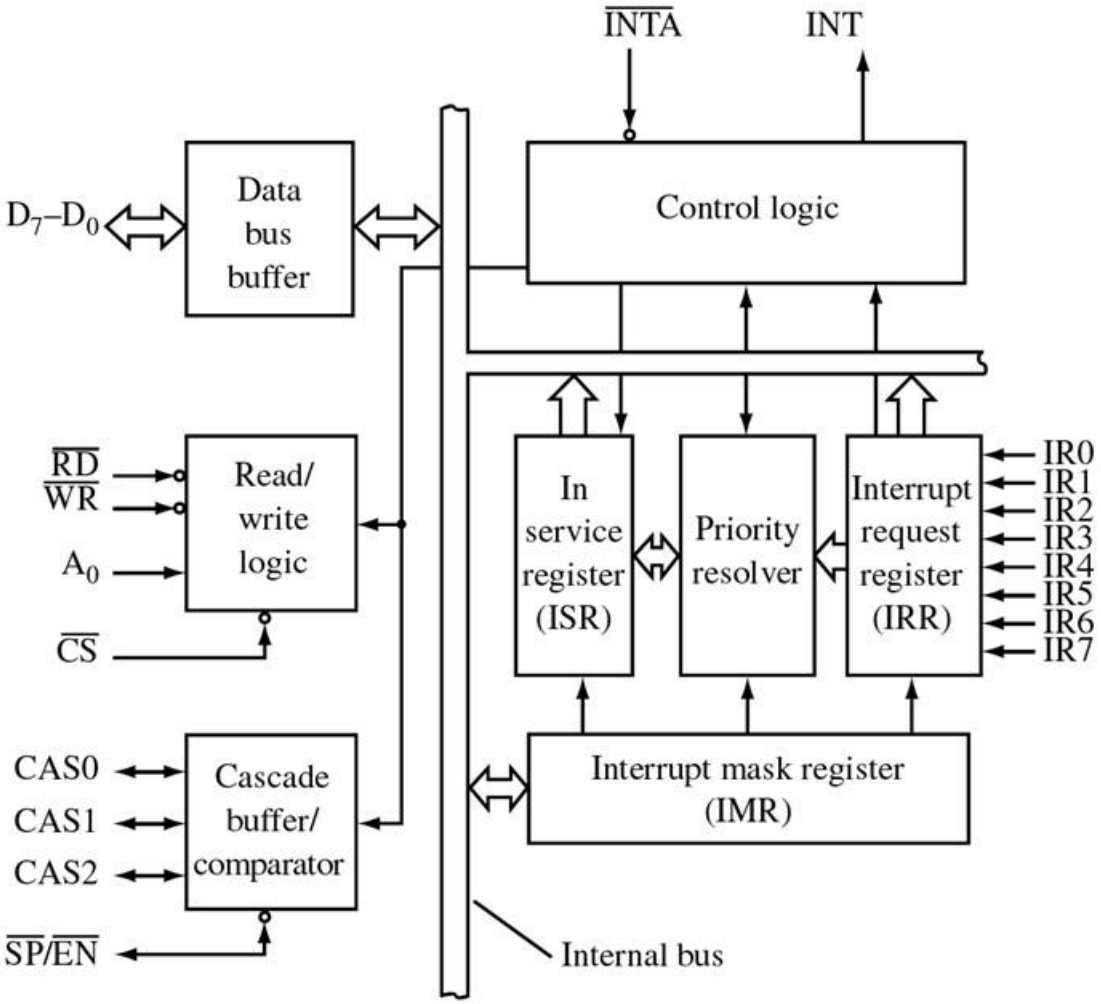
8259 Special Features

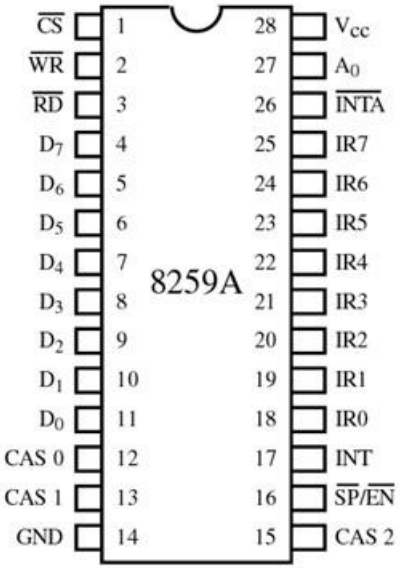
- 8259 PIC is a LSI chip which manages 8 levels of priority interrupts, i.e. it is used to implement 8 levels interrupt system.
- It can be cascaded in a master-slave configuration to implement 64 levels of interrupts.
- It can identify the interrupting device.
- It can resolve the priority of interrupts i.e. it does not require any external priority resolver.
- It can be operated in various priority modes such as fixed priority and rotating priority modes.
- The interrupt requests are individually maskable.

8259 Special Features

- The operating modes and masks may be dynamically changed by the software at any time during execution of the program.
- The 8259 can accepts requests from the peripheral, determines priority of incoming request, checks whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt signal to the microprocessor.
- It can be monitored in buffered mode which can be used for the large system.
- The starting address called vector number is programmable.
- The 8259 is static, does not require clock signal.

8259A Block Diagram





Data Bus Buffer

- This 3-state, bidirectional 8-bit buffer is used to interface the 8259A to the system Data Bus.
- **Control words and status information** are transferred through the Data Bus Buffer.

Read-Write Control Logic

- The function of this block is to accept OUTput commands from the CPU.
- It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the **various control formats** for device operation.
- This function block also allows the status of the 8259A to be transferred onto the Data Bus.

Control Logic

- This block has two pins: INT (Interrupt) as an output, and INTA (Interrupt Acknowledge) as an input.
- The INT is connected to the interrupt pin of the microprocessor. Whenever a valid interrupt is asserted, this signal goes high.
- The INTA is the interrupt acknowledgement signal from the microprocessor.

IRR and ISR

- INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)
- The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service (ISR).
- The IRR is used to store all the interrupt levels which are requesting service;
- The ISR is used to store all the interrupt levels which are being serviced.

Priority Resolver

- This logic block determines the priorities of the bits set in the IRR.
- The highest priority is selected and strobed into the corresponding bit of the ISR during INTA pulse.

Interrupt Mask Register

- The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR.
- Masking of a higher priority input will not affect the interrupt request lines of lower quality.

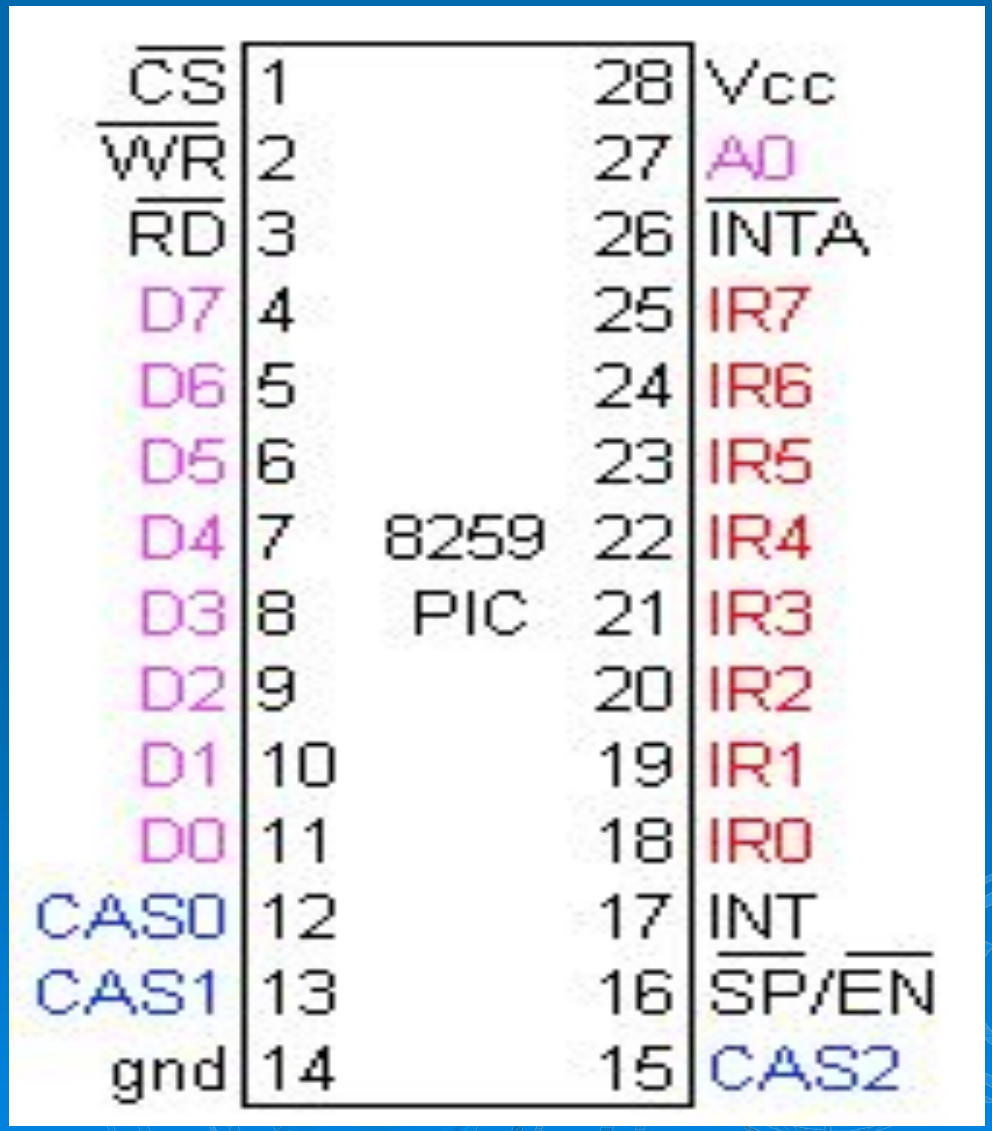
The Cascade Buffer/Comparator

- This function block stores and compares the IDs of all 8259A's used in the system. The associated three I/O pins (CAS0-2) are outputs when the 8259A is used as a master and are inputs when the 8259A is used as a slave.

- As a master, the 8259A sends the ID of the interrupting slave device onto the CAS 0-2 lines.

- The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive INTA pulses.

8259 Pin Connections



Chip Select ($\overline{CS}$)

- A LOW on this input enables the 8259A. No reading or writing of the chip will occur unless the device is selected

A_0

- This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines

$\overline{RD}$ & $\overline{WR}$

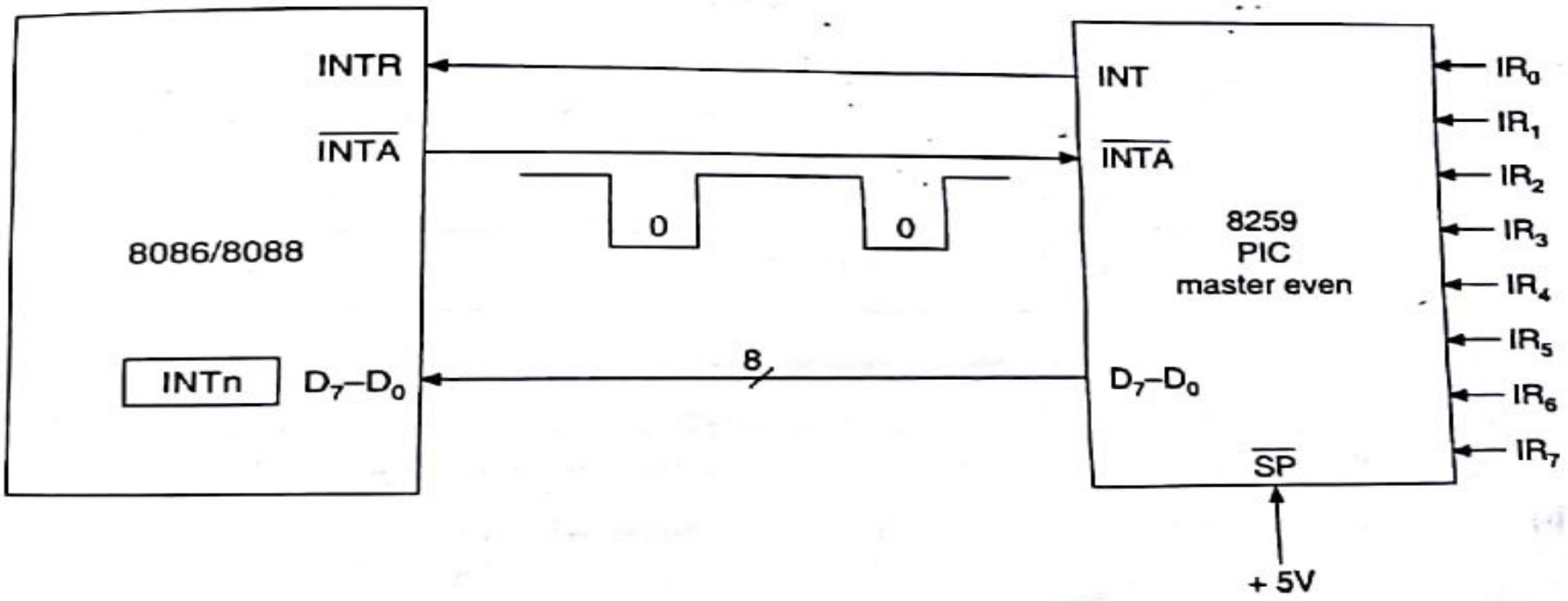
- A LOW on $\overline{WR}$ input enables the CPU to write control words (ICWs and OCWs) to the 8259A.
- A LOW on $\overline{RD}$ input enables the 8259A to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR), or the Interrupt level onto the Data Bus.

$\overline{SP}/\overline{EN}$: Slave program/enable buffer

- This is a dual function pin.
- When in non buffered mode, it is used to designate a master 8259PIC($\overline{SP}$=1) or slave 8259PIC($\overline{SP}$=0), i.e. $\overline{SP}$ pin of master 8259 is connected to Vcc,
- while $\overline{SP}$ pin of slave 8259 is grounded.
- In buffered mode, it can be used as an output to control buffer transceivers (EN).

Sequence of Operation of 8259 PIC with MP 8086/8088

- Powerful feature of 8259A is its :
  # programmability
  # interrupt routine addressing capability(IRAC).
- IRAC allows direct or indirect jumping to specific Interrupt routine



Sequence of operation of 8259 PIC with microprocessor 8086/8088.

Sequence of Operation of 8259 PIC with MP 8086/8088: Event sequence occurring in 8086 system is given below:-

1. One or more of the Interrupt request lines(IR0-IR7) are raised high, setting corresponding IRR bits.

2. 8259A resolves the priority of these requests, and sends an INT signal to MP.

3. The MP ack the INT and responds with INTA pulse.

4. Upon receiving an INTA from MP, highest priority ISR bit is set and corresponding IRR bit is reset. 8259 does not drive the data bus during this cycle.

5. 8086 will initiate a second INTA pulse in which 8259 releases an

Sequence of Operation of 8259 PIC with MP 8086/8088: Event sequence occurring in 8086 system is given below:-

6. This completes interrupt cycle. In the AEOI(automatic end of interrupt) mode, ISR bit is reset at the end of second INTA pulse.
   Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.


Thank you!