Programmable Interval Timer 8253 / 8254

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WHY 8253 / 8254???

Not Possible To Generate Accurate Time Delays Using Delay Routines in 8086

Intel's Programmable Counter/ Timer Device (8253/8254) Facilitates

- **Accurate Time Delays**
- **Minimizes Load On Mp**
- **Real Time Clock**
- **Event Counter**
- **Digital One Shot**
- **Square Wave Generator**
- **Complex Waveform Generator**

8253 vs 8254

8253

- 8253 can operate at frequency up to 2mhz

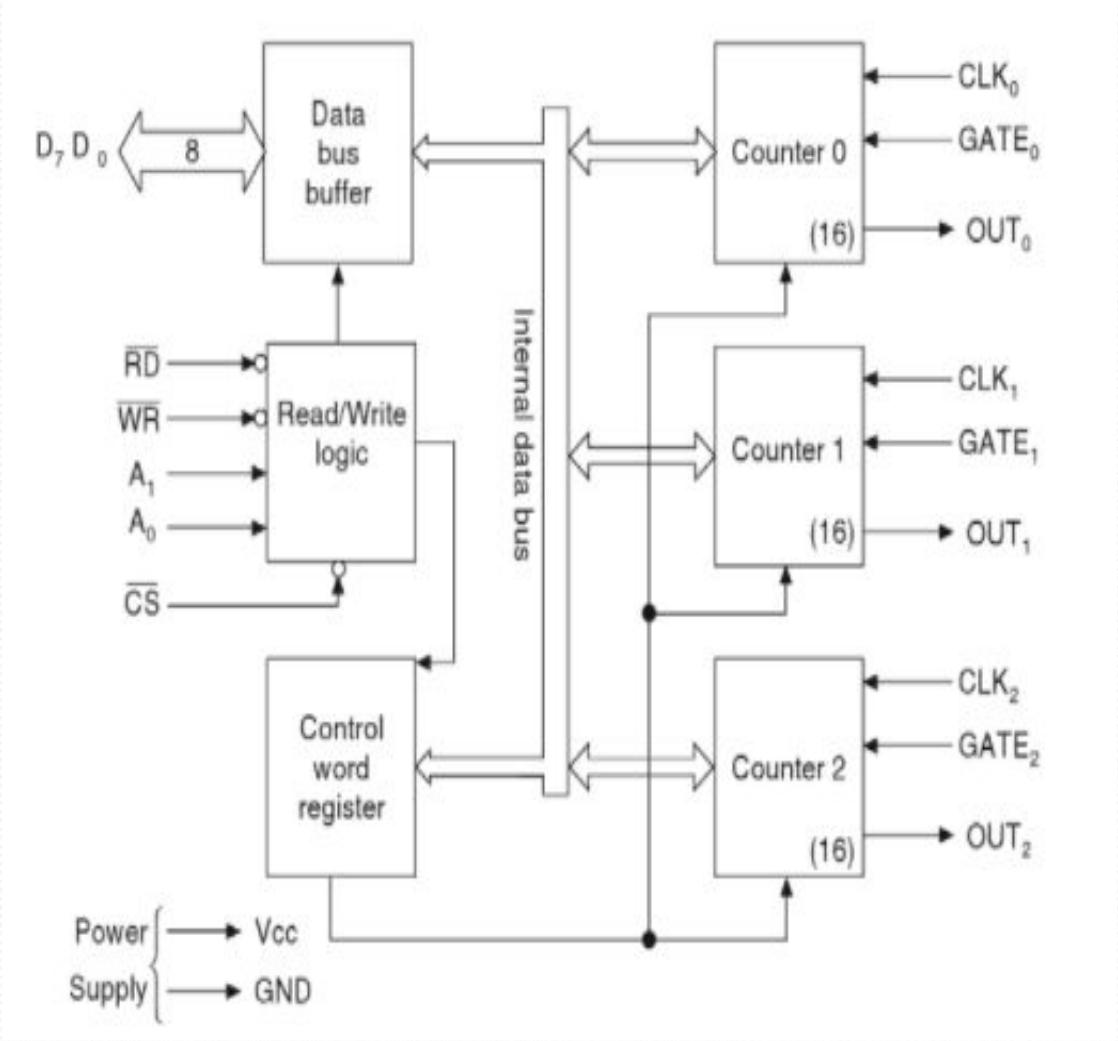
8254-ADVANCED VERSION OF 8253

- 8254 can operate with higher clock Frequency Range (up to 8 Mhz AND 10 Mhz FOR 8254-2)

Features of 8253

- High speed and low power consumption is achieved through silicon gate CMOS technology.
- Completely static operation.
- Three independent 16-bit down counters.
- Operates on 3V to 6V single power supply.
- Six counter modes available for each of the three counters.
- Binary and decimal counting is possible.
- For 8253 DC to 2.6 MHz operating frequency range and for 8254 DC to 8 MHz operating frequency range.
- 24-pin dual in line package.
- 8253 PIT is a programmable interval timer/counter specifically designed for use with the Intel microcomputer system.

Functional Block Diagram of 8253 PIT



1. Data Bus Buffer

The three-state, bidirectional, 8-bit data bus is used to interface the 8253 PIT data bus to the system data bus. It is internally connected to the data bus and its outer pins D_7–D_0 are connected to the system data bus directly. The directions of data buffer are decided by read and write control signals. When read signal is activated, then it transmits data to the system. When write signal is activated, then it receives data from the system data bus. This reading and writing operation is achieved by IN and OUT microprocessor instructions.

The data bus buffer has three basic functions:

(a) Programming the modes of the 8253 PIT.
(b) Loading the count registers.
(c) Reading the count values.

2. Read/Write Logic

This block accepts inputs from system control bus and address bus. The control signals are $\overline{RD}$ and $\overline{WR}$, and address signals used are A_1, A_0 and $\overline{CS}$. From these five signals $\overline{RD}$ and $\overline{WR}$ are connected to $\overline{IOR}$, $\overline{IOW}$, or $\overline{MEMR}$, $\overline{MEMW}$ depending on the type of mapping used. $\overline{RD}$ and $\overline{WR}$ decide the operation is to be performed, i.e. write data to the 8255 PPI or read data from the 8255PPI. A_1 and A_0 are directly connected to address lines A_1 and A_0 of system address lines. The $\overline{CS}$ is connected to the chip select decoder; the selection of 8255 is enabled or disabled by $\overline{CS}$ signal. If logic 0 is applied on this signal, the 8255 PPI is selected or when 1 is applied on this signal, the 8255 PPI is rejected. The address bits A_1 and A_0 select or activate the corresponding port and control word register.

3. Control Word Register

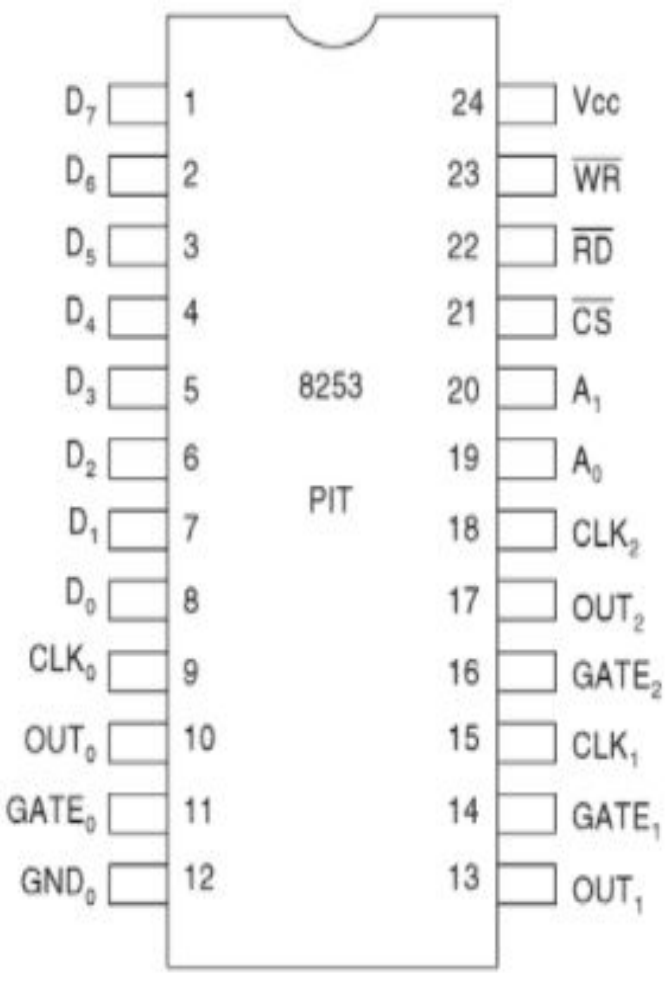
The control word register is selected when A_1 A_0 = 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operation mode of each counter, selection of binary or BCD counting, and the loading of each count register. The data can only be written into control word register, no read operation is allowed.

4. Counters 0, 1 and 2

The three independent 16-bit down counters can be programmed separately through the control word register to decide mode of the counter. Each counter consists of a single, 16-bit, presettable, down counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of the modes specified by the control word register. Also, there are special features in the control word that handle the loading of the count values so that the software overhead can be minimized for these functions. The value of the loaded counter will be decremented by counter at each clock input pulse and hence it is a down counter.

The reading of the contents of each counter is available to the programmer with simple READ operation for event counting applications and special commands and logic are included in the 8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

Pin configuration of 8253 PIT



1. $D_7 - D_0$

Data bus
Pins: 1 to 8
Type: Input/Output
These are the 8-bit bidirectional data bus lines carry data or control word to/from microprocessor.

2. $\overline{CS}$

Chip select
Pin: 21
Type: Input
This is an active low input signal used to select the 8255. If $\overline{CS}$ is 0, then it enables the communication between the 8253 PIT and the microprocessor.

3. $\overline{RD}$

Read
Pin: 22
Type: Input
This is an active low signal. A low on this input enables the 8253 PIT to send the data or status information to the microprocessor on the data bus. Alternately low on this signals means it allows microprocessor to read from the 8253 PIT.

4. $\overline{WR}$

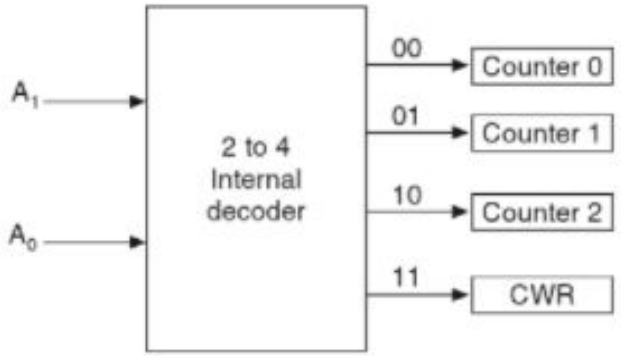
Write
Pin: 23
Type: Input

This is an active low signal. A low on this pin enables the microprocessor to write data or control words into the 8253 PIT.

5. A_1 and A_0

Address lines
Pins: 20 and 19
Type: Input

A concerned signal on these input lines allows selecting counter 0, counter 1, counter 2, and the control word register. These address lines are internally decoded to generate one of the ports and control word registers as shown below:



A_1	A_0	Selects
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control word register (CWR)

Also this address lines along with $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ form the following operation for the 8253:

$\overline{RD}$	$\overline{WR}$	A_1	A_0	$\overline{CS}$	*Input operation (Read)*
0	1	0	0	0	Read counter 0
0	1	0	1	0	Read counter 1
0	1	1	0	0	Read counter 2
0	1	1	1	0	No operation 3 state
1	0	0	0	0	Load counter 0
1	0	0	1	0	Load counter 1
1	0	1	0	0	Load counter 2
1	0	1	1	0	Write control word
X	X	X	X	1	Disable 3 state
1	1	X	X	0	No operation 3 state

6. CLK_0, CLK_1 and CLK_2

Clock input
Pins: 9, 15 and 18
Type: Input
These lines are clock input to the three independent counters, counter 0, counter 1 and counter 2. The pulses applied at these pins will be counted by respective counters.

7. OUT_0, OUT_1 and OUT_2

Output
Pins: 10, 13 and 17
Type: Output
These lines are active high output lines, used to give output of counters. The output will be dependent on mode selected, such as logic 0, logic 1, or frequency output.

8. $GATE_0$, $GATE_1$ and $GATE_2$

Gate control
Pins: 11, 14 and 16
Type: Input

These are active high input signals used to allow external hardware to control the respective counter. It is having different functions in different operating modes. The basic function of GATE is to start and stop the counter. If the signals on these inputs are high, then counter is counting pulses and if it is low, then counter will stop counting.


Thank you!