8086 Microprocessor

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Features of 8086 microprocessor

- It is a 16-bit, N-channel, HMOS (High speed metal oxide semiconductor) microprocessor.
- Its CMOS (Complementary MOS) version, 80C86 is also available.
- It consumes less power.
- The 8086 draws 360 mA on 5V whereas the 80C86 draws only 10 mA.
- 8086 is manufactured for standard temperature range 32 F to 180 F as well as extended temperature range (40 F to +225 F).
- Its clock frequencies for its different versions are: 5, 8 and 10 MHz.
- It was introduced in 1978.

Features of 8086 microprocessor

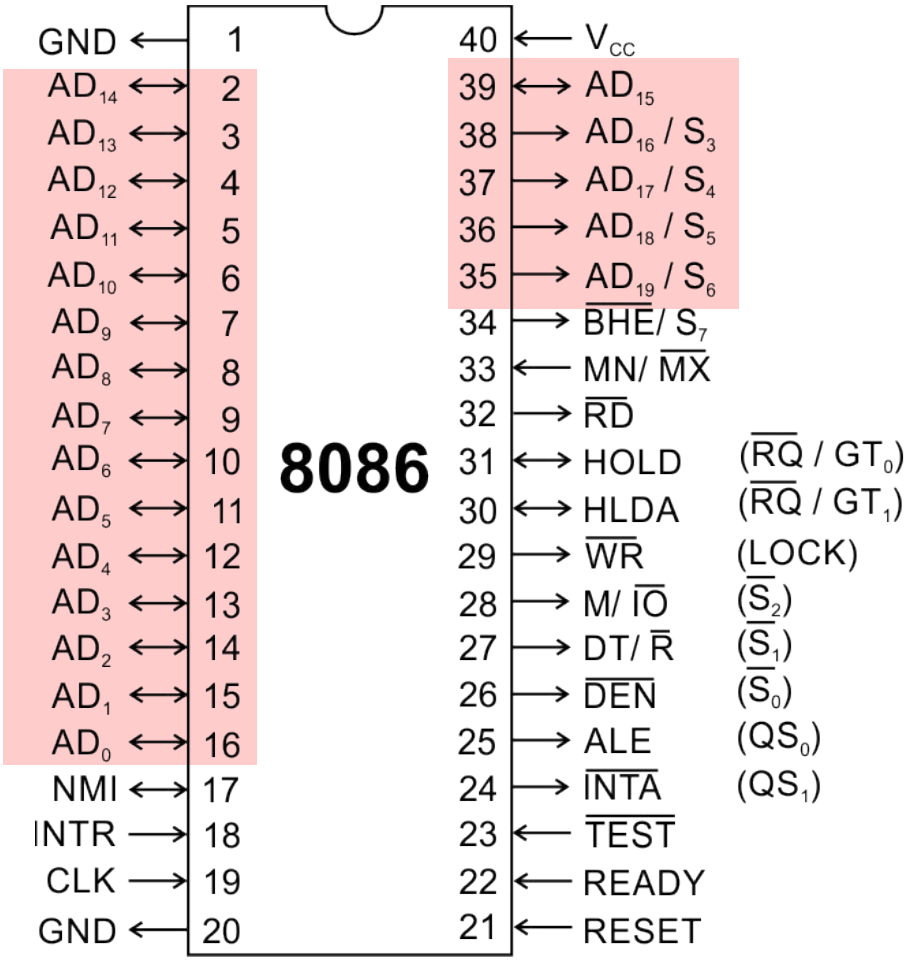
- It contains an electronic circuitry of 29000 transistors.
- It is built on a single semiconductor chip and packaged on a 40-Pin IC package.
- The type of package is DIP (Dual In-Line Package).
- 8086 uses 20 address lines and 16 data lines.
- It can directly address up to 2^20=1Mbytes of memory.
- The 16-bit data word is divided into a low-order byte and a high order byte.
- The 16 low order address lines are time multiplexed with data, and the 4 high order address lines are time multiplexed with status signals.

Pin Diagram of Intel 8086 Microprocessor

Mistake:- Pin 35 to 38 is A_{16}-A_{19} instead of AD_{16}-AD_{19}.

Pins and Signals

Common signals



AD_0-AD_{15} (Bidirectional)

Address/Data bus

Low order address bus; these are multiplexed with data.

When AD lines are used to transmit memory address the symbol A is used instead of AD, for example A_0-A_{15}.

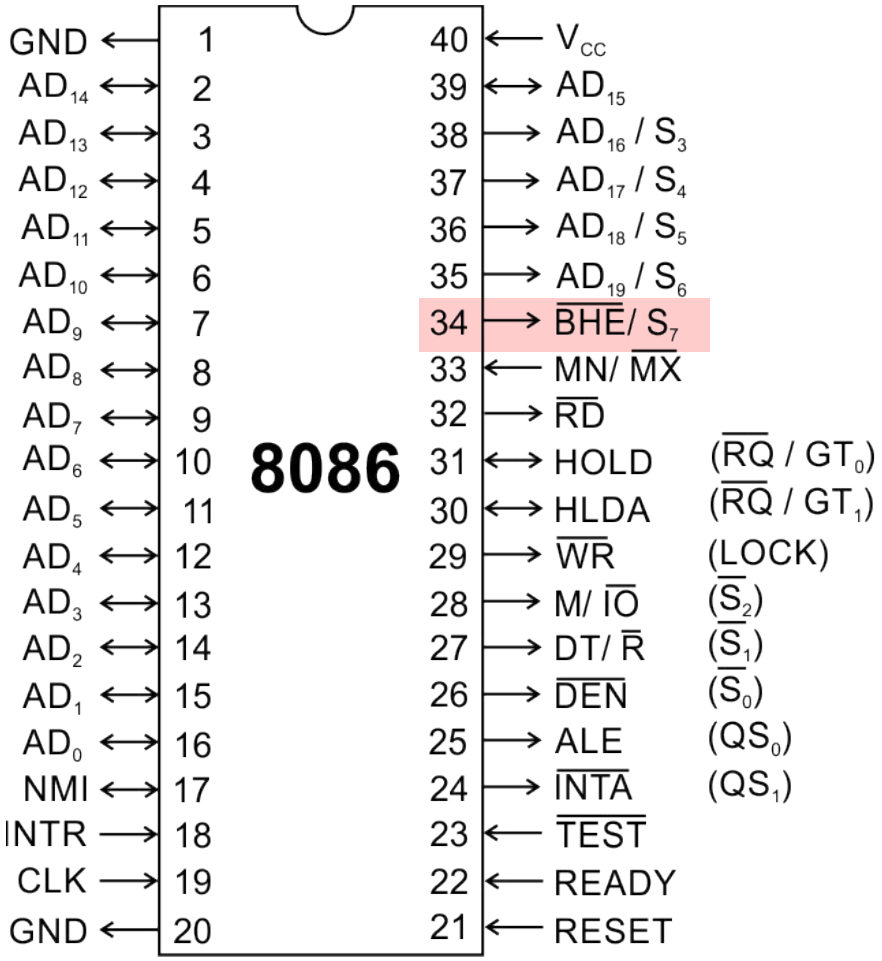
When data are transmitted over AD lines the symbol D is used in place of AD, for example D_0-D_7, D_8-D_{15} or D_0-D_{15}.

A_{16}/S_3, A_{17}/S_4, A_{18}/S_5, A_{19}/S_6

High order address bus. These are multiplexed with status signals.
A_{16} and A_{17} are multiplexed with segment identifier signals S3 and S4.
A_{18} multiplexed with interrupt status S5.
A_{19} with status signal S6.

Pins and Signals

Common signals



BHE (Active Low)/S_7 (Output)

Bus High Enable/Status

(T1 is low)It is used to enable data onto the most significant half of data bus, D_8-D_{15}. 8-bit device connected to upper half of the data bus use BHE (Active Low) signal. It is multiplexed with status signal S_7.(S_7 available during T3 and T4.)

MN/ MX

MINIMUM / MAXIMUM

This pin signal indicates what mode the processor is to operate in.

Pins and Signals

BHE(low)	A0	
0	0	Whole word is transferred
0	1	Upper byte from/to odd address
1	0	Lower byte from/to even address
1	1	None

S_3, S_4, S_5

S3 and S4 identify the memory Segment which is being accessed.

S5 is Interrupt enable status.

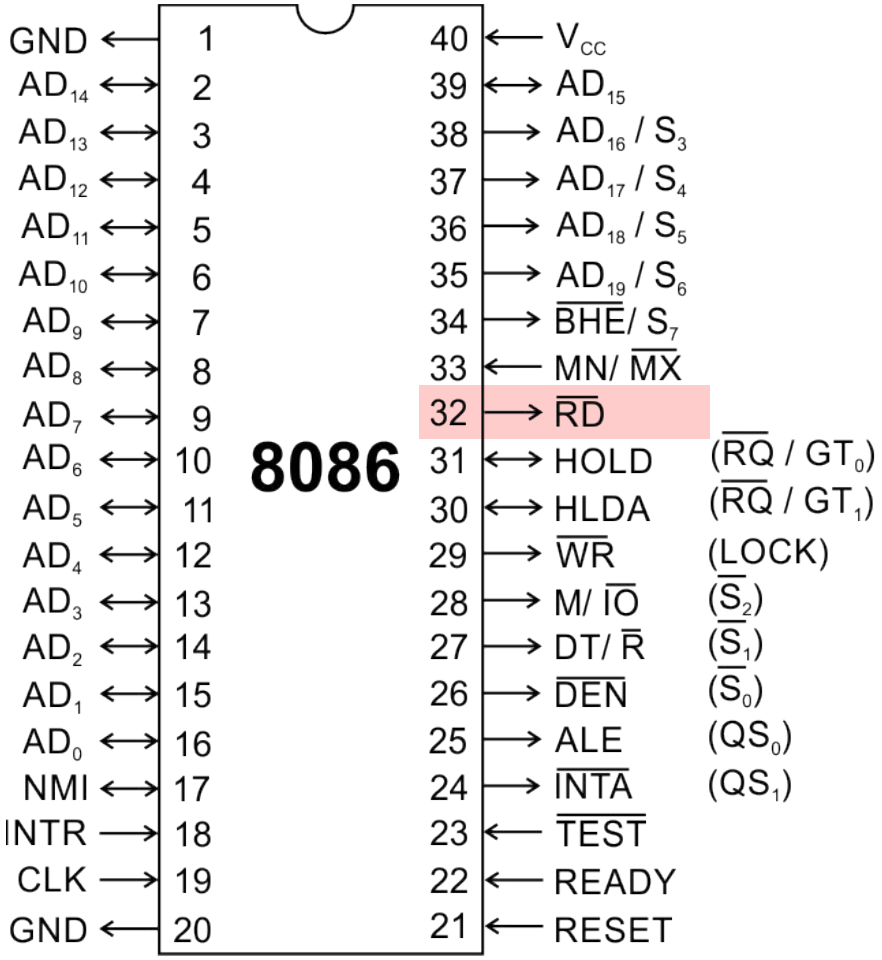
For memory access, S_6 is always zero.

Pins and Signals

S3	S4	
0	0	ES
0	1	SS
1	0	CS
1	1	DS

Pins and Signals

Common signals



TEST

TEST: input is examined by the ``Wait'' instruction. If the TEST input is LOW execution continues, otherwise the processor waits in an ``Idle'' state. This input is synchronized internally during each clock cycle on the leading edge of CLK.

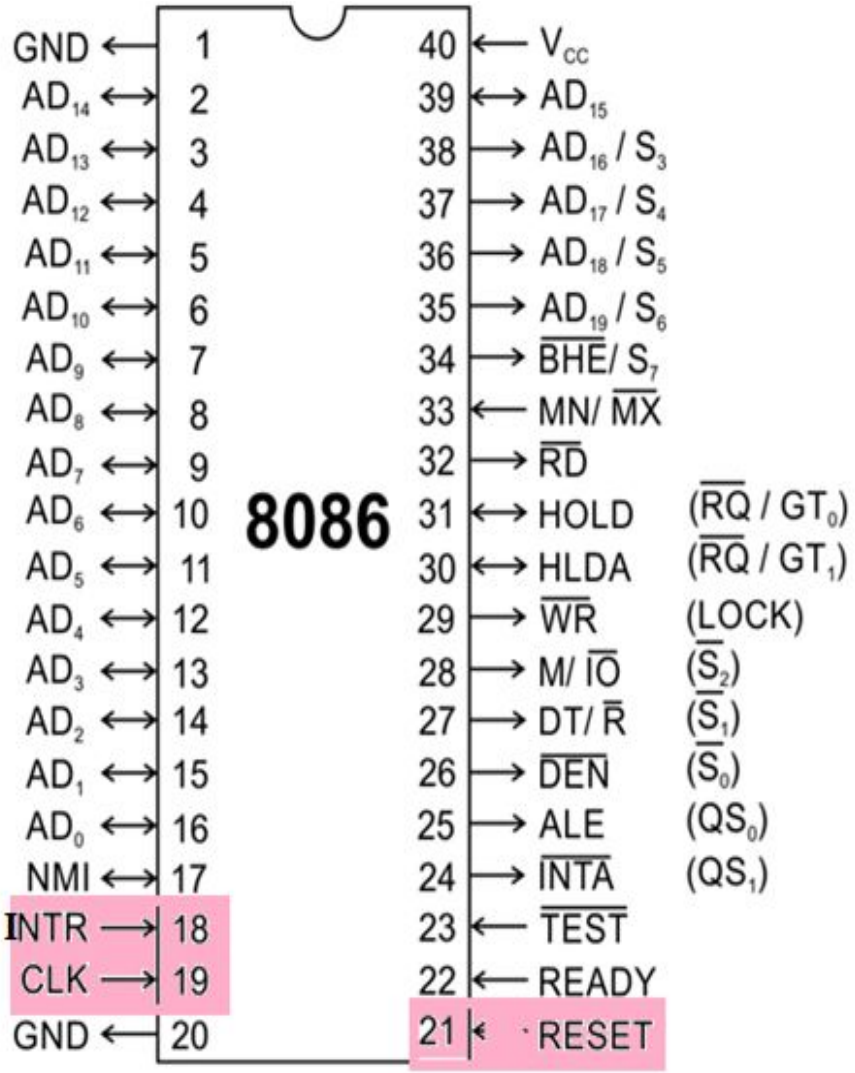
used to synchronize an external activity to the processor internal operation.

RD (Read) (Active Low)

The signal is used for read operation.
It is an output signal.
It is active when low.

Pins and Signals

Common signals



RESET (Input)

Causes the processor to immediately terminate its present activity.

The signal must be active HIGH for at least four clock cycles.

CLK

The clock input provides the basic timing for processor operation and bus control activity.
5,8 or 10 MHz.

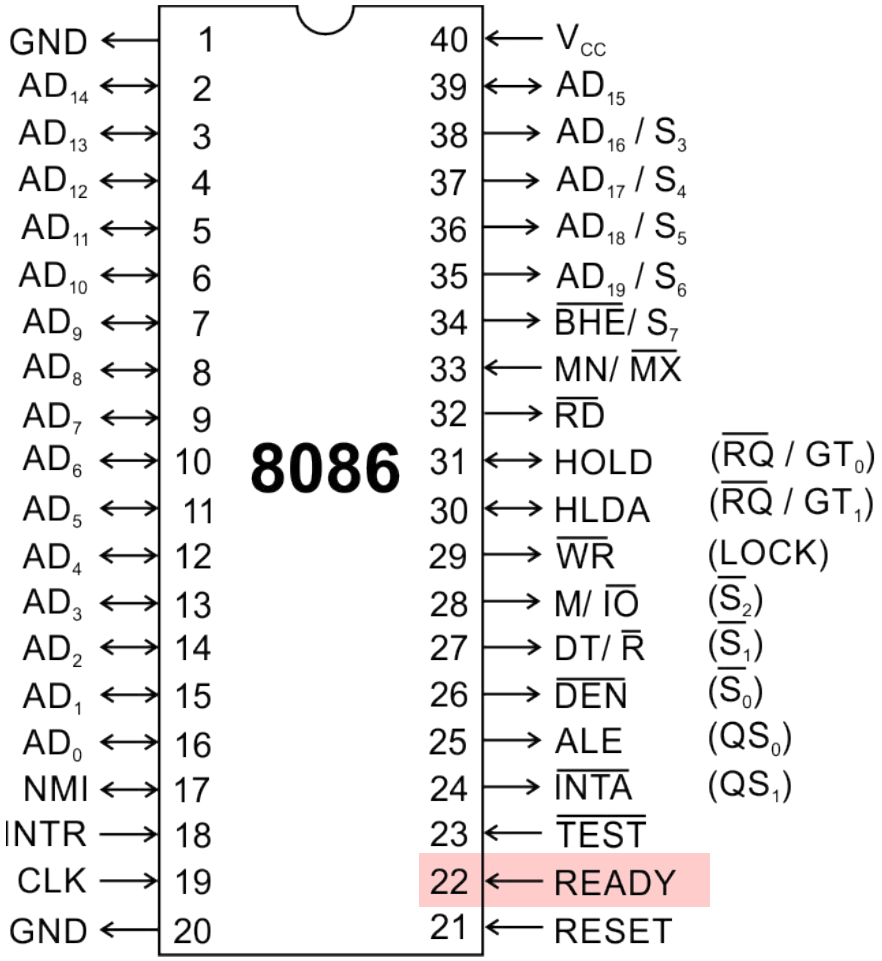
INTR Interrupt Request

This is a triggered input. This is sampled during the last clock cycles of each instruction to determine the availability of the request. If any interrupt request is pending, the processor enters the interrupt acknowledge cycle.

This signal is active high and internally synchronized.

Pins and Signals

Common signals



READY

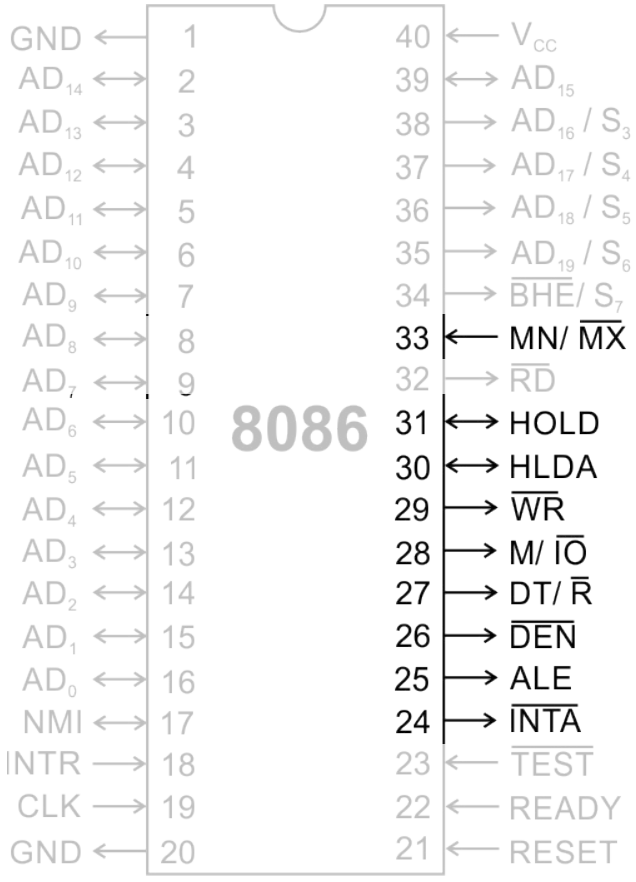
This is the acknowledgement from the slow device(addressed I/O) or memory indicates that peripheral is ready to transfer data.

The signal made available by the devices is synchronized by the 8284A clock generator to provide ready input to the 8086.

The signal is active high.

Pins and Signals

Min/ Max Pins



The 8086 microprocessor can work in two modes of operations : Minimum mode and Maximum mode.

In the minimum mode of operation the microprocessor do not associate with any co-processors and can not be used for multiprocessor systems.

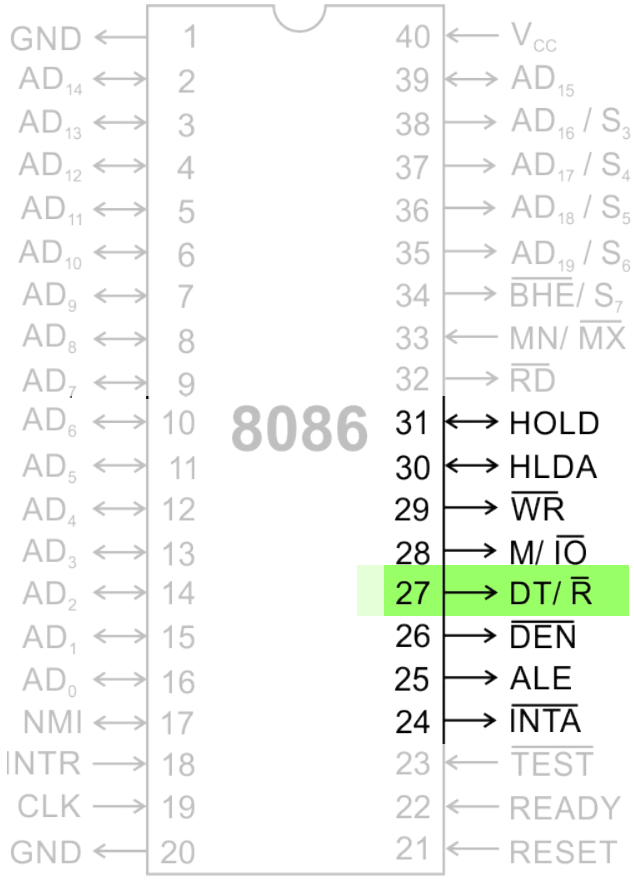
In the maximum mode the 8086 can work in multi-processor or co-processor configuration.

Minimum or maximum mode operations are decided by the pin MN/ MX(Active low).

When this pin is high 8086 operates in minimum mode otherwise it operates in Maximum mode.

Pins and Signals

Minimum mode signals



Pins 24 -31

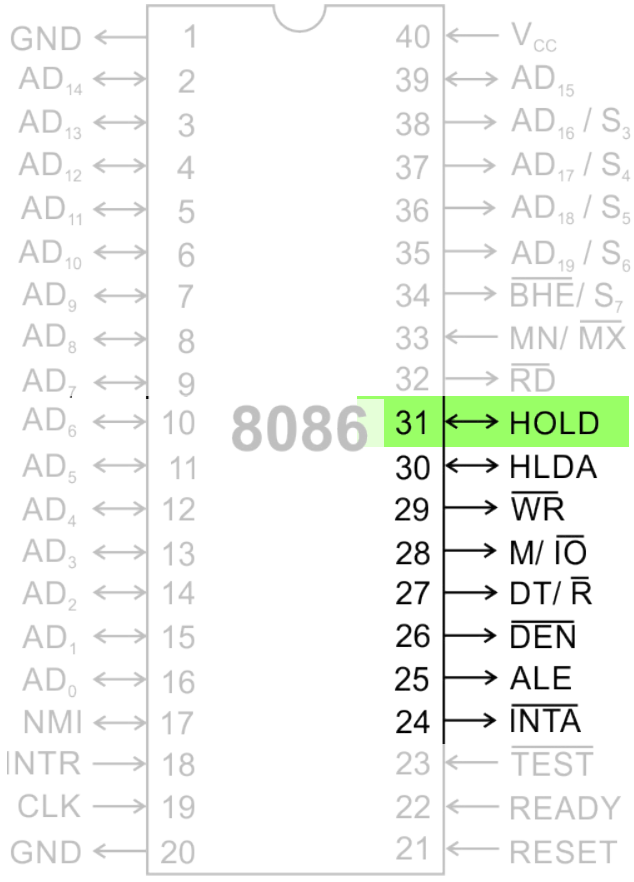
For minimum mode operation, the MN/ $\overline{MX}$ is tied to VCC (logic high)

8086 itself generates all the bus control signals

	(Data Transmit/ Receive) Output signal from the processor to control the direction of data flow through the data transceivers.HIGH-data r sent out,LOW- received.
	(Data Enable) Output signal from the processor used as out put enable for the transceivers
ALE	(Address Latch Enable) Used to demultiplex the address and data lines using external latches
	Used to differentiate memory access and I/O access. For memory reference instructions, it is high. For IN and OUT instructions, it is low.
	Write control signal; asserted low Whenever processor writes data to memory or I/O port
	(Interrupt Acknowledge) When the interrupt request is accepted by the processor, the output is low on this line.

Pins and Signals

Minimum mode signals



Pins 24 -31

For minimum mode operation, the MN/ $\overline{MX}$ is tied to VCC (logic high)

8086 itself generates all the bus control signals

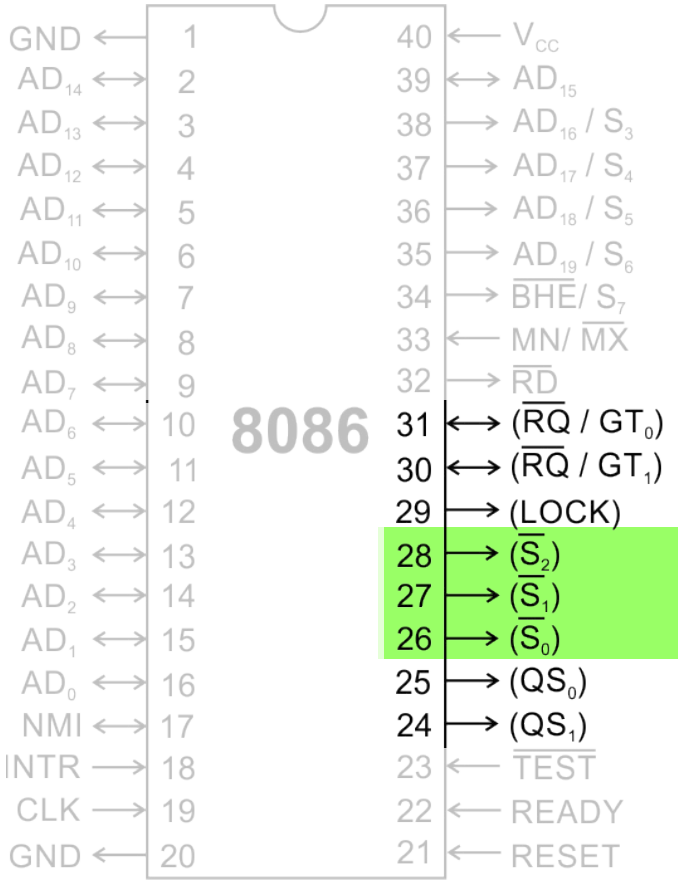
HOLD	**Input signal to the processor form the bus masters as a request to grant the control of the bus.** **Usually used by the DMA controller to get the control of the bus.**
HLDA	**(Hold Acknowledge) Acknowledge signal by the processor to the bus master requesting the control of the bus through HOLD.** **The acknowledge is asserted high, when the processor accepts HOLD.**

Pins and Signals

Maximum mode signals

During maximum mode operation, the MN/ $\overline{MX}$ is grounded (logic low)

Pins 24 -31 are reassigned



Status signals; used by the 8086 bus controller to generate bus timing and control signals. These are decoded as shown.
Signals are connected to bus controller Intel 8288. It generates memory and I/O access control signals.

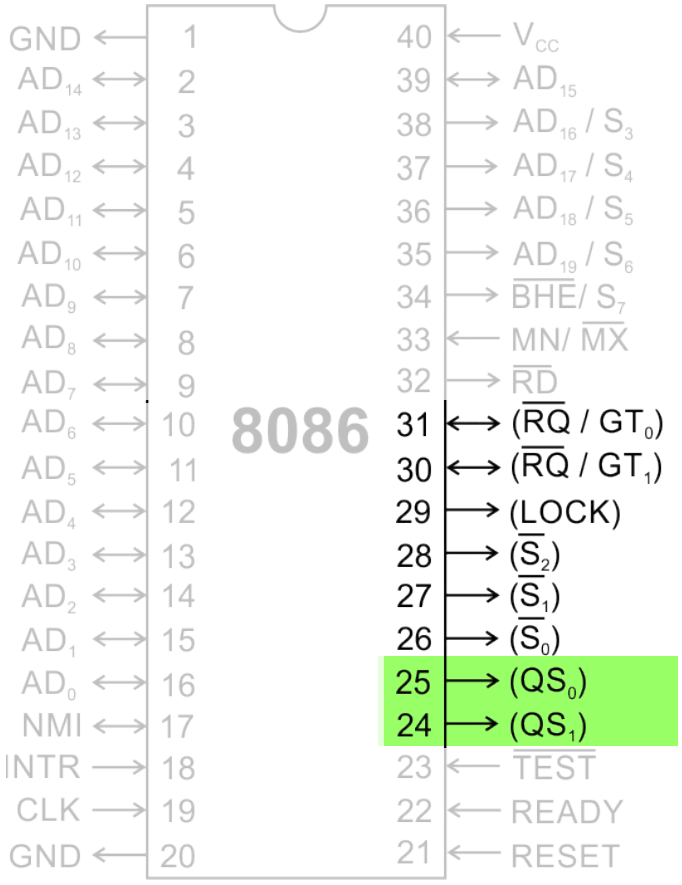
Status Signal			Machine Cycle
$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	
0	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive/Inactive

Pins and Signals

Maximum mode signals

During maximum mode operation, the MN/ $\overline{MX}$ is grounded (logic low)

Pins 24 -31 are reassigned



(Queue Status) The processor provides the status of queue in these lines.

The queue status can be used by external device to track the internal status of the queue in 8086.

The output on QS_0 and QS_1 can be interpreted as shown in the table.

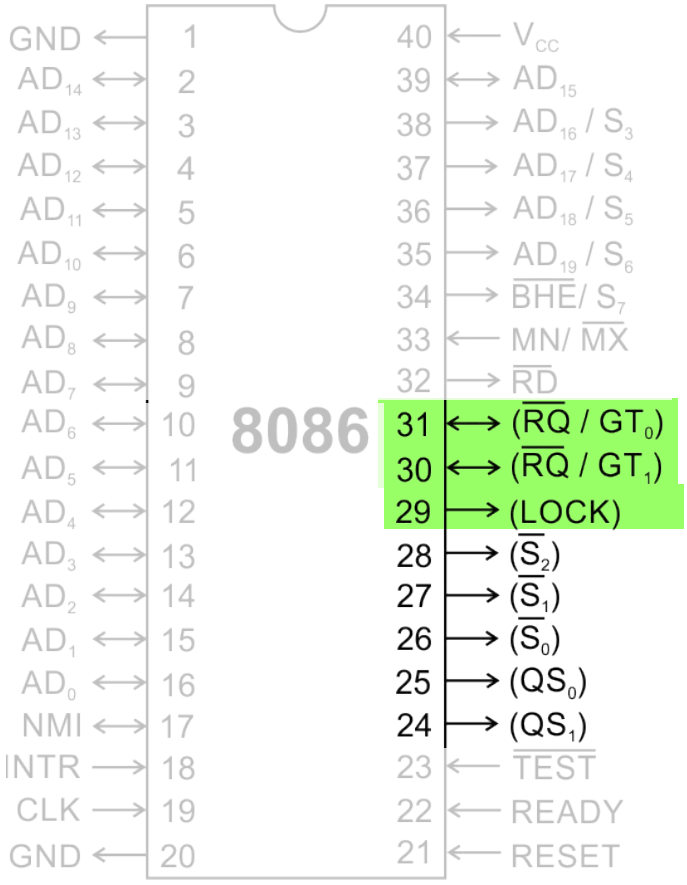
Queue status		Queue operation
QS_1	QS_0	
0	0	No operation
0	1	First byte of an opcode from queue
1	0	Empty the queue
1	1	Subsequent byte from queue

Pins and Signals

Maximum mode signals

During maximum mode operation, the MN/ $\overline{MX}$ is grounded (logic low)

Pins 24 -31 are reassigned



Pins and Signals

Maximum mode signals

During maximum mode operation, the MN/ $\overline{MX}$ is grounded (logic low)

Pins 24 -31 are reassigned

WR(LOW) ALE DEN(LOW) DT/R(LOW)	Not available directly from the processor. These signals are available from the controller 8288.


Thank you!