8279 Keyboard/Display Controller

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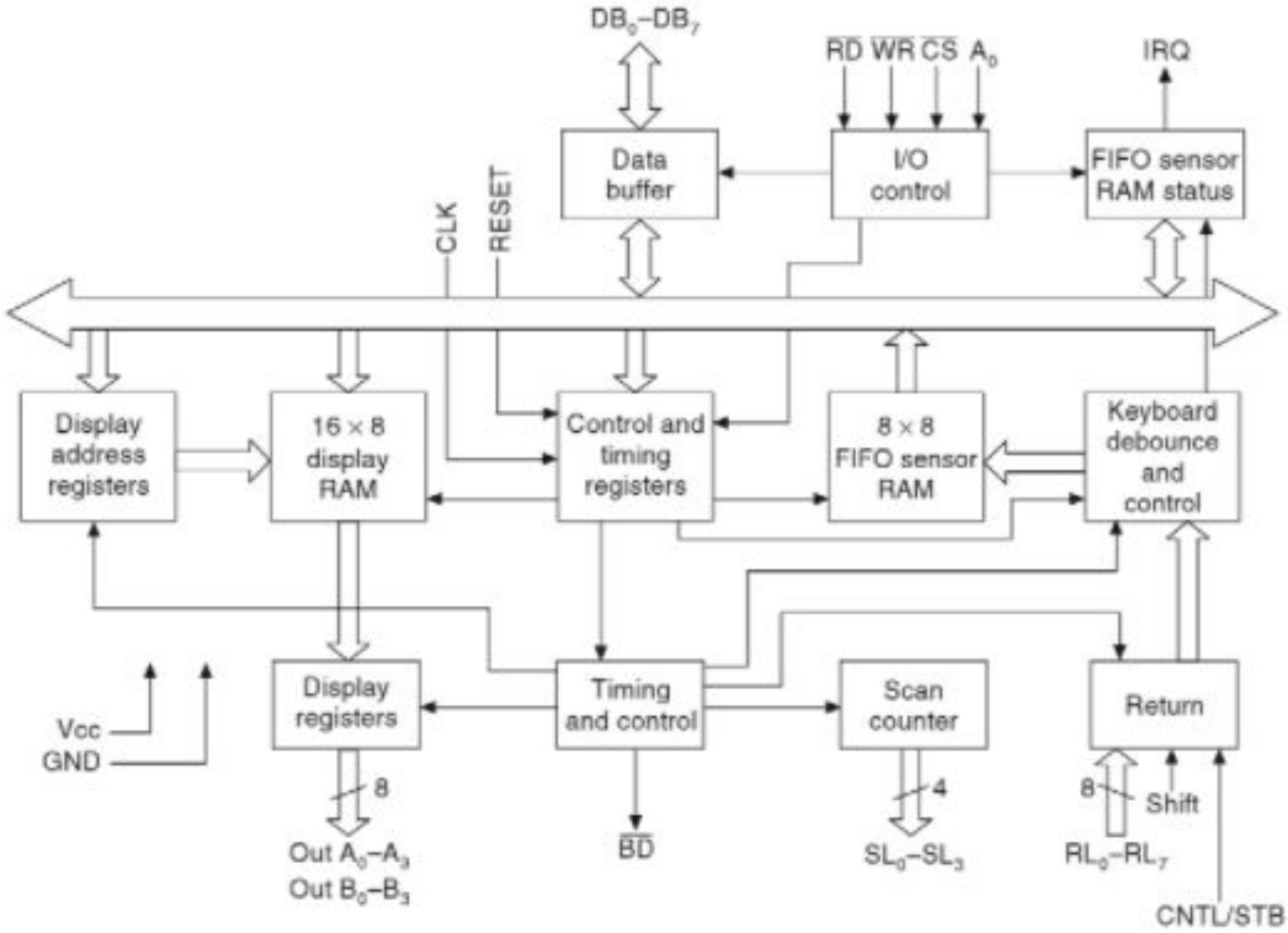
Features of 8279 PKDC

1. It consists of general purpose programmable keyboard and display input/output interfacing device.
2. The 8279 performs simultaneous display operations.
3. The 8279 operates in three input modes:
   (a) Scanned keyboard mode
   (b) Scanned sensor mode
   (c) Strobed input entry mode
4. The 8279 consists of 8-character keyboard FIFO.
5. Two-key lockout and N-key rollover with contact debounce.
6. It consists of dual 8 or 16 numerical display.
7. It consists of single 16-character display.
8. Left or right entry, 16-byte display RAM.
9. Mode programmable from microprocessor.
10. Interrupt output to signal microprocessor when there is keyboard or sensor data available.
11. It consists of 8-byte FIFO to store keyboard information.
12. 16-byte internal display RAM for display refresh. This RAM is readable by the microprocessor.

Architecture of 8279 PKDC



- **Data Buffer**

The 3-state, bidirectional, 8-bit data bus is used to interface the 8279 PKDC data bus to the system data bus. It is internally connected to the data bus, and its outer pins D_7–D_0 are connected to the system data bus directly.

- **DB_0-DB_7 :** These are bidirectional data bus lines. The data and command words to and from the CPU are transferred on these lines.

- **I/O Control**

The directions of data buffer are decided by read and write control signals. When signal read is activated, then it transmits data to the system. When write signal is activated, then it receives data from the system data bus. The pins A_0, $\overline{RD}$, $\overline{RD}$ select the command, status or read/write operations carried out by the microprocessor with the 8279 PKDC.

- **$\overline{RD}$, $\overline{WR}$ (Input / Output) READ / WRITE :** These input pins enable the data buffers to receive or send data over the data bus.

- **A_0(Address lines) :** A high on this line indicates the **transfer of a command or status information**. A low on this line indicates the transfer of data. This is used to select one of the internal registers of 8279.

- **$\overline{CS}$:** Chip Select – A low on this line enables 8279 for normal read or write operations. Other wise, this pin should remain high.

- **Display Address Registers**

The display address registers holds the address of the display RAM location, currently being written or read by the microprocessor. The contents of these registers are automatically updated by the 8279 PKDC to accept the next data entry by the microprocessor.

- **16 × 8 Display RAM**

The 16-byte (16 × 8) display RAM contains the 16 bytes of the data to be displayed on the sixteen seven-segment display in the encoded scan mode.

During initialization of the 8279 PKDC, all locations are loaded with clear code (00) or blank code. The microprocessor can be read or write this RAM. The address of the location to be accessed is specified by command word. During each digit time, the contents of the selected location are transferred into display register. In the encoded mode, the 8279 uses first eight locations or all locations, and in the decoded mode, the 8279 uses only first four locations.

- **Control and Timing Registers**

The 8279 PKDC provides 8 controls and timing registers which are distinguished by higher three bits of the command word. To access these registers A_0 address lines should be high ($A_0 = 1$). These registers store the keyboard and display modes and other operating conditions of the 8279 PKDC. The operations of these registers operation are affected by the reset signal.

- **Keyboard Debounce and Control**

In scanned keyboard mode, it debounces, encodes and stores encoded value into FIFO key closure. It also saves status of shift and control keys into FIFO. It also updates the information stored into FIFO/sensor RAM status register.

In sensor matrix mode, the debounce logic is inhibited and the contents of the return lines are directly transferred to the corresponding location of sensor RAM.

- **Display Registers**

The display registers hold the codes of the character to be displayed. They are divided into two nibbles called nibble A and nibble B. Both of these nibbles can be blanked or inhibited individually. During each digit scan, the contents of some registers hold the blanking code of the display.

- **Timing and Control**

The timing and control logic unit generates all internal keyboards and displays control signals, and controls the basic timings for the operation of the circuit. It also generates BD (Blinking display) signal. This unit provides proper key scan, row scan, display scan, and debounce timings.

- **Scan Counter**

The scan lines SL_0–SL_3 are used to scan keyboard matrix and display digits. These lines can be programmed as encoded or decoded using the mode control word register. In the encoded mode, it provides a 3-bit or 4-bit binary count on scan lines, and in the decoded mode, it decodes the lower two bits of count and provides decoded value on scan lines.

- **Return lines**

The return lines are used to scans for a key closure rowwise. The return lines RL_0–RL_7 are buffered and latched by this block, also these lines are not scanned in strobed input mode.

- **RESET :** This pin is used to reset 8279. A high on this line reset 8279.

- **CLK :** This is a clock input used to generate internal timing required by 8279.

- **IRQ :** This interrupt output lines goes **high** when there is a **data in the FIFO sensor RAM**. The interrupt lines **goes low with each FIFO RAM read operation** but if the FIFO RAM further contains any key-code entry to be read by the CPU, this pin again goes high to generate an interrupt to the CPU.

- **V_{ss}, V_{cc} :** These are the ground and power supply lines for the circuit.

- **SL_0-SL_3-Scan Lines :** These lines are used to **scan the key board matrix and display digits**. These lines can be programmed **as encoded or decoded**, using the mode control register.

- **RL_0 - RL_7 - Return Lines :** These are the input lines which are connected to **one terminal of keys**, while the **other terminal of the keys are connected to the decoded scan lines.** These are normally high, but pulled low when a key is pressed.

- **SHIFT :** The status of the shift input lines is stored along with each key code in FIFO, in scanned keyboard mode. It is pulled up internally to keep it high, till it is pulled low with a key closure.

- **CNTL/STB- CONTROL/STROBED I/P Mode :** In keyboard mode, this lines is used as a **control input and stored in FIFO** on a key closure. The line is a strobed lines that enters the data into FIFO RAM, in strobed input mode. It has an **interrupt pull up**. The lines is pulled down with a key closer.

- **OUT A_0 – OUT A_3 and OUT B_0 – OUT B_3 :** These are the output ports for two 16*4 or 16*8 internal display refresh registers. The data from these lines is synchronized with the scan lines to scan the display and keyboard. The two 4-bit ports may also as one 8-bit port.

- **$\overline{BD}$ – Blank Display :** This output pin is used to blank the display during digit switching or by a blanking closure.


Thank you!