8255 PPI

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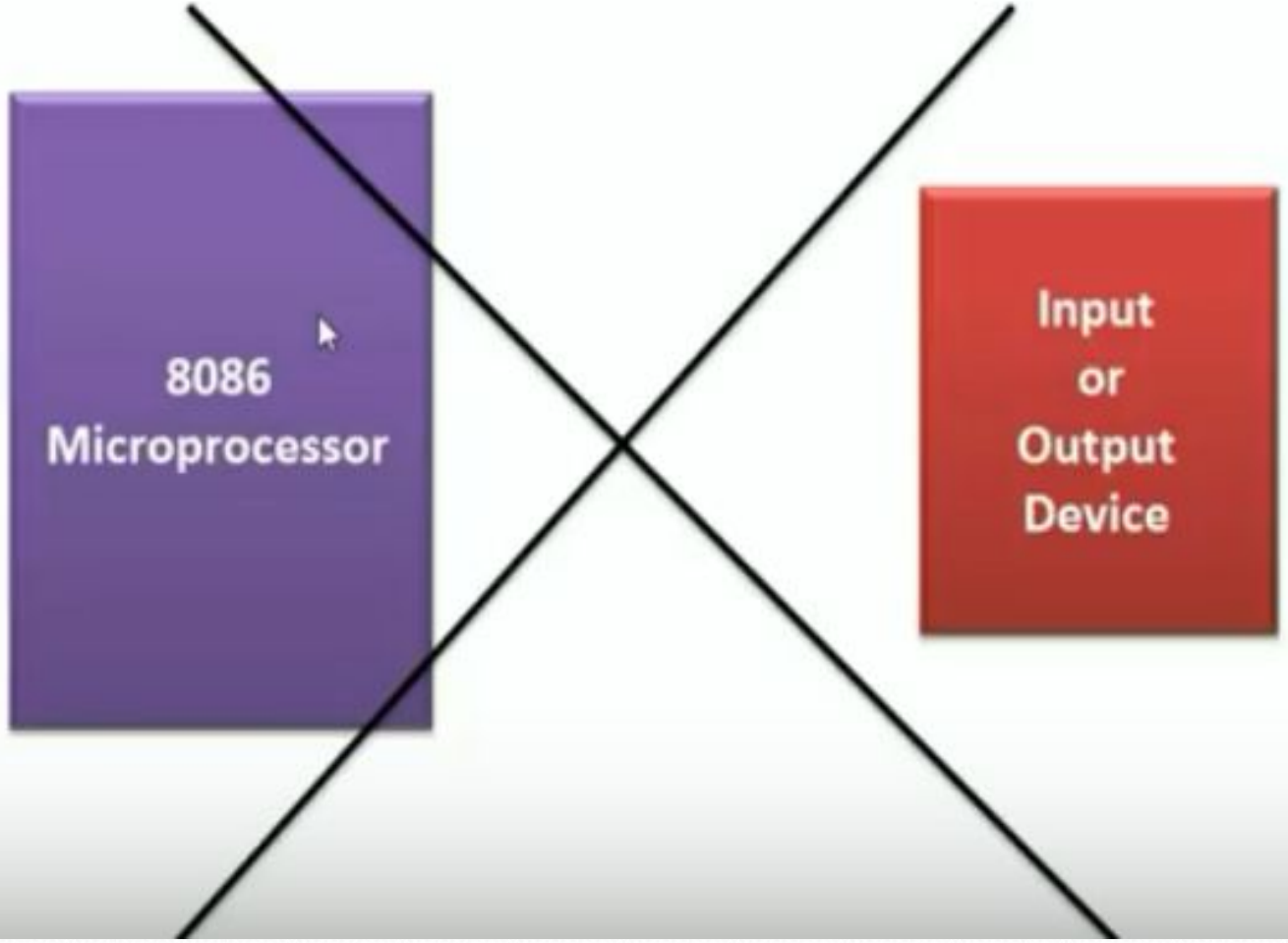
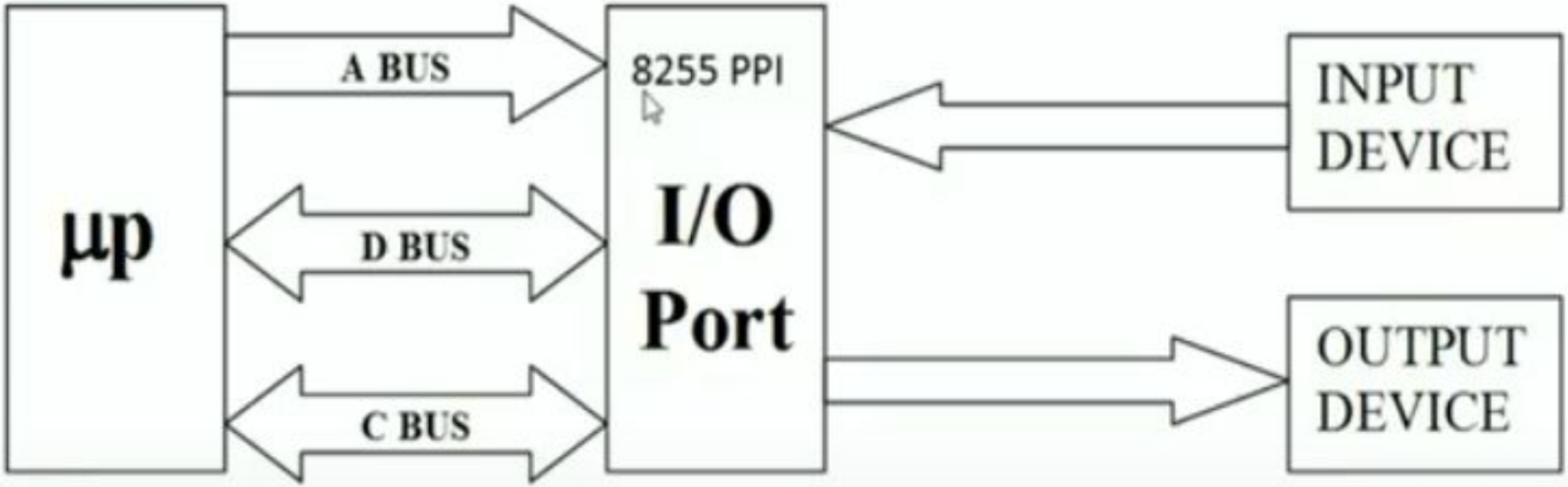
Input or Output Device Can not connected Directly



Basic Concept



8255 - PPI

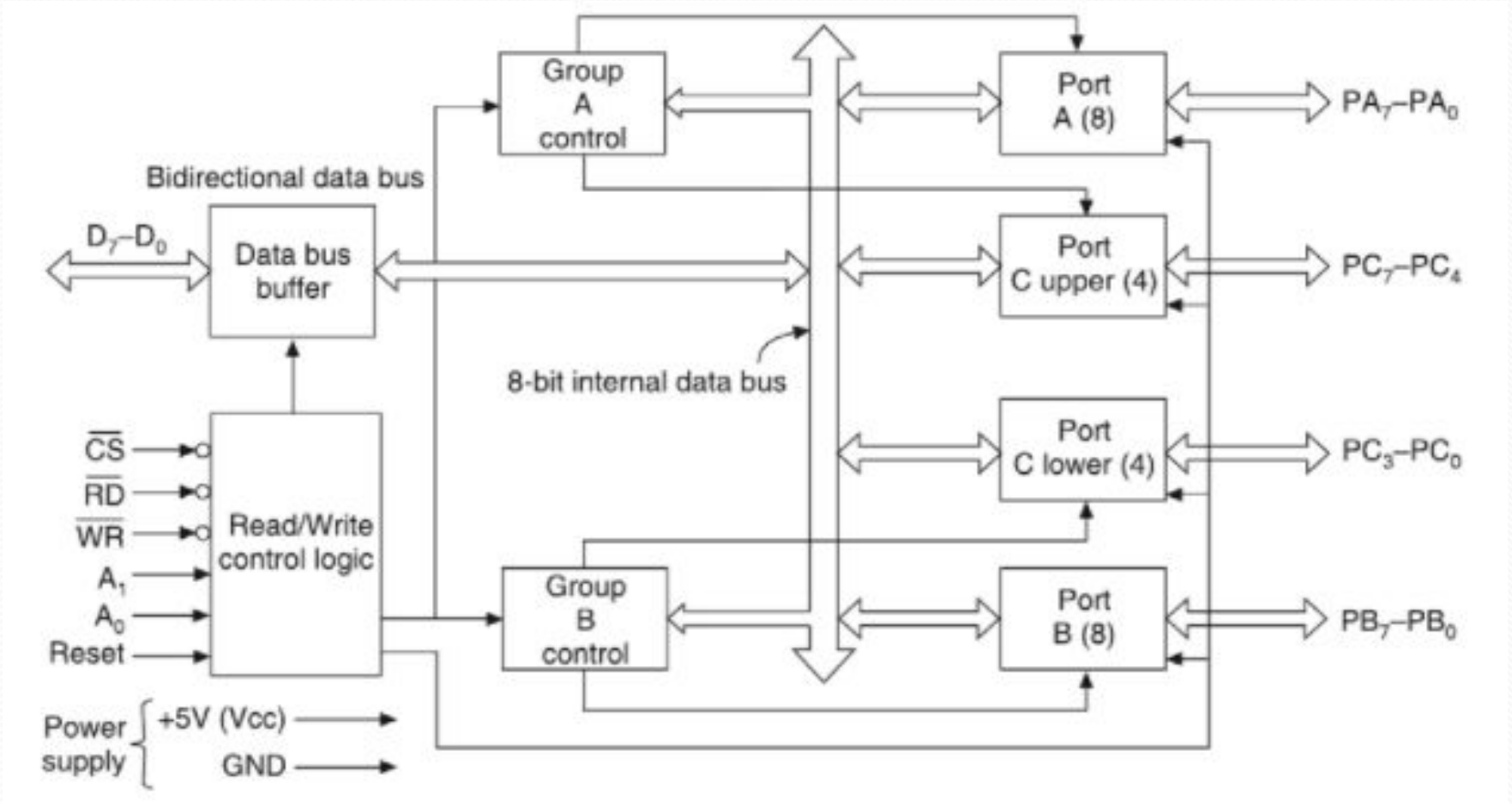
- The 8255A is a general purpose programmable I/O device designed to transfer the data between I/O Device and the processor. It can be used with almost any microprocessor.

- It consists of three 8-bit bidirectional I/O ports (24 I/O lines) which can be configured as per the requirement.

Features of 8255 PPI

1. It is programmable parallel input/output device.
2. High speed and low power consumption due to 3µ silicon gate CMOS technology.
3. 3V to 6V single power supply.
4. Full static operation.
5. The PPI has 24 I/O programmable pins in groups of 12 pins, which are arranged as three 8-bit ports (Port A, Port B, Port C).
6. Bit set/reset function for the Port C pins.
7. The 8255 PPI can interface any TTL compatible I/O device to the microprocessor.
8. It is fully compatible with the Intel microprocessor families.
9. The 8255 PPI is used for interface to the keyboard and the parallel printer port in many of the personal computers.
10. The 8255 PPI is also used to control the timer and the read data from the keyboard interface.

Architecture of 8255



Architecture of 8255

The programmable peripheral interface (PPI) 8255 is also called parallel input/output port chip. The 8255 PPI chip is compatible with Intel's 8-bit, 16-bit and higher version microprocessors. The 8255 PPI contains 24 input/output lines which may be individually programmed in two groups of twelve lines each. These 24 I/O lines are arranged as three 8-bit ports called Port A, Port B and Port C. The two individual groups of I/O pins are called Group A and Group B. The Group A contains Port A (8-bit). The Port C_{Upper} (4-bit). Group B contains Port B (8-bit) and Port C_{Lower} (4-bit).

All of this port of the 8255 PPI can function independently as input or as output by programming the bits of an internal register of the 8255 called control word register. The internal architecture or functional block diagram of the 8255 PPI is shown

The functional block diagram of the 8255 contains the following blocks:

1. Data bus buffer
2. Read/Write control logic
3. Group A and Group B control
4. Port A, Port B and Port C

1. Data Bus Buffer

The 8-bit bidirectional, tristate data bus buffer is used to interface the 8255 data bus with the system data bus. It is internally connected to the internal data bus and its outer pins D_7–D_0 are connected to the system data bus directly. The directions of the data bus are decided by the read or write control signals. When the read signal is activated, then it transmits data to the system data bus, and when the write signal is activated, it receives data from the system data bus. The data bus buffer receives or transmits data and also the control word format for the 8255 PPI.

2. Read/Write Control logic

This block accepts inputs from system control bus and address bus. The control signals used are $\overline{RD}$ and $\overline{WR}$, and address signals used are A_1, A_0 and $\overline{CS}$. From these five signals $\overline{RD}$ and $\overline{WR}$ are connected to $\overline{IOR}$, $\overline{IOW}$, or $\overline{MEMR}$, $\overline{MEMW}$ depending on the types of mapping used. $\overline{RD}$ and $\overline{WR}$ decide the operation to be performed, i.e. write data to the 8255 PPI or read data from the 8255PPI. A_1 and A_0 are directly connected to address lines A_1 and A_0 of system address lines. The $\overline{CS}$ is connected to the chip select decoder; the selection of the 8255 is enabled or disabled by $\overline{CS}$ signal. If logic 0 is applied on this signal, the 8255 PPI is selected or when 1 is applied on this signal, the 8255 PPI is rejected. The address bits A_1 and A_0 select or activate the corresponding port and control word register.

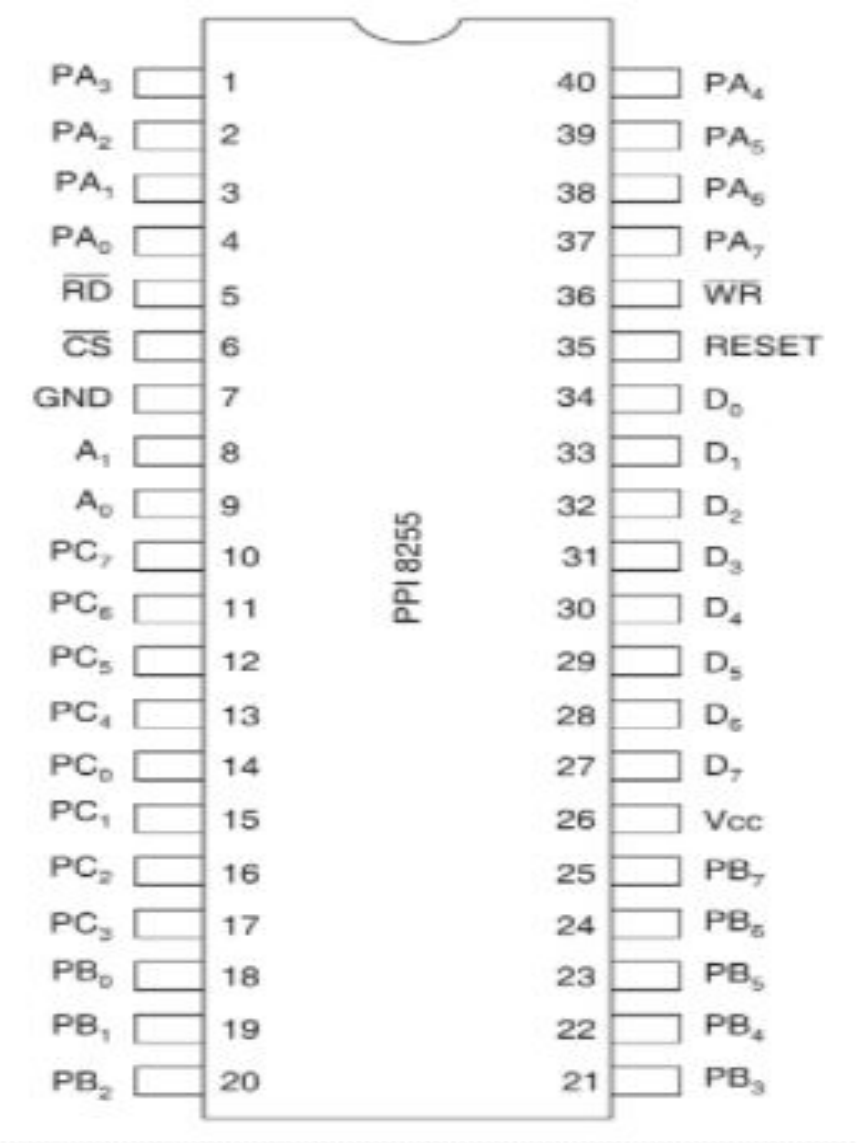
3. Group A and Group B Control

The 8255 PPI is divided into two groups called Group A and Group B. Group A consists of Port A and Port C_{UPPER}, and Group B consists of Port B and Port C_{lower}. So, each group consists of total 12 bits. Each group is accessed or programmed by software. The selection of port bits in Group A and Group B is done by mode operation.

4. Port A, Port B and Port C

The ports A, B and C consist of an 8-bit bidirectional data output letch or buffer and 8-bit data input buffer. The functions of Ports A, B and C are decided by the control bit pattern available in the control word register, and also on the mode operation. The Port C bits are divided into two parts—Port C_{upper} and Port C_{lower}. The Port C bits can be used as simple input/output, handshake signals and status signal, inputs. For handshake signals and status signals it is used in coordination with Port A and Port B. The major feature of Port C includes the direct bit set/reset mode in which only the bits of Port C are operated.

Pin Configuration of 8255



D_7–D_0

Data bus
Pins: 27 to 34
Type: Input/Output
These are the 8-bit bidirectional data bus lines, which carry data or control word to/from microprocessor.

$\overline{CS}$

Chip select
Pin: 6
Type: input

This is an active low input signal used to select the 8255. If $\overline{CS}$ is 0, then it enables the communication between the 8255 PPI and the microprocessor.

$\overline{RD}$

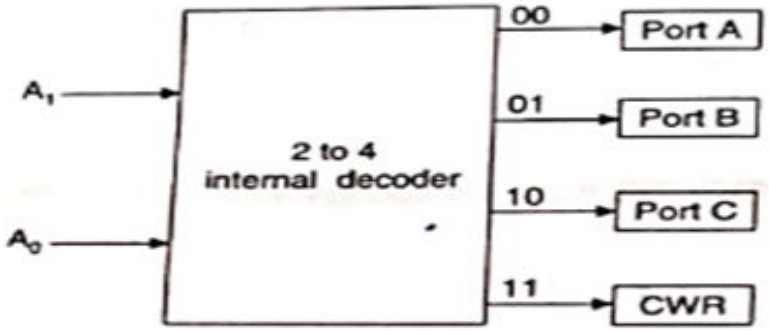
Read
Pin: 5
Type: Input
This is an active low signal. A low on this input enables the 8255 PPI to send the data or status information to the microprocessor on the data bus. Alternatively, low on this signal means it allow the microprocessor to read from the 8255 PPI.

$\overline{WR}$

Write
Pin: 36
Type: Input
This is an active low signal. A low on this pin enables the microprocessor to write data or control words into the 8255 PPI.

A_1 and A_0

Address lines
Pins: 8 and 9
Type: Input
A concerned signal on these input lines allows selecting Port A, Port B, Port C, and the control word register. These address lines are internally decoded to generate one of the ports, and control word register, as shown



Internal decoder of 8255.

A_1	A_0	*Selected port*
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Control word register (CWR)

Also, these address lines along with $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ form the following operations for the 8255:

$\overline{RD}$	$\overline{WR}$	A_1	A_0	$\overline{CS}$	*Input operation (Read)*
0	1	0	0	0	Port A to data bus
0	1	0	1	0	Port B to data bus
0	1	1	0	0	Port C to data bus
0	1	1	1	0	Illegal operation*

*Read operation is not allowed for CWR

$\overline{RD}$	$\overline{WR}$	A_1	A_0	$\overline{CS}$	*Output operation (Write)*
1	0	0	0	0	Data bus to Port A
1	0	0	1	0	Data bus to Port B
1	0	1	0	0	Data bus to Port C
1	0	1	1	0	Data bus to CWR

$\overline{RD}$	$\overline{WR}$	A_1	A_0	$\overline{CS}$	*Input operation (Read)*
X	X	X	X	1	Data bus tristated
1	1	X	X	0	Data bus tristated

Reset

Reset
Pin: 35
Type: Input
This is an active high input signal used to reset the 8255 PPI. When the signal is applied on this pin, it clears the control word register, and all ports are set to input mode. Reset out of microprocessor is connected to reset of the 8255 PPI.

PA_7–PA_0

Port A
Pins: 1 to 4 and 37 to 40
Type: Input/Output
These are the 8-bidirectional input/output pins used to send data to the device (peripheral) or to read data from the device connected with the 8255.

PB_7–PB_0

Port B
Pins: 18 to 25
Type: Input/Output
These are the 8-bidirectional input/output pins used to send data to the device (peripheral) or to read data from the device connected with the 8255.

$PC_7 - PC_0$

Port C

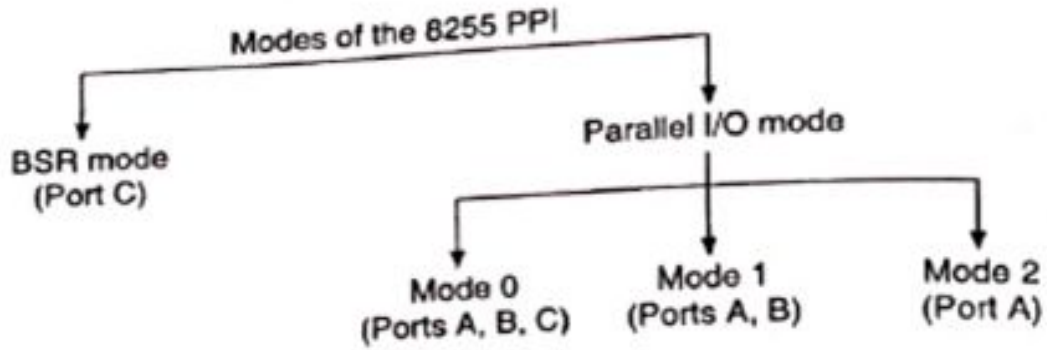
Pins: 10 to 17

Type: Input/Output

These are the 8-bidirectional input/output port pins. These 8 lines are divided into two sections, PC_0 to PC_3 called PC_{lower}, and PC_4 to PC_7 called PC_{upper}. These can be individually used to load or transfer 4 bits of data from PC_{lower} and PC_{upper} sections.

Modes of Operation

The modes of operation of 8255 consist of two basic modes—bit set/reset mode and parallel input/output mode. In the BSR mode, only Port C pins are affected and the individual pins of Port C (PC_0 to PC_7) can be used to set or reset. In the parallel input/output mode, the 8255 ports work as programmable input/output ports. The input/output mode is providing three different modes: Mode 0, Mode 1, and Mode 2 to support different types of applications

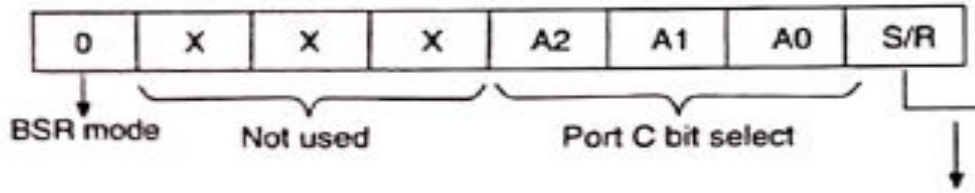


Different types of modes.

The selection of mode either BSR or parallel I/O is done by bit pattern loaded in control word register. The control word register is selected, when $A_1 = 0$, $A_0 = 0$, $\overline{CS} = 0$, and $\overline{WR} = 0$. The read operation is not allowed for control word register. The two basic modes are selected by D_7-bit of control word register. When $D_7 = 0$, then BSR (bit set/reset mode) is selected, and when $D_7 = 1$, then parallel I/O mode is selected.

1. BSR Mode

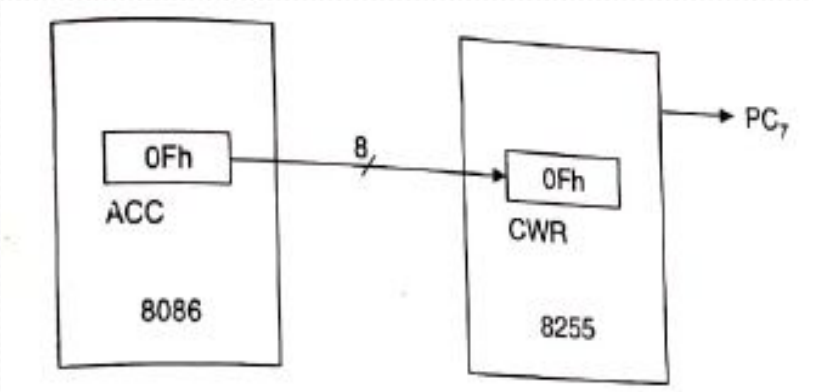
The BSR mode is used to set or reset the individual bits of Port C pins by writing the control word in the control word register. The control word format for the BSR mode is shown in the Figure . A control word with $D_7 = 0$ is identified as BSR mode and it does not alter any previously transmitted control word with $D_7 = 1$ (Parallel I/O mode), therefore, the I/O operations of Port A and Port B are not affected by the BSR mode. The individual pin (address) of Port C is selected by address A2 A1 A0 of control word register. The bit is set or reset is decided by the S/R (D_0) bit of control word format. The bits D_6, D_5 and D_4 do not care bit for the BSR mode and it is not used.



A2	A1	A0	Bit select
0	0	0	PC_0
0	0	1	PC_1
0	1	0	PC_2
0	1	1	PC_3
1	0	0	PC_4
1	0	1	PC_5
1	1	0	PC_6
1	1	1	PC_7

Control word format in BSR mode.

Write a set of instructions to set PC7 pin of 8255 PPI having ctrl word register at 47h.



The control word format of BSR mode to set PC_7 pin of 8255 PPI is shown below.

0	X	X	X	A2	A1	A0	S/R	
0	0	0	0	1	1	1	1	= 0F h

The given address of CWR is 47h. Here last bit, i.e. A_0 is 1, it means that the 8255 PPI is connected with the odd bank. And bits A_1 A_2 = 11, so this address is belonging to CWR of the odd bank of the 8255 PPI.

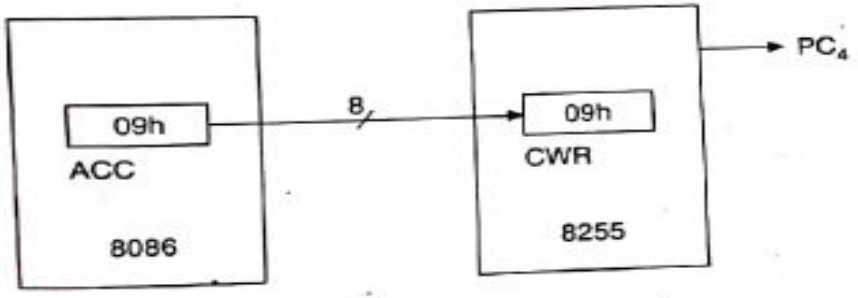
```
MOV AL, 0Fh     ; Initialization of control word to set PC7
OUT 47h, AL     ; Transfer on control word
HLT / INT3
```

Write a set of instructions to set bit 4 of Port C. Assume the address of Port A is 10H.

Solution: The given address of Port A is 10h, so the address of control word register is 16h

0000 0001

Ports	*Address*
Port A	10
Port B	12
Port C	14
CWR	16



The control word format of the BSR mode to set PC_7 pin of the 8255 PPI is shown below.

0	X	X	X	A2	A1	A0	S/R	
0	0	0	0	1	0	0	1	= 09 h

```
MOV AL, 09h
OUT 16h, AL
HLT / INT3
```

Write an assembly language program to set PC6,PC2 and PC4 bits of Port C, and reset them after 50 ms.

The control word format to set PC_6, PC_2 and PC_4 is given below.

0	X	X	X	A2	A1	A0	S/R	
0	0	0	0	1	1	0	1	= 0Dh == PC_6 Set
0	0	0	0	0	1	0	1	= 05h == PC_2 Set
0	0	0	0	1	0	0	1	= 09h == PC_4 Set

The control word format to reset PC_6, PC_2, and PC_4 is given below.

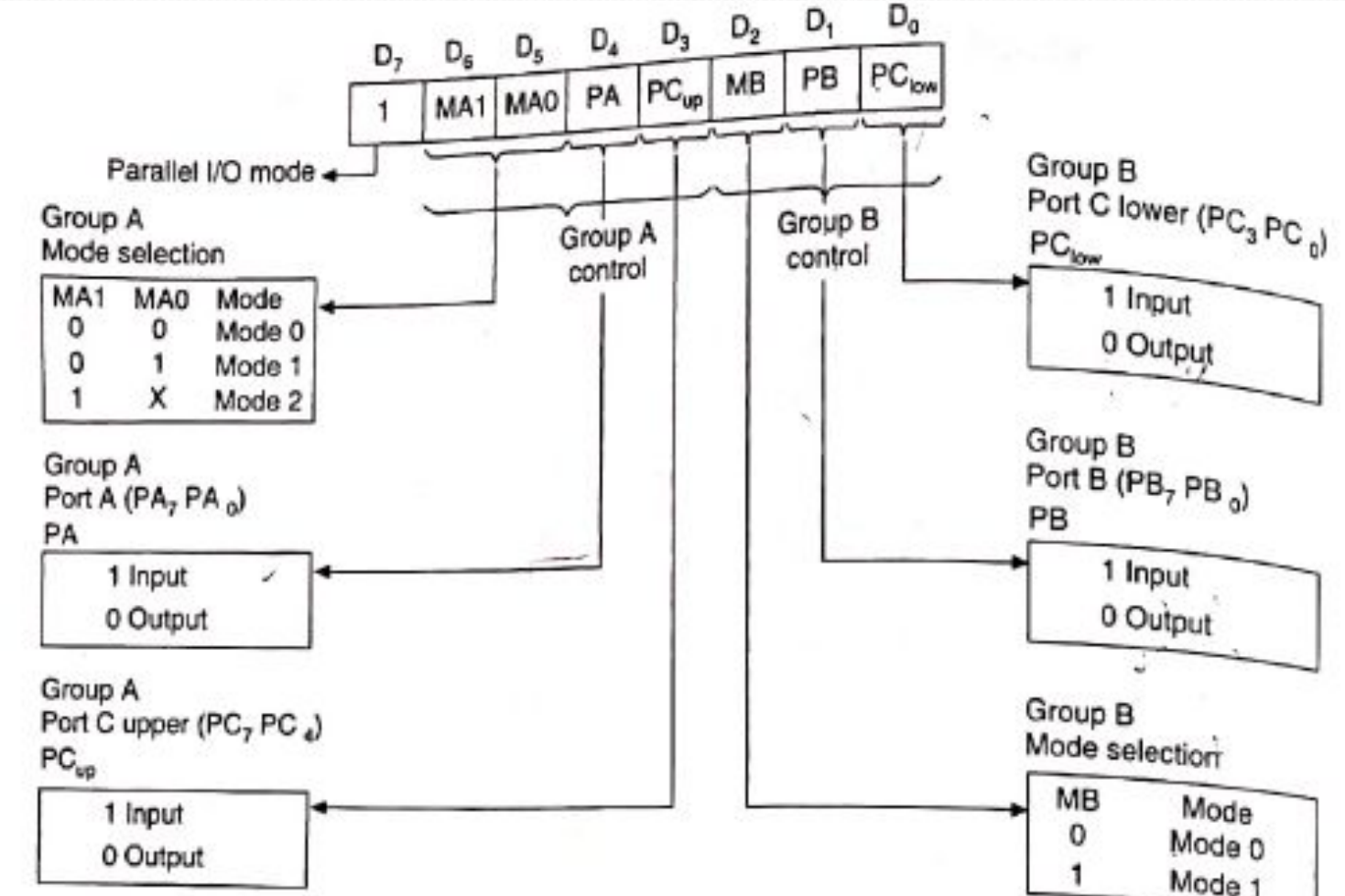
0	X	X	X	A2	A1	A0	S/R	
0	0	0	0	1	1	0	0	= 0Ch == PC_6 Reset
0	0	0	0	0	1	0	0	= 04h == PC_2 Reset
0	0	0	0	1	0	0	0	= 08h == PC_4 Reset

Cont..

- Here the address of CWR is not given, so assume add. of Port A is ooh, so the address of CWR is o6h.

```
MOV AX, 3000h
MOV SS, AX          ; Initialize stack memory segment
MOV SP, 0100H
MOV AL, 0Dh
OUT 06h, AL         ; Set PC6 of Port C
MOV AL, 05h
OUT 06h, AL         ; Set PC2 of Port C
MOV AL, 09h
OUT 06h, AL         ; Set PC4 of Port C
CALL DELAY          ; Delay of 50 ms
MOV AL, 0Ch
OUT 06h, AL         ; Reset PC6 of Port C
MOV AL, 04h
OUT 06h, AL         ; Reset PC2 of Port C
MOV AL, 08h
OUT 06h, AL         ; Reset PC4 of Port C
HLT / INT3
```

Parallel I/O mode



Control word format in parallel I/O mode.

Example 1: Initialize 8255 PPI to define:

1. Port A output in mode 1.
2. Port B input in mode 0.
3. Port C_{low} as output.

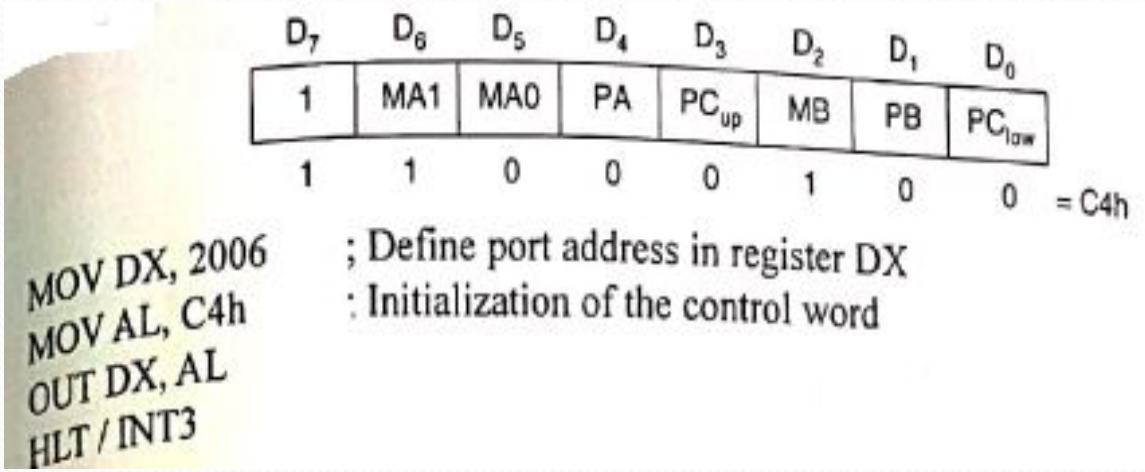
   8 bit address of CWR is 06h.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	MA1	MA0	PA	PC_{up}	MB	PB	PC_{low}
1	0	1	0	0	0	1	0 = A2h

If the information about the port whether it is input or output is not given, then always assume the default case, i.e. when system is reset, all the ports are defined in output ports. In this problem, port PC_{UP} is not given, so assume it is an output port.

```
MOV AL, A2h      ; Initialization of the control word
OUT 06h, AL
HLT / INT3
```

Example 2: Write an initialization sequence to define Port A in mode 2, Port B as output in mode 1. The 16 bit address of CWR is 2006h.



D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1	MA1	MA0	PA	PC_{up}	MB	PB	PC_{low}	
1	1	0	0	0	1	0	0	= C4h

```
MOV DX, 2006    ; Define port address in register DX
MOV AL, C4h     : Initialization of the control word
OUT DX, AL
HLT / INT3
```

Example 3: Define the 8255 PPI Port A as input in mode 0, Port B as input in mode 1. The address of control word register is 81507.

Solution: It is important to note that the address of CWR is given as 81507. This is a memory address and hence in this case memory mapped I/O technique, is used. In memory mapped I/O technique, always use memory-related instruction, instead of IN/OUT instruction. Or, if I/O ports are used as memory, then IN and OUT instructions cannot be used.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1	MA1	MA0	PA	PC_{up}	MB	PB	PC_{low}	
1	0	0	1	0	1	1	0	= 96h

```
MOV AX, 8150h
MOV DS, AX          ; Define data memory segment
MOV [0007], 96h     ; Transfer control word format on memory address
HLT / INT3
```

Example 4: Write a set of Instructions to perform the following:

1. Initialize Port A as input in mode 0
2. Initialize Port B as output in mode 1
3. Initialize Port C upper as output and Port C lower as input

Solution: The address of CWR is not given, so assume address of CWR is 06h

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1	MA1	MA0	PA	PC_{up}	MB	PB	PC_{low}	
1	0	0	1	0	1	0	1	= 95h

```
MOV AL, 95h
OUT 06h, AL
HLT / INT3
```

Example 5: Write an ALP that will input the contents of Port B and Port C, and then perform ANDing and output the result to Port A. Port A is connected with address 10600H.

Solution: The address of Port A is 10600h and it is a 20-bit address, so memory mapped input/output technique is used. The addresses of Ports B, C and CWR are given below.

Ports	*Address*
Port A	10600h
Port B	10602h
Port C	10604h
CWR	10606h

```
MOV AX, 1000h
MOV DS, AX      ; Initialize data segment memory at address 1000
MOV AL, [0602h] ; Read Port B
MOV BL, [0604h] ; Read Port C
AND AL, BL      ; Perform ANDing the contents of Port B and Port C
MOV [0600h], AL ; Writes data to Port A
```


Thank you!