

Roll Number: _____

Thapar Institute of Engineering & Technology, Patiala

Department of Computer Science & Engineering

'U' grade EXAMINATION (March 2022)

B. E.(COE) (Final Year): Semester VIII,
X

Course Code: UCS704

Course Name: Embedded System Design

March 8, 2022

Tuesday, 17:30

Time: 2 Hours, M. Marks: 45

Faculty: Dr. Gaurav Mishra

Note: All questions carry equal marks. Attempt any five questions.

Assume missing data, if any, suitably.

Q.1 (a)	What is an embedded system? What are the features required to design an embedded system?	(5)																				
(b)	Why the personal computer (PC) is not considered as embedded system?	(4)																				
Q.2 (a)	What are the differences between the microprocessor and microcontroller?	(4)																				
(b)	What are the different components required to design the temperature monitor embedded system (explain with the block diagram)?	(5)																				
Q.3 (a)	Draw the internal diagram of DRAM chip. List the steps of typical read operation in DRAM cell	(5)																				
(b)	Discuss the scenario when memory shadowing is useful in the operation of an embedded system.	(4)																				
Q.4 (a)	Differentiate following: a. SRAM and DRAM b. Timer and counter c. LED and OLED d. Microprocessor and Microcontroller e. EPROM and EEPROM	(9)																				
Q.5	Consider the following set of three real-time periodic tasks: <table><tr><th>Task</th><th>Start (ms)</th><th>Processing time(ms)</th><th>Period (ms)</th><th>Deadline (ms)</th></tr><tr><td>T1</td><td>20</td><td>25</td><td>150</td><td>100</td></tr><tr><td>T2</td><td>40</td><td>10</td><td>50</td><td>50</td></tr><tr><td>T3</td><td>60</td><td>50</td><td>200</td><td>200</td></tr></table> i. Check whether the three given tasks are schedulable under Rate Monotonic Algorithm. Show all intermediate steps in your computation. ii. Draw the Gantt chart for the one cycle of execution i.e. tasks arrives periodically till the maximum processing time task finishes its one execution completely.	Task	Start (ms)	Processing time(ms)	Period (ms)	Deadline (ms)	T1	20	25	150	100	T2	40	10	50	50	T3	60	50	200	200	(3) (4) (2)
Task	Start (ms)	Processing time(ms)	Period (ms)	Deadline (ms)																		
T1	20	25	150	100																		
T2	40	10	50	50																		
T3	60	50	200	200																		

	iii. When T3 finishes its first execution.	
Q.6 (a)	What are the types of robots? Write the steps for designing an autonomous robotic system.	(5)
(b)	What are the actuators used for designing the robotic system?	(4)
Q.7 (a)	Explain the working of following 8051 pin i. PSEN(bar) ii. EA(bar) iii. RXD	(5)
(b)	Write two differences between RISC and CISC architectures. Also mention name of one processor for each.	(4)

Roll Number: _____ Group: _____ Name: _____

Thapar Institute of Engineering & Technology, Patiala
Department of Computer Science & Engineering
'U' Grdae Sessional Quiz

B. E. - IV Year (COE), Semester VIII, X

Course Code: UCS704

March 8, 2022, Tuesday

Course Name: Embedded System Design

Name Of Faculty: GAM

Time: 15 mins, M. Marks: 15

Q.1 Which of the following is the properties of Field Programmable Gate Array (FPGA)?

- (a) Reconfigurable circuit
- (b) Easier entry-barrier
- (c) Both of (a) and (b)
- (d) None of the above

Q.2 Internet of Things is driven by combination of:

- (a) Sensors and Connectivity
- (b) Connectivity and People & Processes
- (c) Sensors and People & Processes
- (d) Sensors, Connectivity, and People & Processes

Q.3 Which of the following is the Local Network technologies in IoT?

- (a) Bluetooth
- (b) LoRa
- (c) ZigBee
- (d) Sigfox

Q.4 What is the standard form of LPWAN?

- (a) Low-Protocol Wide-Area Network
- (b) Low-Power Wireless-Area Network
- (c) Low-Power Wide-Area Network
- (d) None of the Above

Q.5 What does FRIDGE stand for?

- (a) the floating-point programming design environment
- (b) the fixed-point programming design environment
- (c) floating-point programming decoding
- (d) fixed-point programming decoding

Q.6 Earliest deadline first algorithm assigns priorities according to

- (a) periods
- (b) deadlines
- (c) burst times
- (d) None of the these

Q.7 If the period of a process is 'p', then the rate of the task is

- (a) p^2 (b) $2 \cdot p$
- (c) $1/p$ (d) P

Q.8 is the maximum time a task can wait and still meet its deadline.

- (a) Laxity (b) Tardiness
- (c) Schedule time (d) None of these

Q.9 The Von-Neumann architecture has:

- (a) separate bus just for peripherals (b) separate bus for Code & Data memory
- (c) common bus for Code & Data memory (d) none of these

Q.10 The internal RAM memory of the 8051 is:

- (a) 32 bytes (b) 64 bytes (c) 128 bytes (d) 256 bytes

Q.11 In LCD, which hex command performs the function of 'Display on, cursor on and blinking'?

- (a) 0x0A (b) 0x0C
- (c) 0x0F (d) 0x0E

Q.12 If the deadline of an embedded system cannot complete its task within its deadline then it is called _____ type of embedded system.

- (a) Soft real time
- (b) Hard real time
- (c) Stand alone
- (d) Networked embedded system

Q.13 How many transistor are required for storing 1 byte data in DRAM

- (a) 32 (b) 48 (c) 8 (d) 16

Q.14 In BMI, when a person close his/her eyes..... waves are obtained

- (a) High power alpha (b) Low power alpha
- (c) High power beta (d) Low power beta

Q.15 The processor clock is used as reference clock is during the operation of

- (a) Counter (b) Timer
- (c) Stop watch (d) System clock

Roll Number: _____ Group: _____ Name: _____

Thapar Institute of Engineering & Technology, Patiala
Department of Computer Science & Engineering
'U' Grdae Sessional Lab Quiz

B. E. - IV Year (COE), Semester VIII, X

Course Code: UCS704

Course Name: Embedded System Design

Time: 5 mins, M. Marks: 5

March 8, 2022, Tuesday

Name Of Faculty: GAM

Q.1 #60 \$finish indicates

- (a) End of simulation time
- (b) End of simulation at 60 time units
- (c) Suspend simulation at 40 time units
- (d) None of these

Q.2 What is the system task to suspend simulation in Verilog?

- (a) \$finish
- (b) \$monitor
- (c) \$display
- (d) \$stop

Q.3 if m is declared as register type variable (reg m;), the default value of m is:

- (a) 1
- (b) Z
- (c) 0
- (d) x

Q.4 The carry propogation of half adder can be expressed as (inputs are m and n)

- | | |
|----------------------|-----------------|
| (a) $B_p = m+n$ | (b) $B_p = m.n$ |
| (c) $B_p = \sim m.n$ | (d) $B_p = m^n$ |

Q.5 Setup time is:

- (a) Minimum time the data must arrive before active clock edge
- (b) Maximum time the data must arrive before active clock edge
- (c) Minimum time the data cannot change after active clock edge
- (d) None of the above