Roll Number: Thapar Institute of Engineering & Technology, Patiala Department of Computer Science & Engineering WRITTEN EXAMINATION B. E.(COE) (Final Year): Semester-VII Course Code: UCS704/UCS614 B.E. MBA (COE) (Third Year): Semester-V Course Name: Embedded System Design October 18, 2021 Monday, 10:00 AM - 12:00 Noon Time: 2 Hours, M. Marks: 45 Faculty: DET, AA, NS, GAM Note: All questions carry equal marks. Attempt any five questions. Assume missing data, if any, suitably. Q.1 (a) Computers use 2's complement representation for negative numbers. (3) Write two advantages for representing signed numbers using 2's complement over 1's complement. ii. How to identify, whether, the given number is positive or negative in 2's complement representation? Show the process of adding -120 and 45 using 2's complement to justify your answer. (b) What are the different components required to design the temperature (3) monitor embedded system (explain with the block diagram)? (c) 8051 is an 8-bit microcontroller unit (MCU), why? An 8051 based system (3) uses a clock of 16 MHz frequency. Calculate the time period of one machine cycle. Q.2 (a) Describe the working of Power on Reset (PoR) circuit for 8051 (3) microcontroller. What is the use of Schmitt trigger in PoR circuit? (b) Draw the internal diagram of DRAM chip and clearly show all the (3) components and connections. (3) (c) Describe the use of tightly coupled memory in embedded systems. **Q.3 (a)** LED display is a popular choice to show alphanumeric information in many embedded system applications. Twelve segments LED is one such display (3)

- Q.3 (a) LED display is a popular choice to show alphanumeric information in many embedded system applications. Twelve segments LED is one such display device which uses 12 LEDs to represent various alphabet and numbers as shown in Fig.1. Assume common cathode connection to connect all 12 LEDs, "a" as the LSB bit, "l" as MSB bit and refer remaining bits in order. Find 12 segment codes (in binary) to display following characters.
 - i. V (capital)
 - ii. Y (capital)
 - iii. D (capital)

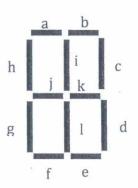


Fig. 1:12 segment LED display

- (b) What do you understand by DPST (double pole single throw) switch type?(3) Give one application of this contact type along with the diagram.
- (c) What is the primary advantage of using differential pair to transmit the data over single ended in Analog to Digital Converter (ADC)? According to your opinion, which one is more preferable in serial ADCs? Justify your answer.
- Q.4 (a) How Spread spectrum technique help to protect from eavesdropping? (2)
 - (b) What is frequency re-use in cellular technology? (2)
 - (c) Draw the block diagram for Brain Machine Interface (BMI) and briefly (5) describe its each component.
- Q.5 Consider the following set of three independent real-time periodic tasks running on a uniprocessor using Rate Monotonic Scheduling (RMA). Show the intermediate steps in your computation and answer following:

Task	CPU burst (msec)	Period (msec)	Deadline (msec)
T1	20	100	100
T2	30	150	150
Т3	90	200	200

- i. Determine whether the given set of periodic real-time tasks is RMA (2) schedulable using Liu and Layland test.
- ii. Draw the Gantt chart and check the schedulability of the given-set of periodic tasks using RMA. If T2 is able to meet its first deadline then at what time T2 finish its first execution.
- iii. Assume that context switching overhead does not exceed 1mSec and (2) is to be taken under consideration in scheduling computation.

 Determine whether the given set of periodic real-time tasks is RMA schedulable using Liu and Layland test.
- iv. Draw the Gantt chart (for part c) and check the schedulability of the given-set of periodic tasks using RMA. If T1 is able to meet its first deadline then at what time T1 finish its first execution.
- v. Is a good algorithm for scheduling of hard real-time tasks tries to (1) complete each task in the shortest possible time? Justify your choice.

- * Q.6 (a) Many DSP processors boast of 'zero overhead loops'. What do they mean by this?
 - (b) How use of Super Harvard architecture in Digital Signal Processing (DSP) processor may improve the performance of DSP algorithms? How does it contribute to obtain "high memory bandwidth"?
 - (c) Digital Signalling Processing (DSP) processors either use fixed point and (4) floating point representation. Name one DSP processors for each which uses fixed point and floating point representation. Represent the number (1.234)₁₀ in fixed point representation with scaling factor of 10⁻⁴.
 - Q.7 Consider the designing of Smart Home Safety System to monitor the nearby activities. The system not only monitors but also reacts at an early stage in view of premise safety. In case of any vulnerability identified, system issues suitable control action. The system captures data in real time and support device level processing along with sending data to the processing unit for real time decision making. The security system uses wireless sensor network (WSN) and radio frequency identification technology (RFID) to support advanced security features. The highlight of system is as follows:
 - RFID readers and other autonomous devices work together for process integration and real time decision making.
 - Wireless sensor network nodes enhance the capabilities of RFID tags, results to smart devices.
 - Replacement of WSN nodes with RFID tags removes the barrier of power drain.
 - Use of WSN provides wireless connectivity balance the low communication range of RFID tags.
 - i. Draw the block diagram for the Smart Home Safety System. (5)
 - ii. What type of embedded system the Smart Home Safety System you (1) consider and why?
 - iii. Identify the suitable architecture of your proposed solution. (2)
 - iv. How you ensure the correctness and robustness of system? (1)